Exhibit 7

FORM PTO-1449 (modified) To: U.S. Department of Commerce --REPLACEMENT-- Patent and Trademark Office				Atty. Dkt. No.	043326-000-0021	Client Ref.		
INFORMATION DISCLOSURE STATEMENT FORM 1449				Inventor(s): **Jayesh R. BHAKTA et al.**				
				Patent No.: **7,619,912**				
				Date of Issue: **November 17, 2009**				
	Page	1	o f 1	Examiner: SOFOCLEOUS, Alexander		Group Art Unit: 2824		

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
w/hc	2006/0117152	06-01-2006	AMIDI ET AL.	711	154	
√	6,209,074	03-27-2001	DELL ET AL.	711	170	

FOREIGN PATENT DOCUMENTS

	Document Number	Date (dd/mm/yy)	Country	Applicant Name	English Abstract	Translation available

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

whc	Murdocca, Miles J., Heuring, Vincent P.; Principles of Computer Architecture, Prentice Hall, Inc., Upper Saddle River, NJ, 2000; pp.243-252.
	"Quad Band Memory (QBMA™): DDR200/266/333 devices producing DDR400/533/667" (the "QBMA Reference"), published by the QBMA Alliance, Platform Conference, San Jose, California, January 23-24, 2002.
√	JEDEC Standard No. 21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Revision 1.3, Release 11b, January 2002.

Examiner	Date Considered: 8/23/2010

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

20995   7590   04/04/2011
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EXAMINER
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ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
04/04/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Inter Parte Reexamination Communication Transmittal Form

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CENTRAL REEXAMINATION UNIT

Transmittal of Communication to Third Party Requester
Inter Partes Reexamination

REEXAMINATION CONTROL NO. : 95000578
PATENT NO. : 7619912
TECHNOLOGY CENTER : 3999
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified Reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the inter partes reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an ex parte reexamination has been merged with the inter partes reexamination, no responsive submission by any ex parte third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the Central Reexamination Unit at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

PTOL-2070(Rev.07-04)

http://uspto-a-pattr-3/CRU/InterPatesTransmitalForm.aspx?CtrlNO=95000578

OFFICE ACTION IN **INTER PARTES** *REEXAMINATION*	Control No. ~~95/000,579~~ 95/000,578 +95/001,339	**Patent Under Reexamination** 7619912
	Examiner Woo H. Choi	**Art Unit** 3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on _____
Third Party(ies) on <u>8 June 2010, 20 October 2010, 21 October 2010</u>

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:
<u>2</u> MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.
For Third Party Requester's Comments on the Patent Owner Response:
30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892
2. ☒ Information Disclosure Citation, PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims <u>1-51</u> are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☒ Claims <u>21</u> are confirmed. [Unamended patent claims]
4. ☐ Claims _____ are patentable. [Amended or new claims]
5. ☒ Claims <u>1-20 and 22-51</u> are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____ ☐ are acceptable ☐ are not acceptable.
8. ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has:
    ☐ been received. ☐ not been received. ☐ been filed in Application/Control No <u>95000578</u>.
10. ☐ Other _____

U.S. Patent and Trademark Office
PTOL-2064 (08/06)

Paper No. 20110329

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INTER PARTES REEXAMINATION OFFICE ACTION

1.   This is an *inter partes* reexamination of U.S. Patent No. 7,619,912 ('912 patent). On

February 28, 2011 three *inter partes* proceedings, 95/000,578, 95/000,579, and 95/001,339

initiated based upon three different requests by Requester 2, Requester 3, and Requester 1,

respectively, have been merged. Clams 1-51 are subject to reexamination. The references

discussed herein are as follows:

- U.S. Patent No. 5,926,827 ("Dell 1");

- U.S. Patent No. 6,209,074 ("Dell 2");

- *Quad Band Memory (QBM^{TM}): DDR 200/266/333 devices producing DDR400/533/667*, QBM Alliance, Platform Conference, San Jose, California, January 23-24, 2002 ("QBMA");

- U.S. Patent No. 5,745,914 ("Connolly");

- U.S. Patent No. 6,414,868 ("Wong");

- U.S. Patent Application Publication No. 2006.0117152 ("Amidi");

- *Design Specification for PC2100 and PC1600 DDR SDRAM Registered DIMM*, JEDEC Standard No. 21-C, Revision 1.3, Release 11b, January 2002, ("JEDEC 21C");

- *Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications*, JEDEC Standard No. 82-4B, May 2003, ("JEDEC 82-4B");

- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79C, March 2003, ("JEDEC 79C");

- Micron, *DDR SDRAM RDIMM*, MT36VDDF12872 & MT36VDDF28672 Data Sheet © 2002, ("Micron");

- Murdocca, Miles, J., *Principles of Computer Architecture*, Prentice Hall, Inc., 2000 ("Murdocca").

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Statutory Bases for Rejections - 35 USC §§ 102 and 103

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Summary of Rejections

4.   The following list is the summary of rejections in this Office action.

Ground 1: Obviousness over QBMA and JEDEC 21C (Proposed by Requester 1)

        Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 2: Obviousness over QBMA and Dell 2 (Proposed by Requester 1)

        Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 3: Anticipation by Amidi (Proposed by Requesters 1 and 2)

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Rejection of claims 1, 3-4, 6-7, 9-11, 15, 18-20, 24-25, 28-29, 31-34, 36-37, 39,

and 41-43, proposed by Requesters 1 and 2, is **adopted**.

Rejection of claims 8, 22, 27, 38, 44, 45, and 50, proposed by Requester 2, is

adopted.

Rejection of claims 2, 5, 14, 23, 30, 40, 46, and 51, proposed by Requester 1, is

adopted.

Rejection of claim 21, proposed by Requesters 1 and 2, is **not adopted**.

Ground 4: Obviousness over Amidi (Proposed by Requester 1)

Proposed rejection of claims 1-15, 18-20, 23-25, 27-34, 36-43, 45-48, 50, and 51

is **adopted**.

Proposed rejection of claims 16, 17, and 21 is **not adopted**.

Ground 5: Obviousness over Amidi and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-15, 18-20, and 22-51 is **adopted**.

Proposed rejection of claims 16, 17, and 21 is **not adopted**.

Ground 6: Obviousness over Amidi and JEDEC Standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-

39, 41-45, and 50 is **adopted**.

Proposed rejection of claim 21 is **not adopted**.

Ground 7: Obviousness over Murdocca and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42 is **not**

adopted.

Ground 8: Anticipation by Dell 1 (Proposed by Requester 2)

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Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39,

41-45, and 50 is **not adopted**.

Ground 9: Obviousness over Dell 1 and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-

39, 41-45, and 50 is **adopted**.

Proposed rejection of claim 21 is **not adopted**.

Ground 10: Anticipation by Wong (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39,

41-45, and 50 is **not adopted**.

Ground 11: Obviousness over Wong and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-

39, 41-45, and 50 is **adopted**.

Proposed rejection of claim 21 is **not adopted**.

Ground 12: Obviousness over Micron and Connelly (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39,

41-45, and 50 is **adopted**.

Ground 13: Obviousness over Micro and Amidi (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-

39, 41-45, and 50 is **adopted**.

Proposed rejection of claim 21 is **not adopted**.

Discussion of Rejections

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Ground 1

5.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and

JEDEC 21C. The proposed rejection is **not adopted**.

6.   With respect to claims 1, 15, and 28, Requester alleges that QBMA discloses "a circuit

mounted to the printed board, the circuit comprising a logic element and a register" as claimed.

Requester identified the QBM switch disclosed in QBMA on page 17 as the circuit or the logic

element (see Request 1 pp. 42-43). The QBM switch shown on page 17 is reproduced below.

As shown in the figure above, the QBM switch takes 8-bits (C[0,7]) + two strobe signals (DQS

C), and three control signals (Enable, SB, BE CLK) on the DIMM side of the interface as inputs.

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In contrast, the claim requires "the logic element [to] receiv[e] a set of input control signals from the computer system, the set of input control signal comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." Thus, the claim requires the logic element to receive a set of at least four signals: one row/column address signal, two bank signals, and one chip-select signal. It is clear from the figure that none of the signals received by the QBM switch corresponds to any of the set of input signals required by the claim.

7.   Requester 1 alleges that QBMA discloses RAS and CAS signals. However, these signals are not address signals or a chip-select signal. Although Requester 1 also asserts, citing pages 17-20 and 23, that QBMA discloses a bank select signal which is supplied to the QBM switch, Requester 1 has failed to identify the bank select signals allegedly taught by QBMA from any of the figures on any of the cited pages. Requester 1 further alleges that the QBM controller shown on page 24 provides address and control signals to the memory DIMM. While Requester 1 is correct that address and control lines are shown on page 24, Requester 1 has failed to show how page 24 of QBMA teaches the "logic element" limitation above.

8.   Requester 1 also alleges "that providing such input control signals to a logic element was well known at the time of the invention" (see Request 1, p. 43). There is no evidence on the record that it was well known to provide the recited set of input signals to a QBM switch at the time of the invention. Based on the above allegation without evidence, Requester 1 concludes that "it would have been obvious to one of ordinary skill in the art to provide such input control signals to the logic element particularly given that such was standard in the industry at the time

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of the invention." Again, Requester 1 has provided no evidence that providing a row/column

address signal, bank address signals, and a chip-select signal to the QBM switch was standard in

the industry.

9.   With respect to claim 39, the claim recites an integrated circuit that comprises a logic

element, wherein the logic element receives bank address signals and at least one command

signal. As with the other independent claims, Requester 1 identified the QBM switch as the

logic element. However, as shown above, the QBM switch does not receive bank address signals

or a command signal as input.

10.   Requester 1 also alleges that the limitation "the at least one integrated circuit element

generating a plurality of output signals in response to the plurality of input signals, the plurality

of output signals comprising row address signals, column address signals, bank address signals,

command signals, and the first number of chip-select signals" is taught by the QBM switch

which "contains circuitry that takes address bits [0,7] from "C:DIMM connector side" and maps

to "A or B: memory chip side" address A[0,7] or B[0,7]" (see Request, p. 64). This allegation is

based on Requester's interpretation of C[0,7] signals, shown on page 17 of QBMA, as address

signals. While QBMA does not explicitly state whether C[0,7] is a set of address signals or data

signals, the Figure above shows that the set of 8-bit signals (C[0,7] is the only set of 8-bit signals

shown in the Figure) is associated with the two data strobe signals for circuitries A and B (DQS

C_A and DQS C_B). Thus, it is more likely than not that C[0,7] is a set of signal that represents 8

data bits, rather than address bits as asserted by Requester 1.

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Ground 2

11.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and Dell 2. The proposed rejection is **not adopted**.

12.   The Examiner initially notes that Requester 1's proposed rejection maps alleged teachings of the two references applied (QBMA and Dell 2) to limitations of individual claims in a claim chart without clearly ascertaining the differences between the prior art and the claims at issue (step 2 of the *Graham* v. *John Deere Co.* obviousness analysis framework). The proposed rejection does not make it clear as to which features from which references are to be applied in a combination to make a system that teaches all of the limitations of the claims. For example, the claim chart for claim 1, at pages 71-74 of the Request, maps every element of claim 1 to some teaching in Dell 2 appearing to allege that claim 1 is anticipated by Dell 2. Yet, the proposed rejection uses QBMA as the primary reference and Dell 2 as a secondary reference.

13.   With respect to claims 1, 15, and 28, Requester 1 alleges that the limitation "the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signal, and at least one chip-select signal" is taught by the combination of the QBM switch and Dell 2's logic circuit that receives "a number of address inputs an a number of bank address signals from a memory controller with said address input and bank address input signals corresponding to N bank memory devices" and that it would have been obvious to combine the teachings. As discussed

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above, the QBM switch does not receive any of the recited input signals. Dell 2 does not cure

this deficiency because while the passage cited in Request 1 discloses a logic circuit receiving a

number of address input and a number of bank address signals, Dell 2 does not teach that the

logic circuit receives a chip-select signal.

14.   Requester 1 alleges that it would have been obvious to combine the teachings of QBMA

and Dell 2 to produce a logic element which receives input control signals including at least one

row/column address signal, bank address signals, and a chip-select signal to facilitate memory

domain translation. However, Requester 1 has not explained how adding address signals and a

chip-select signal as inputs to the QBM switch facilitates memory domain translation. QBMA

does not disclose the use of the QBM switch for memory domain translation. Memory modules

disclosed in QBMA do not appear to handle row/column address and bank signals through the

QBM switch. Thus, it makes little sense to redesign the modules by rerouting the address/bank

signals through the QBM switch to use the QBM switch for memory domain translation

application when Dell's invention can be use for that purpose without any redesign.

15.   Requester 1 also alleges that the limitation "the circuit generating a set of output control

signals in response to the set of input control signals corresponding to the first number of DDR

memory device arrange in the first number of ranks" is taught by both QBMA and Dell 2,

without making it clear whether the combined system uses QBMA's teaching or Dell's teaching.

As discussed above, the QBM switch does not generate addresses. As to Dell 2's disclosure, the

passage cited by Requester 1 that allegedly teaches this limitation (c8:20-27) is a textual

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description of Figure 1A. Figure 1A shows remapping of address signal A12 as BA1. The rest

of the address signals and the bank signal BA0 are used as they are. Therefore, Dell 2's circuit

does not "generate a set of output control signals in response to the set of input control signals."

To the extent that remapping of A12 as BA1 can be considered "generating an output signal,"

Dell 2 teaches generating an output control signal BA1, not "output control signals" as required

by the claims.

16.   Claims also require the circuit to "generat[e] and transmit[] a second command signal and

the set of output control signals to the plurality of memory devices" in response to a first

command signal and the set of input control signal. Again, Requester 1 does not make it clear

whether the combined circuit is to use QBMA's teaching or Dell's teaching with respect to this

limitation. Requester asserts that QBMA's disclosure that a QBM uses standard DDR

commands teaches this limitation. However, the claim specifically requires the circuit to

respond to a first command by generating a second command. QBMA does not specifically

disclose that a QBM generates and transmits commands in response to standard DDR commands

or that it generates standard DDR commands in response to commands received by the circuit.

Likewise, the passage in Dell 2 cited by Requester 1 does not disclose a circuit that generates and

transmits a command in response to another command as required by the claims.

17.   Claim 39 recites limitations that are similar to those of claim 1 discussed above. See the

discussion of claim 1 above.

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Ground 3

18.   Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45,

and 50 are anticipated by Amidi. Proposed rejection of claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25,

27-29, 31-34, 36-39, 41-45, and 50, is **adopted**.

19.   Claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 are rejected

under 35 U.S.C. 102(e) as being as being anticipated by Amidi.

20.   With respect to claim 1, Amidi discloses **a memory module (Figure 4) connectable to a**

computer system, the memory module comprising:

   a printed circuit board (see Figure 4, 400);

   a plurality of double data rate (DDR) memory devices (404) mounted to the printed

circuit board, the plurality of memory devices having a first number of memory devices

arranged in a first number of ranks (see Figure 4, the module has four ranks); .

   a circuit mounted to the printed circuit board, the circuit comprising a logic element

and a register (408), the logic element receiving a set of input control signals (see Figure 6,

the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and signals) **from the**

computer system, the set of input control signals comprising at least one row/column

address signal (Add[n:0]), bank address signals (BA[1:0]), and at least one chip select signal

(cs0), the set of input control signals corresponding to a second number of memory devices

arranged in a second number of ranks, the second number of memory devices smaller than

the first number of memory devices and the second number of ranks less than the first

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number of ranks (see paragraphs 10-12, Amidi's invention is a transparent four rank module fitting into a memory socket meant for a two rank module), **the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks** (see Figure 6 and paragraph 52, "CPLD also ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules. For example, CPLD 604 generates rsc2 and rcs3 …"); **and**

> **a phase-lock loop device (412) mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of memory devices, the logic element, and the register.**

21.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see Figure 4, cs0 and cs1) **and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals** (rcs0a-rcs3a).

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22.   With respect to claim 4, **the first number of chip-select signals is two and the second number of chip-select signals is four** (see the discussion of claim 3 above).

23.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Figure 6, CPLD).

24.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (see Figure 6, the claim does not preclude the logic element that comprises the CLPD and the register).

25.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

26.   With respect to claim 9, **the register comprises a plurality of register devices** (Figure 8, 820, 822, 828, 830).

27.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board** (Figure 4A, ranks 0 and 2 are on the front side), **a third set of DDR memory devices on a second side of the printed circuit**

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board, and a fourth set of DDR memory devices on the second side of the printed circuit

board (Figure 4B, ranks 1 and 3 are on the back side), the DDR memory devices of the second

set spaced from the DDR memory devices of the first set, the DDR memory devices of the

fourth set spaced from the DDR memory devices of the third set (this is inherent as two

physical devices cannot occupy the same space at the same time).

28.   With respect to claim 11, the DDR memory devices of the second set are spaced from

the DDR memory devices of the first set in a direction along the first side and the memory

devices of the fourth set are spaced from the memory devices of the third set in a direction

along the second side (see paragraph 34, the devices are stacked on the front and the back side).

29.   With respect to claims 15 and 28 see the discussion of claim 1 above.

30.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

31.   With respect to claim 18, the command signal is transmitted to two ranks of the first

number of ranks at a time (see Figure 6 and paragraph 52).

32.   With respect to claim 19, the command signal comprises a refresh command signal

(see paragraph 52).

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33.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

34.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see Figure 6, register).

35.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Figure 6, CPLD).

36.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see Figure 6).

37.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

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38.   With respect to claims 31 and 32, see the discussion of claim 3 above.

39.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (see Figure 6).

40.   With respect to claim 34, **the first number of ranks is four and the second number of ranks is two** (paragraph 41).

41.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (paragraph 52).

42.   With respect to claim 37, **the input command signal is a precharge signal and the output command signal is a precharge signal** (paragraph 52).

43.   With respect to claim 38, **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.** See the discussion of claim 37 above.

44.   With respect to claim 39, see claims 1 and 3 above.

45.   Proposed rejection of claim 21 is **not adopted**. With respect to claim 21, Requester 1 alleges that paragraphs 37, 38 and 57 disclose the claim limitation. These paragraphs and

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Figures 4 and 6 appear disclose a register that stores input signals and transmit output signals during both column and row access procedures. However, there is no specific disclosure that an input signal stored during a row access procedure is stored for subsequent use during a column access procedure.

46.   Requester 1 asserts that claims 1-7, 9-11, 14, 15, 18-21, 23-25, 28-34, 36, 37, 39-43, 46, and 51 are anticipated by Amidi. Proposed rejection of claims 1-7, 9-11, 14, 15, 18-20, 23-25, 28-34, 36, 37, 39-43, 46, and 51, is **adopted**.

47.   With respect to claims 1, 3-4, 6-7, 9-11, 15, 18-20, 24-25, 28-29, 31-34, 36-37, 39, and 41-43, see above.

48.   <u>Claims 2, 5, 14, 23, 30, 40, 46, 51 are rejected under 35 U.S.C. 102(e) as being as being anticipated by Amidi.</u>

49.   With respect to claim 2, **the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure** (see Figures 6A and 6B, register 608, the register is used to store and transmit addresses for row and column access**).**

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50.   With respect to claim 5, **the circuit receives and buffers a plurality of row/column**

address signals of the input control signals during a row access procedure and sends the

buffered plurality of row/column address signals to the plurality of DDR memory devices

during a subsequent column access procedure (see Figures 6A and 6B, register 608).

51.   With respect to claim 14, **the set of input control signals corresponds to a first**

memory density, and the set of output control signals corresponds to a second memory

density, the second memory density greater than the first memory density (see paragraph

41, "The CPLD 410 emulates a two ranks memory module on the four rank memory module

400. CPLD 410 allows a system having a memory socket with only two chip select signals

routed to interface with a four rank memory module where typically a two rank memory module

couples with the memory socket.").

52.   With respect to claims 23, 30, and 51, see the rejection of claim 2 above.

53.   With respect to claim 40, **the plurality of output signals corresponds to a first number**

of DDR memory devices arranged in the two or more ranks which are selectable by the

first number of chip-select signals and wherein the plurality of input signals corresponds to

a second number of DDR memory devices arranged in ranks which are selectable by the

second number of chip-select signals, wherein the memory module simulates a virtual

memory module having the second number of DDR memory devices (see paragraph 41; see

also Figures 6A and 6B, CLPD 604 input and output signals).

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54.   With respect to claim 46, **the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank** (see Figures 4A and 4B).

55.   Rejection of claims 21, proposed by Requesters 1 and 2, is **not adopted**. Requester 2 explains that Amidi teaches that since standard DDR memory modules have only one set of address lines, two sets of addresses must be provided to access certain types of cells and that Amidi's memory module stores the input signals to provide column address signals on a separate cycle from the row address signals citing paragraph 61. However, Requester 2 fails to explain how paragraph 61 teaches the actual limitation "wherein the configured to store an input signal of the set of input signal during a row access procedure for subsequent use during a column access procedure." The cited paragraph does not disclose that an input address signal stored during a row access procedure is retained for subsequent use during a column access procedure from the cited pages.

Ground 4

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56.   Requester 1 asserts that claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, and 51 are obvious over Amidi. Proposed rejection of claims 1-15, 18-20, 21, 23-25, 27-34, 36-43, 45-48, 50, and 51, is **adopted**.

57.   <u>Claims 1-15, 18-20, 23-25, 27-34, 36-43, 45-48, 50, and 51 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi.</u>

58.   With respect to claims 1-11, 14, 15, 18-25, 27-34, 36-45, 51 and 50 see the rejection of these claims as being anticipated by Amidi above. Because these claims are anticipated by Amidi, they are necessarily obvious over Amidi.

59.   With respect to claims 12, 13, and 48, see the rejection of claim 10 as being anticipated by Amidi above. Although Requester 1 does not address the requirement that the plurality of DDR memory devices comprise a plurality of DDR2 memory devices, substituting a known memory device with a faster memory device to achieve the predictable result of faster access speed would have been obvious to one skilled in the art at the time of the invention.

60.   With respect to claim 47, see the rejection of claim 10 above.

61.   Proposed rejection of claims 16, 17, and 21 is **not adopted**. With respect to claims 16, 17, Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication that the command signal may be transmitted to the DDR memory devices

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serially in a sequential fashion" without any reasoned explanation to support the assertion.

Conclusion of obviousness requires more that a mere conclusory statement.

62.   With respect to claim 21, the proposed rejection does not address the actual limitation of

the claim that requires storage of an input signal during a row access procedure for subsequent

use during a column access procedure.

Ground 5

63.   Requester 1 asserts that claims 1-51 are obvious over Amidi in view of Dell 2. Proposed

rejection of claims 1-15, 18-20, and 22-51 is **adopted**.

64.   Claims 1-15, 18-20, and 22-51 are rejected under 35 U.S.C. 103(a) as being as being

unpatentable over Amidi in view of Dell 2.

65.   With respect to claims 1-15, 18-21, 23-25, 27-34, 36-43, 45-48, 50, and 51, see the

rejection of these claims on ground 4 above.

66.   With respect to claim 22, **the command signal comprises a read command signal or a

write command signal** (read and write commands are inherent in any functioning memory

module), **the set of input signals comprises a density bit which is a row address bit** (the

specification describes the density bit simply as a row address bit that is latched during the

activate command for the selected bank, with no other attribute), **and the circuit is configured**

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to store the row address bit during an activate command for a selected bank (see Amidi,

Figure 6A, row address bits are stored in a register and an activate command to activate a row

requires row address bits).

67.   With respect to claim 26, **the logic element receives the bank address signals and the**

command signal from the computer system and the register receives the bank address

signals and the command signal from the computer system (see Amidi, Figure 6A, register

608).

68.   With respect to claim 35, the combination of Amidi and Dell 2 discloses a memory

module that controls four ranks of memory devices with control signals configured to control

two ranks of memory devices. A memory module that comprises four ranks of memory devices

and control signals configured to control two ranks comprises two ranks of memory devices and

control signals configured to control one rank.

69.   With respect to claim 44, see the rejection of claim 26 above.

70.   With respect to claim 49, **the plurality of input signals corresponds to a first memory**

density, and the plurality of output signals corresponds to a second memory density, the

second memory density greater than the first memory density (see Amidi, paragraph 41).

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71.   Proposed rejection of claims 16, 17, and 21 is **not adopted**. With respect to claims 16

and 17, see the discussion of these claims above.

72.   With respect to claim 21, Requester 1 points to c8:29-41 of Dell 2's specification that

teaches storing a re-mapped BA1 signal supplied at RAS time to re-send at CAS time. However,

Requester 1 does not make it clear how this teaching can be combined with Amidi to result in a

memory module of claim 21. Requester 1's proposed rejection provides mapping of teachings

from both Amidi and Dell 2 to different elements of claim 21, without providing any guidance as

to how the teachings from the two references are to be combined to result in a memory module

that discloses all of the limitations of claim 21. Amidi discloses a memory module that uses the

column address bit A11 to determine the active rank (see paragraph 57). Amidi does not appear

to use a signal supplied during a row access procedure. It is not clear how Dell 2's teaching of

retaining the re-mapped BA1 signal can be applied in Amidi's memory module. Bank address

signals are not re-mapped in Amidi's memory module.

Ground 6

73.   Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45,

and 50 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50, is **adopted**.

74.   Claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 are rejected

under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of JEDEC 21-C.

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75.   Because these claims are anticipated by Amidi, they are necessarily obvious over Amidi

in view of JEDEC 21-C. See ground 4 above.

76.   With respect to claims 10 and 11, spacing of memory devices is also an obvious matter of

design choice subject to constraints imposed by various practical engineering, manufacturing,

marketing, cost, and other considerations.

77.   Proposed rejection of claims 21 is **not adopted**. See the discussion of this claim above.

Ground 7

78.   The Examiner notes that Requester has failed to properly raise a substantial new question

of patentability based on Murocca and Dell 2 combination. Nevertheless, Requester's proposed

rejection based on Murdocca and Dell2 has been considered on the merit as discussed below.

79.   Requester 1 asserts that claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42, and 51 are

obvious over Murdocca and Dell 2. The proposed rejection is **not adopted**.

80.   Requester 1 identified Murdocca's 1-to-2 decoder, shown on page 250, as the logic

element that receives a set input control signals from the computer system, the set of input

control signals comprising at least one row/column address signal, bank address signal, and at

least one chip select signal. Requester asserts that it would have been obvious to combine the

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method for constructing larger RAMs from smaller RAMs disclosed in Murdocca with the logic

element disclose in Dell 2 that receives a number of address inputs and a number of bank address

signals. However, Requester fails to explain how the proposed combination would result in the

claimed logic element. For example, Requester does not explain how Murdocca's 1-to-2 decoder

that takes one address signal as input and a chip select signal as a control signal to produce two

output signals can accommodate bank address signals and how the output bank address signals

are used to construct the claimed circuit. A combination proposed cannot be just a patchwork of

different circuit elements that teach different limitations of the claim. In addition to containing

all of the limitations of the claim, the proposed combined circuit must make sense in terms of its

overall structure and function. It must work as a unit that comprises all of the claimed structural

features and be functional as a unit in the manner claimed.

81.   Moreover, all claims require a circuit that "responds to a first command signal and the set

of input control signals from the computer system by generating and transmitting a second

command signal and the set of output control signal to the plurality of memory devices."

Requester 1 asserts that Murdocca's teaching of a 1-to-2 decoder and Dell 2's disclosure at

c2:44-49 and c8:32-41 disclose the circuit. The 1-to-2 decoder taught by Murdocca is an address

decoder. It does not respond to a command. Nor does it generate any command. Dell 2's circuit

that remaps addresses does not respond to a command by generating another command as

required by the claims. Therefore, the proposed combination does not teach a circuit that

responds to a first command by generating and transmitting a second command as required by

the claims.

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Ground 8

82.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are anticipated by Dell 1. Proposed rejection is **not adopted**. Claims are anticipated when a single reference teaches all of the limitations of the claims. Requester 2's proposed rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C "establishes that a DIMM has a PLL mounted to the printed circuit board" (Request 2, p. 63). However, Requester 2 fails to explain where in Dell 1 a PLL is taught or how JEDEC 21-C's teaching of a PLL is attributable to Dell 1.

Ground 9

83.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are obvious over Dell 1 in view of JEDEC standards. Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **adopted**.

84.   <u>Claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Dell 1 in view of JEDEC 21-C.</u>

85.   With respect to claim 1, Dell 1 discloses **a memory module** (see Figure 3, DIMM with two banks of memory chips) **connectable to a computer system, the memory module comprising:**

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a printed circuit board (see c23-39, DIMMs for IBM PCs are implemented with PCBs;

see JEDE 21-C);

a plurality of memory devices mounted to the printed circuit board (see Figure 3,

4Mx4 chips 40x), the plurality of memory devices having a first number of memory devices

arranged in a first number of ranks (see Figure 3; see also c1:60-67, 36 devices in two banks);

a circuit mounted to the printed circuit board, the circuit comprising a logic element

and, the logic element receiving a set of input control signals (see Figure 3, the DIMM

receives RAS, CAS, OE, WE, and A0-A11 signals) from the computer system, the set of input

control signals comprising at least four address signals (A0-A11), the set of input control

signals corresponding to a second number of memory devices arranged in a second number

of ranks (see c1:46-53, 60-67, nine devices in one bank), the second number of memory

devices smaller than the first number of memory devices and the second number of ranks

less than the first number of ranks, the circuit generating a set of output control signals in

response to the set of input control signals (see Figure 3, the circuit generates two CA0, two

WE0, two OE0, RAS A, RAS B signals, and two sets of address signals A0-A10), the set of

output control signals corresponding to the first number of memory devices arranged in

the first number of ranks (the set of output control signals correspond to 36 4Mx4 devices

arranged in two banks), wherein the circuit further responds to a first command signal (CBR

refresh for one bank of 8Mx8 memory devices) and the set of input control signals from the

computer system by generating and transmitting a second command signal and the set of

output control signals to the plurality of memory devices (see c6:22-29, Dell 1 disclose

generating a CBR refresh command to both banks of 4Mx4 memory devices by activating two

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RAS signals), **the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks.**

86.   However, Dell 1 does not specifically disclose that 1) the memory devices are **double-data-rate (DDR)** devices, 2) the circuit comprises **a register**, 3) the address signals comprise at least **one row/column address signal, bank address signals, and at least one chip-select signal**, and 4) the memory module comprises **a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of memory devices, the logic element, and the register.** On the other hand, JECED 21-C discloses 1) the use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20-4-10; see also p. 4.20.4-18), 3) address signals that comprise at least one row/column signal (p. 4.20.4-10, input signal A0-A13 to register), bank address signals (BA0-BA1), at least one chip-select signal (S0), and 4) a phase-lock loop device mounted to the printed circuit board (p. 4.20.4-29) that is operatively coupled to other elements of the module (see p. 4.20.4-17).

87.   It would have been obvious to one of ordinary skill in the art, having the teachings of Dell 1 and JEDEC 21-C before him at the time the invention was made, to design the DIMM of Dell 1 in compliance with the JEDEC standard to make it compatible with computer systems that expect DIMMs installed in the system to be standard compliant.

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88.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip select signal lines; a set of input signals with four chip select signals comprise two chip select signals) **and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3, would generate four output signal lines, RS0-RS3).

89.   With respect to claim 4, **the first number of chip-select signals is two and the second number of chip-select signals is four** (see the discussion of claim 3 above).

90.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Dell 1, c4:28-29).

91.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (see the rejection of claim 1; the logic element of Dell 1 includes a circuit that receives input signals, thus in a DIMM that results from the combination, input signals received by the logic element would be buffered in registers as taught by JEDEC 21-C).

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92.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

93.   With respect to claim 9, **the register comprises a plurality of register devices** (see JEDEC 21-C, p. 4.20.4-18, Register 1 and Register 2).

94.   With respect to claims 15 and 28 see the discussion of claim 1 above.

95.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

96.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Dell 1, c6:28-30, CBR refresh command refreshes both banks concurrently).

97.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

98.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

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99.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Dell 1 and JEDEC), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an activate command to activate a row requires row address bits).

100.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit** (see Dell 1, c4:28-29)**, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.**

101.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see JEDEC 21-C, p. 4.20.4-10).

102.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

103.   With respect to claims 31 and 32, see the discussion of claim 3 above.

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104.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (see JEDEC, p. 4.20.4-10 and 4.20.4-7: JEDEC discloses registers that receive BA0-BA1 and RAS, CAS, and WE signals; JEDEC also discloses that RAS, CAS, and WE define the operation to be executed, i.e., command, by the SDRAM when sampled at the positive rising edge of the clock).

105.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Dell 1, c6:28-30).

106.   With respect to claim 37, although Dell 1 and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal,** they do disclose receiving input commands and generating output commands as claimed. One of ordinary skill in the art would realize that Dell 1's high density DIMM with RAS address re-mapping must work for all commands, not just the ones specifically mentioned in the disclosure.

107.   With respect to claim 38, Dell 1 and JEDEC 21-C discloses that **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.** See the discussion of claim 37 above.

108.   With respect to claim 39, see claims 1 and 3 above.

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109.   Proposed rejection of claims 21 is **not adopted**. Requester asserts that JEDEC 21-C "teaches that all input control signals to DIMM pass through the register, which stores them internally before re-driving them, including during a column access procedure" citing pages 40.20.4-67 and 40.20.4-11 (Request 2, pp. 242-243). However, Requester fails to explain how those pages teach the actual limitation "wherein the configured to store an input signal of the set of input signal during a row access procedure for subsequent use during a column access procedure." The Examiner cannot ascertain which input signal stored during a row access procedure is retained for subsequent use during a column access procedure from the cited pages.

Ground 10

110.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are anticipated by Wong. Proposed rejection is **not adopted**. Claims are anticipated when a single reference teaches all of the limitations of the claims. Requester's proposed rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C "explains that a DIMM has a PLL mounted to the printed circuit board" (Request, p. 674). However, Requester fails to explain where in Wong a PLL is taught or how JEDEC 21-C's teaching of a PLL is attributable to Wong.

Ground 11

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111.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are obvious over Wong in view of JEDEC standards. Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

112.   Claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Wong in view of JEDEC 21-C.

113.   With respect to claim 1, Wong discloses **a memory module** (see Figure 3, DIMM with two banks of memory chips) **connectable to a computer system, the memory module comprising:**

a printed circuit board (see Figure 3, 1000);

a plurality of memory devices mounted to the printed circuit board (Figure 3, 1002), **the plurality of memory devices having a first number of memory devices arranged in a first number of ranks** (1012 and 1012);

a circuit mounted to the printed circuit board, the circuit comprising a logic element and, the logic element receiving a set of input control signals (see Figures 4A and 4B) **from the computer system, the set of input control signals comprising at least** four address signals (A0-A13), **the set of input control signals corresponding to a second number of memory devices arranged in a second number of ranks** (see c2:1-10, Wong discloses that a separate bank of memory typically requires at minimum either a unique RAS or unique CAS for each bank; see Figure 4, the input signal set contains one RAS and one CAS, i.e., a set for a single bank), **the second number of memory devices smaller than the first number of memory**

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devices and the second number of ranks less than the first number of ranks, the circuit

generating a set of output control signals in response to the set of input control signals (see

Figure 4, the circuit generates two CAS, two WE, two RAS signals, and two sets of address

signals A0-A12), **the set of output control signals corresponding to the first number of**

memory devices arranged in the first number of ranks (the set of output control signals

correspond to 36 4Mx4 devices arranged in two banks), **wherein the circuit further responds**

to a first command signal and the set of input control signals from the computer system by

generating and transmitting a second command signal and the set of output control signals

to the plurality of memory devices (c2:30-34, CBR refresh for both banks), **the first command**

signal and the set of input control signals corresponding to the second number of ranks and

the second command signal and the set of output control signals corresponding to the first

number of ranks.

114.   However, Wong does not specifically disclose that 1) the memory devices are **double-**

data-rate (DDR) devices, 2) the circuit comprises **a register,** 3) the address signals comprise at

least **one row/column address signal, bank address signals, and at least one chip-select**

signal, and 4) the memory module comprises **a phase-lock loop device mounted to the printed**

circuit board, the phase-lock loop device operatively coupled to the plurality of memory

devices, the logic element, and the register. On the other hand, JECED 21-C discloses 1) the

use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20.4-

10; see also p. 4.20.4-18), 3) address signals that comprise at least one row/column signal (p.

4.20.4-10, input signal A0-A13 to register), bank address signals (BA0-BA1), at least one chip-

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select signal (S0), and 4) a phase-lock loop device mounted to the printed circuit board (p.

4.20.4-29) that is operatively coupled to other elements of the module (see p. 4.20.4-17).

115.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Wong and JEDEC 21-C before him at the time the invention was made, to design the DIMM of

Wong in compliance with the JEDEC standard to make it compatible with computer systems that

expect DIMMs installed in the system to be standard compliant.

116.   With respect to claim 3, **the set of input control signals comprises a first number of**

chip-select signals (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip

select signal lines; a set of input signals with four chip select signals comprise two chip select

signals) **and wherein the set of output control signals comprises a second number of chip-**

select signals greater than the first number of chip-select signals (see JEDEC 21-C, p. 4.20.4-

12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip

select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3,

would generate four output signal lines, RS0-RS3).

117.   With respect to claim 4, **the first number of chip-select signals is two and the second**

number of chip-select signals is four (see the discussion of claim 3 above).

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118.   With respect to claim 6, **the logic element comprises an application-specific**

integrated circuit, a field-programmable gate array, a custom-designed semiconductor

device, or a complex programmable-logic device (see Wong, c2:41-44).

119.   With respect to claim 7, **the bank address signals of the set of input control signals**

are received by both the logic element and the register (see the rejection of claim 1; the logic

element of Wong includes a circuit that receives input signals, thus in a DIMM that results from

the combination, input signals received by the logic element would be buffered in registers as

taught by JEDEC 21-C).

120.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and**

the logic element are portions of a single component (these are all portions of a single DIMM

which is a component of a personal computer).

121.   With respect to claim 9, **the register comprises a plurality of register devices** (see

JEDEC 21-C, p. 4.20.4-18, Register 1 and Register 2).

122.   With respect to claims 15 and 28 see the discussion of claim 1 above.

123.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

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124.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Wong, c3:30-34).

125.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

126.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

127.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Wong and JEDEC), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an activate command to activate a row requires row address bits).

128.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Wong, c2:41-42).

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129.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see JEDEC 21-C, p. 4.20.4-10).

130.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

131.   With respect to claims 31 and 32, see the discussion of claim 3 above.

132.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (see JEDEC, p. 4.20.4-10 and 4.20.4-7: JEDEC discloses registers that receive BA0-BA1 and RAS, CAS, and WE signals; JEDEC also discloses that RAS, CAS, and WE define the operation to be executed, i.e., command, by the SDRAM when sampled at the positive rising edge of the clock).

133.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Wong, c2:28-34).

134.   With respect to claim 37, although Wong and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal,** they do disclose receiving input commands and generating output commands

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as claimed. One of ordinary skill in the art would realize that Wong's memory expansion

module including multiple memory banks and a bank control circuit must work for all

commands, not just the ones specifically mentioned in the disclosure.

135.   With respect to claim 38, Wong and JEDEC 21-C discloses that **the input command**

signal is a read signal or a write signal and the output command signal is a read signal or a

write signal. See the discussion of claim 37 above.

136.   With respect to claim 39, see claims 1 and 3 above.

137.   Proposed rejection of claims 21 is **not adopted**. Requester asserts that JEDEC 21-C

"teaches that all input control signals to DIMM pass through the register, which stores them

internally before re-driving them, including during a column access procedure" citing pages

40.20.4-67 and 40.20.4-14 (Request, pp. 856-857). However, Requester fails to explain how

those pages teach the actual limitation "wherein the configured to store an input signal of the set

of input signal during a row access procedure for subsequent use during a column access

procedure." The Examiner cannot ascertain which input signal stored during a row access

procedure is retained for subsequent use during a column access procedure from the cited pages.

Ground 12

138.   Claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are rejected

under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connolly.

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139.   With respect to claim 1, Micron discloses **a memory module** (Figures 1-3) **connectable**

to a computer system, the memory module comprising:

a printed circuit board (see Figure 1);

a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted**

to the printed circuit board, the plurality of memory devices having a first number of

memory devices arranged in a first number of ranks (see Figure 4, the module has two

ranks);

a circuit mounted to the printed circuit board, the circuit comprising a logic element

and a register (p.4, Figure 4, Register U37 & U38), **the logic element receiving a set of input**

control signals (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #) **from the**

computer system, the set of input control signals comprising at least one row/column

address signal (A0-A12), bank address signals (BA0, BA1), and at least one chip select

signal (S0); and

a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,**

the phase-lock loop device operatively coupled to the plurality of memory devices, the logic

element, and the register.

140.   However, Micron does not specifically disclose that "the set of input control signals

corresponding to a second number of memory devices arranged in a second number of ranks, the

second number of memory devices smaller than the first number of memory devices and the

second number of ranks less than the first number of ranks, the circuit generating a set of output

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control signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of ranks,

wherein the circuit further responds to a first command signal and the set of input control signals

from the computer system by generating and transmitting a second command signal and the set

of output control signals to the plurality of memory devices, the first command signal and the set

of input control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks."

141.   On the other hand, Connolly discloses a DIMM that receives a set of input control signals

(Figure 3, RAS, CAS, OE, WE, A0-A11), **the set of input control signals corresponding to a**

second number of memory devices arranged in a second number of ranks (see Figure 2,

there are nine devices in one rank), **the second number of memory devices smaller than the**

first number of memory devices and the second number of ranks less than the first number

of ranks (see Figure 3, there are 36 devices in two ranks), **the circuit generating a set of output**

control signals in response to the set of input control signals (see Figure 3, the circuit

generates two CA0, two WE0, two OE0, RAS A, RAS B signals, and two sets of address signals

A0-A10), **the set of output control signals corresponding to the first number of memory**

devices arranged in the first number of ranks(the set of output control signals correspond to

36 4Mx4 devices arranged in two banks), **wherein the circuit further responds to a first**

command signal (CBR refresh for one bank of 8Mx8 memory devices) **and the set of input**

control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices

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(see c6:46-49, Connolly discloses generating a CBR refresh command to both banks of 4Mx4 memory devices by activating two RAS signals), **the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks.**

142.   It would have been obvious to one of ordinary skill in the art, having the teachings of Micron and Connolly before him at the time the invention was made, to modify the design the DIMM of Micron to incorporate Connolly's technique for converting system signals from one address configuration to a different address configuration, to be able to use lower capacity memory devices which can be much cheaper (see Connolly, c1:38-63).

143.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see Micron, Figure 4, register input signal S0) **and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals** (register output signals S0 and S1).

144.   With respect to claim 4, Micron and Connolly do not specifically disclose that **the first number of chip-select signals is two and the second number of chip-select signals is four.** However, it would have been obvious to one of ordinary skill in the art to add two additional chip select signals to design a module with more memory banks in order to increase the memory capacity of the module.

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145.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Connolly, Figure 4, ASIC LOGIC 46).

146.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (see the rejection of claim 1; the logic element of Micron includes a circuit that receives the input signals; the Examiner also notes that the claim does not preclude the logic element from comprising a register).

147.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

148.   With respect to claim 9, **the register comprises a plurality of register devices** (Micron Figure 4, U37 & U38).

149.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board** (Micron, Figure 7, U1-U10; see also Figure 8, U1-U6), **a second set of DDR memory devices on the first side of the printed circuit board** (Figure 7, U11-U18; Figure 8., U7-U12), **a third set of DDR memory devices on a second side of the printed circuit board** (Figure 7, U19-U28; Figure 8, U21-U26), **and a fourth set of DDR memory devices on the second side of the printed**

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circuit board (Figure 7, U29, U36; Figure 8, U28-U33), **the DDR memory devices of the**

second set spaced from the DDR memory devices of the first set, the DDR memory devices

of the fourth set spaced from the DDR memory devices of the third set (see Figure 7 and 8).

150.   With respect to claim 11, **the DDR memory devices of the second set are spaced from**

the DDR memory devices of the first set in a direction along the first side and the memory

devices of the fourth set are spaced from the memory devices of the third set in a direction

along the second side (see Figure 7 and 8).

151.   With respect to claims 15 and 28 see the discussion of claim 1 above.

152.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

153.   With respect to claim 18, **the command signal is transmitted to two ranks of the first**

number of ranks at a time (see Connolly, c6:46-49, CBR refresh command refreshes both

banks concurrently).

154.   With respect to claim 19, **the command signal comprises a refresh command signal**

(see the discussion of claim 18 above).

155.   With respect to claim 20, **the command signal is transmitted to the two ranks of the**

first number of ranks concurrently (see claim 18 above).

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156.   With respect to claim 21, **the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure** (see Connolly, Figure 7, SYS RAS signal stored in 90 is used to generate CAS L and CAS R).

157.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Micron and Connolly; see also Micron Table 6), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (Micron, Figure 4, row address bits are stored in a register and an activate command to activate a row requires row address bits).

158.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit** (Connolly, Figure 4), **a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.**

159.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (Micron, Figure 4).

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160.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

161.   With respect to claims 31 and 32, see the discussion of claim 3 above.

162.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (Micron, Figure 4).

163.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Connolly, c6:46-49).

164.   With respect to claim 37, **the input command signal is a precharge signal and the output command signal is a precharge signal** (Micron, Table 6).

165.   With respect to claim 38, **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal** (Micron, Table 6).

166.   With respect to claim 39, see claims 1 and 3 above.

Ground 13

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167.   Requester 3 asserts that claims 1, 3-4, 6-1, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are obvious over Micron in view of Amidi. Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

168.   Claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Amidi.

169.   With respect to claim 1, Micron discloses **a memory module (Figures 1-3) connectable to a computer system, the memory module comprising:**

   a printed circuit board (see Figure 1);

   a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted to the printed circuit board, the plurality of memory devices having a first number of memory devices arranged in a first number of ranks** (see Figure 4, the module has two ranks);

   a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register (p.4, Figure 4, Register U37 & U38), **the logic element receiving a set of input control signals** (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #) **from the computer system, the set of input control signals comprising at least one row/column address signal (A0-A12), bank address signals (BA0, BA1), and at least one chip select signal (S0); and**

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a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,**

the phase-lock loop device operatively coupled to the plurality of memory devices, the logic

element, and the register.

170.   However, Micron does not specifically disclose that "the set of input control signals

corresponding to a second number of memory devices arranged in a second number of ranks, the

second number of memory devices smaller than the first number of memory devices and the

second number of ranks less than the first number of ranks, the circuit generating a set of output

control signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of ranks,

wherein the circuit further responds to a first command signal and the set of input control signals

from the computer system by generating and transmitting a second command signal and the set

of output control signals to the plurality of memory devices, the first command signal and the set

of input control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks."

171.   On the other hand, Amidi discloses a DIMM that receives a set of input control signals

(see Figure 6, the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and signals),

the set of input control signals comprising at least one row/column address signal

(Add[n:0]), bank address signals (BA[1:0]), and at least one chip select signal (cs0), the set

of input control signals corresponding to a second number of memory devices arranged in

a second number of ranks, the second number of memory devices smaller than the first

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number of memory devices and the second number of ranks less than the first number of

ranks (see paragraphs 10-12, Amidi's invention is a transparent four rank module fitting into a

memory socket meant for a two rank module), **the circuit generating a set of output control**

signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of

ranks, wherein the circuit further responds to a first command signal and the set of input

control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices,

the first command signal and the set of input control signals corresponding to the second

number of ranks and the second command signal and the set of output control signals

corresponding to the first number of ranks (see Figure 6 and paragraph 52, "CPLD also

ensures that all commands for a two rank memory module conveyed by the module connector

602 are also performed on the four rank memory modules. For example, CPLD 604 generates

rsc2 and rcs3 …").

172.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Micron and Amidi before him at the time the invention was made, to modify the design the

DIMM of Micron to adopt Amidi's transparent four rank memory module for standard two rank

sub-system teachings to be able to use lower capacity memory devices which can be much

cheaper (Amidi, p. 1, paragraph 8).

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173.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see Amidi, Figure 4, cs0 and cs1) **and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals** (rcs0a-rcs3a).

174.   With respect to claim 4, **the first number of chip-select signals is two and the second number of chip-select signals is four** (see the discussion of claim 3 above).

175.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Amidi, Figure 6, CPLD).

176.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (see Amidi, Figure 6, the claim does not preclude the logic element that comprises the CLPD and the register).

177.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

178.   With respect to claim 9, **the register comprises a plurality of register devices** (Amidi, Figure 8, 820, 822, 828, 830).

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179.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board** (Amidi, Figure 4A, ranks 0 and 2 are on the front side), **a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board** (Figure 4B, ranks 1 and 3 are on the back side), **the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set** (this is inherent as two physical devices cannot occupy the same space at the same time).   Micron discloses this limitation as well. See the discussion of claim 10 above.

180.   With respect to claim 11, **the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side** (see Amidi, paragraph 34, the devices are stacked on the front and the back side; see also Micron, Figures 7 and 8).

181.   With respect to claims 15 and 28 see the discussion of claim 1 above.

182.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

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183.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Amidi, Figure 6 and paragraph 52).

184.   With respect to claim 19, **the command signal comprises a refresh command signal** (see Amidi, paragraph 52).

185.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

186.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see Amidi, Figure 6, register).

187.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Amidi, Figure 6, CPLD).

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189.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see Amidi, Figure 6).

190.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

191.   With respect to claims 31 and 32, see the discussion of claim 3 above.

192.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (see Amidi, Figure 6).

193.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Amidi, paragraph 52).

194.   With respect to claim 37, **the input command signal is a precharge signal and the output command signal is a precharge signal** (Amidi, paragraph 52).

195.   With respect to claim 38, **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.** See the discussion of claim 37 above.

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196.   With respect to claim 39, see claims 1 and 3 above.

197.   Proposed rejection of claims 21 is **not adopted**. Requester cites Table 6 of Micron and

paragraph 61 of Amidi, without any explanation as to how the cited passages disclose the

limitation "wherein the configured to store an input signal of the set of input signal during a row

access procedure for subsequent use during a column access procedure." The cited passages do

not disclose that an input address signal stored during a row access procedure is retained for

subsequent use during a column access procedure from the cited pages. Requester asserts that

one of ordinary skill in the art would have known how to select and store needed inputs for later

use. However, requester fails to explain which "input signal from a row access procedure that

would be needed in - but would otherwise be unavailable during - subsequent column access

procedure" would be saved for later use.

Examiner's Statement of Reasons for Patentability/Confirmation

198.   Claim 21 is deemed to be patentable and/or confirmed over the prior art of record for the

following reasons: As discussed above, none of the combinations proposed by Requester teaches

the limitation that requires a set of pins that receives a sense command that is separate from a set

of pins that receives a write command.

Submissions

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199.   In order to ensure full consideration of any amendments, affidavits or declarations, or

other documents as evidence of patentability, such documents must be submitted in response to

this Office action. Submissions after the next Office action, which is intended to be an Action

Closing Prosecution (ACP), will be governed by 37 CFR 1.116(b) and (d), which will be strictly

enforced.

Extensions of Time

200.   Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes*

reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant"

and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c)

requires that *inter partes* reexamination proceedings "will be conducted with special dispatch"

(37 CFR 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are

provided for in 37 CFR 1.956. Extensions of time are not available for third party requester

comments, because a comment period of 30 days from service of patent owner's response is set

by statute. 35 U.S.C. 314(b)(3).

Service of Papers

201.   Any paper filed with the USPTO, i.e., any submission made, by either the Patent Owner

or the Third Party .Requester must be served on every other party in the reexamination

proceeding, including any other third party requester that is part of the proceeding due to merger

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Art Unit: 3992

of the reexamination proceedings. As proof of service, the party submitting the paper to the

Office must attach a Certificate of Service to the paper, which sets forth the name and address of

the party served and the method of service. Papers filed without the required Certificate of

Service may be denied consideration. 37 CFR 1.903; MPEP 2666.06.

Amendment in Reexamination Proceedings

202.   Any proposed amendment to the specification and/or claims in this reexamination

proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37

CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). Amendments in an

inter partes reexamination proceeding are made in the same manner that amendments in an

exparte reexamination are made. MPEP 2666.01. See MPEP 2250 for guidance as to the manner

of making amendments in a reexamination proceeding.

Notification of Concurrent Proceedings

203.   The patent owner is reminded of the continuing responsibility under 37 CFR 1.985(a), to

apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the

patent undergoing reexamination or any related patent throughout the course of this

reexamination proceeding. The third party requester is also reminded of the ability to similarly

inform the Office of any such activity or proceeding throughout the course of this reexamination

proceeding. See MPEP § 2686 and 2686.04.

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All correspondence relating to this *inter partes* reexamination proceeding should be directed as follows:

By U.S. Postal Service Mail to:

Mail Stop *Ex Parte* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building
401 Dulany St.
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/Woo H. Choi/

Woo H. Choi
Primary Examiner
Central Reexamination Unit 3992

NETL.018RX1 / NETL.018RX6 / NETL.018RX7   PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee	: Bhakta et al.	
Inter Partes Reexamination No.	: 95/000,578; 95/000,579; 95/001,339	
Filing Date	: October 20, 2010; October 21, 2010; June 8, 2010	
For	: MEMORY MODULE DECODER	
Group Art Unit	: 3992	
Confirmation No.	: 8810; 3547; 5035	

RESPONSE TO OFFICE ACTION IN *INTER PARTES* REEXAMINATION COMMUNICATION MAILED APRIL 4, 2011

Mail Stop Inter Partes Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The owner ("Patent Owner") of U.S. Patent No. 7,619,912 ("the '912 patent") submits herein remarks in response to the Office Action mailed April 4, 2011 ("the Office Action") in the above-captioned merged *inter partes* reexamination proceedings. The owner hereby requests reconsideration by the Examiner.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Claim Status and Support for New and Amended Claims are set forth on pages separate from the pages containing changes to the claims, beginning at page 21 of this paper.

Remarks begin on page 34 of this paper.

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Filing Date   : October 20, 2010; October 21, 2010; June 8, 2010

AMENDMENTS TO THE CLAIMS

Please add new Claims 52-118. Claims 1-51 remain as originally issued.

1.   (Original)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

2.   (Original)   The memory module of claim 1, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

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Filing Date   : October 20, 2010; October 21, 2010; June 8, 2010

3.   (Original)   The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4.   (Original)   The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5.   (Original)   The memory module of claim 1, wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column address signals to the plurality of DDR memory devices during a subsequent column access procedure.

6.   (Original)   The memory module of claim 1, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

7.   (Original)   The memory module of claim 1, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8.   (Original)   The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9.   (Original)   The memory module of claim 1, wherein the register comprises a plurality of register devices.

10.   (Original)   The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11.   (Original)   The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

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12.   (Original)   The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

13.   (Original)   The memory module of claim 12, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

14.   (Original)   The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

15.   (Original)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

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a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

16.   (Original)   The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

17.   (Original)   The memory module of claim 16, wherein the command signal comprises a read command signal.

18.   (Original)   The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19.   (Original)   The memory module of claim 18, wherein the command signal comprises a refresh command signal.

20.   (Original)   The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21.   (Original)   The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

22.   (Original)   The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

23.   (Original)   The memory module of claim 15, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure and to transmit the stored input signal as an output signal of the set of output signals during a subsequent column access procedure.

24.   (Original)   The memory module of claim 15, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

25.   (Original)   The memory module of claim 15, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

26.   (Original)   The memory module of claim 25, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

27.   (Original)   The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28.   (Original)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register.

29.   (Original)   The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

30.   (Original)   The memory module of claim 29, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

31.   (Original)   The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

32.   (Original)   The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

33.   (Original)   The memory module of claim 28, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

34.   (Original)   The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35.   (Original)   The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36.   (Original)   The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37.   (Original)   The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38.   (Original)   The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39.   (Original)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-

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lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank.

40.   (Original)   The memory module of claim 39, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

41.   (Original)   The memory module of claim 39, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

42.   (Original)   The memory module of claim 39, wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices.

43.   (Original)   The memory module of claim 42, wherein the logic element receives the second number of chip-select signals.

44.   (Original)   The memory module of claim 43, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

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45.   (Original)   The memory module of claim 39, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

46.   (Original)   The memory module of claim 39, wherein the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank.

47.   (Original)   The memory module of claim 39, wherein the DDR memory devices of the second rank are spaced from the DDR memory devices of the first rank in a direction along the first side.

48.   (Original)   The memory module of claim 39, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of the printed circuit board.

49.   (Original)   The memory module of claim 39, wherein the plurality of input signals corresponds to a first memory density, and the plurality of output signals corresponds to a second memory density, the second memory density greater than the first memory density.

50.   (Original)   The memory module of claim 39, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.

51.   (Original)   The memory module of claim 39, wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

52.   (New)   The memory module of claim 1, wherein the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated

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by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

53.   (New)   The memory module of claim 52, wherein the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR memory devices, the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register.

54.   (New)   The memory module of claim 53, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation, wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device.

55.   (New)   The memory module of claim 54, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

56.   (New)   The memory module of claim 54, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

57.   (New)   The memory module of claim 1, wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

58.   (New)   The memory module of claim 57, wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory devices, and the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.

59.   (New)   The memory module of claim 58, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

60.   (New)   The memory module of claim 58, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

61.   (New)   The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row

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address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

62.   (New)   The memory module of claim 61, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

63.   (New)   The memory module of claim 62, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

64.   (New)   The memory module of claim 1, wherein the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

65.   (New)   The memory module of claim 1, wherein the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries.

66.   (New)   The memory module of claim 1, wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals.

67.   (New)   The memory module of claim 1, wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

68.   (New)   The memory module of claim 67, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device, wherein the memory module is operable for use in a server system.

69.   (New)   The memory module of claim 67, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

70.   (New)   The memory module of claim 67, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

71.   (New)   The memory module of claim 67, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

72.   (New)   The memory module of claim 1, wherein the logic element is responsive at least in part to a first set of values of at least one address bit and the at least one chip-select signal of the set of input control signals by generating rank-selecting signals of the set of output control signals that select none of the first number of ranks for activation, and the logic element is further responsive at least in part to a second set of values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select two ranks of the first number of ranks for activation.

73.   (New)   The memory module of claim 72, wherein the logic element is further responsive at least in part to values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for activation, and the logic element is further responsive at least in part to the values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for read or write access.

74.   (New)   The memory module of claim 73, wherein the at least one address bit comprises a row address bit and a bank address bit.

75.   (New)   The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory

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(DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

76.   (New)   The memory module of claim 75, wherein the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages.

77.   (New)   The memory module of claim 15, wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input signals by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals.

78.   (New)   The memory module of claim 77, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

79.   (New)   The memory module of claim 77, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device.

80.   (New)   The memory module of claim 15, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

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81.   (New)   The memory module of claim 80, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

82.   (New)   The memory module of claim 28, wherein the logic element is responsive at least in part to the bank address signals and the chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

83.   (New)   The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

84.   (New)   The memory module of claim 82, wherein the plurality of DDR DRAM devices and the logic element are timed to clock signals from the phase-lock loop device.

85.   (New)   The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices.

86.   (New)   The memory module of claim 85, wherein the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank and the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has.

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87.   (New)   The memory module of claim 39, wherein the logic element is responsive at least in part to the bank address signals and the second number of chip-select signals of the plurality of input signals by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the set of input signals.

88.   (New)   The memory module of claim 87, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

89.   (New)   The memory module of claim 87, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device.

90.   (New)   The memory module of claim 39, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

91.   (New)   The memory module of claim 90, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

92.   (New)   The memory module of claim 1, wherein the set of input control signals includes row/column address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to row/column address bits (A_0 - A_n), wherein the logic element operates in response at least in part to row/column address bit A_{n+1} and does not operate in response to the row/column address bits (A_0 - A_n), and the register operates in response at least in

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part to the row/column address bits (A_0 - A_n) and does not operate in response to the row/column address bit A_{n+1}.

93.   (New)   The memory module of claim 39, wherein the set of input signals includes address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to address bits (A_0 - A_n), wherein the logic element operates in response at least in part to address bit A_{n+1} and does not operate in response to the address bits (A_0 - A_n), and the register operates in response at least in part to the address bits (A_0 - A_n) and does not operate in response to the address bit A_{n+1}.

94.   (New)   The memory module of Claim 1, wherein the logic element receives a bit of a non-bank address signal of the set of input control signals in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command.

95.   (New)   The memory module of Claim 94, wherein the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the rank-selecting signals for a subsequent read or write command.

96.   (New)   The memory module of Claim 15, wherein the logic element receives a bit of a non-bank address signal of the set of input signals in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command.

97.   (New)   The memory module of Claim 96, wherein the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the rank-selecting signals for a subsequent read or write command.

98.   (New)   The memory module of Claim 28, wherein the logic element receives a bit of a non-bank address signal of the set of input control signals in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command.

99.   (New)   The memory module of Claim 98, wherein the logic element further receives the bank address signals in conjunction with the activate command and uses the

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bank address signals to generate the rank-selecting signals during a subsequent read or write command.

100. (New)   The memory module of Claim 39, wherein the logic element receives a bit of a non-bank address signals of the plurality of input signals in conjunction with an activate command and uses the bit to generate the first number of chip-select signals for a subsequent read or write command.

101. (New)   The memory module of Claim 100, wherein the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the first number of chip-select signals for a subsequent read or write command.

102. (New)   The memory module of claim 28, wherein the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR DRAM devices of the plurality of DDR DRAM devices.

103. (New)   The memory module of claim 39, wherein the logic element comprises means for generating the chip-select signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

104. (New)   The memory module of claim 28, wherein the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR DRAM device boundaries.

105. (New)   The memory module of claim 39, wherein the logic element comprises means for generating the chip-select signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries.

106. (New)   The memory module of claim 1, wherein the logic element comprises means for using at least one address bit received by the memory module during an activate command operation to generate chip-select signals for a read or write command operation, the read or write command operation subsequent to the activate command operation.

107. (New)   The memory module of claim 28, wherein the logic element comprises means for using at least one address bit received by the memory module during an activate command operation to generate rank-selecting signals of the set of output control signals

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for a read or write command operation, the read or write command operation subsequent to the activate command operation.

108.   (New)   The memory module of claim 39, wherein the logic element comprises means for using at least one address bit received by the memory module during an activate command operation to generate the chip-select signals for a read or write command operation, the read or write command operation subsequent to the activate command operation.

109.   (New)   The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

110.   (New)   The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

111.   (New)   The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

112.   (New)   The memory module of claim 1, wherein the logic element comprises means for performing sequential and combinatorial logic procedures to generate rank-selecting signals of the set of output control signals.

113.   (New)   The memory module of claim 28, wherein the logic element comprises means for performing sequential and combinatorial logic procedures to generate rank-selecting signals of the set of output control signals.

114.   (New)   The memory module of claim 39, wherein the logic element comprises means for performing sequential and combinatorial logic procedures to generate the chip-select signals.

115.   (New)   The memory module of claim 1, wherein the first command signal is a row access command signal, and the logic element uses sequential and combinatorial logic procedures with at least one address bit of the set of input control signals and the at least one chip-select signal to generate chip-select signals for the second command signal.

116.   (New)   The memory module of claim 115, wherein the logic element further uses the sequential and combinatorial logic procedures with the at least one address bit to generate chip-select signals for a column access command signal subsequent to the row access

command signal, wherein the memory module receives a second column access command signal between receiving the row access command signal and the subsequent column access command signal.

117.   (New)   The memory module of claim 28, wherein the input command signal is a row access command signal, and the logic element uses sequential and combinatorial logic procedures with at least one address bit of the set of input signals and the chip-select signal to generate a chip-select signal for the output command signal.

118.   (New)   The memory module of claim 117, wherein the logic element further uses the sequential and combinatorial logic procedures with the at least one address bit to generate a chip-select signal for a column access command signal subsequent to the row access command signal, wherein the memory module receives a second column access command signal between receiving the row access command signal and the subsequent column access command signal.

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CLAIMS STATUS AND SUPPORT FOR NEW AND AMENDED CLAIMS

CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
1-51	Pending	
52	Pending	"the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals"; col. 6, ll. 55-63; col. 7, ll. 23-28, 46-50; col. 7, l. 55 – col. 8, l. 43; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 64 – col. 23, l. 25; Figs. 1A, 1B, 3A, 3B.
		"the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks"; col. 6, l. 64 – col. 7, l. 53; Figs. 1A, 1B, 3A, 3B.
53	Pending	"the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR memory devices"; col. 5, ll. 31-36; Figs. 1A, 1B.
		"the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register"; col. 5, ll. 28-31; Figs. 1A, 1B.
54	Pending	"the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation"; col. 7, ll. 50-51; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
		"the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device"; Figs. 1A, 1B.
		"the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device"; Figs. 1A, 1B.
55	Pending	"the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device"; col. 6, ll. 39-43.
		"the logic element transmitting the generated first number of chip-

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices"; Figs. 1A, 1B, 3A, 3B.
56	Pending	"the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.
		"the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
57	Pending	"operation of the register is responsive at least in part to clock signals received from the phase-lock loop device"; col. 5, ll. 28-31; Figs. 1A, 1B.
		"the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device"; col. 5, ll. 28-31; Figs. 1A, 1B.
		"the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks"; col. 6, l. 64 – col. 7, l. 53; Figs. 1A, 1B, 3A, 3B.
58	Pending	"the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register"; col. 5, ll. 31-36; col. 7, ll. 50-51; Figs. 1A, 1B, 3A, 3B.
		"the register transmitting the buffered bank address signals to the plurality of DDR memory devices"; col. 5, ll. 31-36; Figs. 1A, 1B.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		"the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals"; col. 6, ll. 55-63; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 50 – col. 23, l. 25; Figs. 1A, 1B, 3A, 3B.
59	Pending	"the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device"; col. 6, ll. 39-43.
		"the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices"; Figs. 1A, 1B, 3A, 3B.
60	Pending	"the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.
		"the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
61	Pending	"the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		"the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
62	Pending	"the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank"; col. 10, ll. 30-45.
63	Pending	"the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has"; col. 10, ll. 30-45.
64	Pending	"the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices"; col. 2, ll. 36-38; col. 3, ll. 54-60; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, l. 47 – col. 24, l. 12; Figs. 4B, 5.
65	Pending	"the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries"; col. 2, ll. 36-38; col. 14, ll. 12-14; col. 17, l. 28 – col. 19, l. 52.
66	Pending	"the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals"; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, ll. 6-25; Figs. 3A, 3B.
67	Pending	"the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"; col. 2, ll. 36-38; col. 17, l. 28 – col.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		19, l. 52; col. 22, ll. 50-63; col. 23, ll. 6-25; col. 24, ll. 1-5; Figs. 1A, 3A, 3B.
68	Pending	"the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device"; col. 5, ll. 27-31; Figs. 1A, 1B.
		"the memory module is operable for use in a server system"; col. 1, ll. 28-31; col. 2, ll. 10-12.
69	Pending	"the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices"; col. 3, ll. 54-60; col. 23, l. 47 – col. 24, l. 12; Figs. 4B, 5.
70	Pending	"the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries"; col. 14, ll. 12-14.
71	Pending	"the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation"; col. 2, ll. 36-38; col. 7, ll. 50-51; col. 17, l. 28 – col. 29, l. 52; Figs. 1A, 1B, 3A, 3B.
72	Pending	"the logic element is responsive at least in part to a first set of values of at least one address bit and the at least one chip-select signal of the set of input control signals by generating rank-selecting signals of the set of output control signals that select none of the first number of ranks for activation"; col. 2, ll. 36-38; col. 7, l. 55 – col. 8, l. 60.
		"the logic element is further responsive at least in part to a second set of values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select two ranks of the first number of ranks for activation"; col. 7, l. 55 – col. 8, l. 60.
73	Pending	"the logic element is further responsive at least in part to values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for activation, and the logic element is further responsive at least in part to the value of the at least one address bit and the at least one

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for read or write access"; col. 2, ll. 36-38; col. 7, l. 55 – col. 8, l. 60; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
74	Pending	"the at least one address bit comprises a row address bit and a bank address bit"; col. 6, ll. 55-63; col. 7, ll. 39-53; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-57; Figs. 1A, 3A, 3B.
75	Pending	"each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width"; col. 6, ll. 12-24; col. 12, ll. 26-29.
		"each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank"; col. 2, ll. 16-22; col. 5, ll. 60-64.
		"the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
76	Pending	"the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages"; col. 12, ll. 26-29.
77	Pending	"the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input signals"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, ll. 6-25; col. 24, ll. 1-5; Figs. 1A, 3A, 3B.
78	Pending	"the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries"; col. 14, ll. 12-14.
79	Pending	"the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device"; col. 5, ll. 27-31; Figs. 1A, 1B.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
80	Pending	"the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.
		"the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
81	Pending	"the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank"; col. 10, ll. 30-45.
		"the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has"; col. 10, ll. 30-45.
82	Pending	"the logic element is responsive at least in part to the bank address signals and the chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, ll. 6-25; col. 24, ll. 1-5; Figs. 1A, 3A, 3B.
83	Pending	"the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM memory device boundaries"; col. 14, ll. 12-14.
84	Pending	"the plurality of DDR DRAM devices and the logic element are timed to clock signals from the phase-lock loop device"; col. 5, ll. 27-31; Figs. 1A, 1B.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
85	Pending	"the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.
		"the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
86	Pending	"the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank"; col. 10, ll. 30-45.
		"the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has"; col. 10, ll. 30-45.
87	Pending	"the logic element is responsive at least in part to the bank address signals and the second number of chip-select signals of the plurality of input signals by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the set of input signals"; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, ll. 6-25; col. 24, ll. 1-5; Figs. 1A, 3A, 3B.
88	Pending	"the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries"; col. 14, ll. 12-14.
89	Pending	"the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device"; col. 5, ll. 27-31; Figs. 1A, 1B.

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
90	Pending	"the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank"; col. 9, ll. 27-32; col. 10, ll. 59-63.
		"the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"; col. 9, ll. 24-28, 32-34; col. 10, ll. 63-65.
		"the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices"; col. 10, l. 31-55; col. 10, l. 65 – col. 11, l. 4; col. 11, ll. 36-38.
91	Pending	"the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank"; col. 10, ll. 30-45.
		"the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has"; col. 10, ll. 30-45.
92	Pending	"the set of input control signals includes row/column address bits $(A_0 - A_{n+1})$"; col. 7, ll. 39-41; Figs. 1A, 1B.
		"the DDR memory devices are responsive at least in part to row/column address bits $(A_0 - A_n)$"; Figs. 1A, 1B.
		"the logic element operates in response at least in part to row/column address bit A_{n+1} and does not operate in response to the row/column address bits $(A_0 - A_n)$"; col. 7, l. 55 – col. 8, l. 64; Figs. 1A, 1B.
		"the register operates in response at least in part to the row/column address bits $(A_0 - A_n)$ and does not operate in response to the row/column address bit A_{n+1}"; col. 7, ll. 43-46; Figs. 1A, 1B.
93	Pending	"the set of input signals includes address bits $(A_0 - A_{n+1})$"; col. 7,

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		ll. 39-41; Figs. 1A, 1B.
		"the DDR memory devices are responsive at least in part to address bits $(A_0 - A_n)$"; Figs. 1A, 1B.
		"the logic element operates in response at least in part to address bit A_{n+1} and does not operate in response to the address bits $(A_0 - A_n)$"; col. 7, l. 55 – col. 8, l. 64; Figs. 1A, 1B.
		"the register operates in response at least in part to the address bits $(A_0 - A_n)$ and does not operate in response to the address bit A_{n+1}"; col. 7, ll. 43-46; Figs. 1A, 1B.
94	Pending	"the logic element receives a bit of a non-bank address signal of the set of input control signals in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 9, ll. 18-21; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
95	Pending	"the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
96	Pending	"the logic element receives a bit of a non-bank address signal of the set of input siganls in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 9, ll. 18-21; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
97	Pending	"the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
98	Pending	"the logic element receives a bit of a non-bank address signal of the set of input control signals in conjunction with an activate command and uses the bit to generate rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 9, ll. 18-21; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
99	Pending	"the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the rank-selecting signals for a subsequent read or write command"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52;

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		Figs. 1A, 1B, 3A, 3B.
100	Pending	"the logic element receives a bit of a non-bank address signals of the plurality of input signals in conjunction with an activate command and uses the bit to generate the first number of chip-select signals for a subsequent read or write command"; col. 9, ll. 18-21; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
101	Pending	"the logic element further receives the bank address signals in conjunction with the activate command and uses the bank address signals to generate the first number of chip-select signals for a subsequent read or write command"; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
102	Pending	"the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR DRAM devices of the plurality of DDR DRAM devices"; col. 2, ll. 36-38; col. 3, ll. 54-60; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, l. 47 – col. 24, l. 12; Figs. 4B, 5.
103	Pending	"the logic element comprises means for generating the chip-select signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices"; col. 3, ll. 54-60; col. 17, l. 28 – col. 19, l. 52; col. 22, ll. 50-63; col. 23, l. 47 – col. 24, l. 12; Figs. 4B, 5.
104	Pending	"the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR DRAM device boundaries"; col. 2, ll. 36-38; col. 14, ll. 12-14; col. 17, l. 28 – col. 19, l. 52.
105	Pending	"the logic element comprises means for generating the chip-select signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries"; col. 14, ll. 12-14; col. 17, l. 28 – col. 19, l. 52.
106	Pending	"the logic element comprises means for using at least one address bit received by the memory module during an activate command operation to generate chip-select signals for a read or write command operation, the read or write command operation subsequent to the activate command operation"; col. 7, ll. 50-51; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
107	Pending	"the logic element comprises means for using at least one address

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		bit received by the memory module during an activate command operation to generate rank-selecting signals of the set of output control signals for a read or write command operation, the read or write command operation subsequent to the activate command operation"; col. 2, ll. 36-38; col. 7, ll. 50-51; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
108	Pending	"the logic element comprises means for using at least one address bit received by the memory module during an activate command operation to generate the chip-select signals for a read or write command operation, the read or write command operation subsequent to the activate command operation"; col. 7, ll. 50-51; col. 17, l. 28 – col. 19, l. 52; Figs. 1A, 1B, 3A, 3B.
109	Pending	"the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices"; col. 9, ll. 22-34; col. 10, l. 31 – col. 11, l. 4; col. 11, ll. 36-38.
110	Pending	"the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR DRAM devices"; col. 9, ll. 12-34; col. 10, l. 31 – col. 11, l. 4; col. 11, ll. 36-38.
111	Pending	"the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices"; col. 9, ll. 12-34; col. 10, l. 31 – col. 11, l. 4; col. 11, ll. 36-38.
112	Pending	"the logic element comprises means for performing sequential and combinatorial logic procedures to generate rank-selecting signals of the set of output control signals"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 15 – col. 23, l. 25; Figs. 3A, 3B.
113	Pending	"the logic element comprises means for performing sequential and combinatorial logic procedures to generate rank-selecting signals of the set of output control signals"; col. 2, ll. 36-38; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 15 – col. 23, l. 25; Figs. 3A, 3B.
114	Pending	"the logic element comprises means for performing sequential and combinatorial logic procedures to generate the chip-select signals"; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 15 – col. 23, l. 25;

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CLAIM	STATUS AS OF THE DATE OF THIS AMENDMENT	SUPPORT FOR NEW OR AMENDED CLAIM CAN BE FOUND AT LEAST AT:
		Figs. 3A, 3B.
115	Pending	"the first command signal is a row access command signal"; col. 8, l. 65 – col. 9, l. 21.
		"the logic element uses sequential and combinatorial logic procedures with at least one address bit of the set of input control signals and the at least one chip-select signal to generate chip-select signals for the second command signal"; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 15 – col. 23, l. 25; Figs. 3A, 3B.
116	Pending	"the logic element further uses the sequential and combinatorial logic procedures with the at least one address bit to generate chip-select signals for a column access command signal subsequent to the row access command signal"; col. 17, l. 28 – col. 19, l. 52.
		"the memory module receives a second column access command signal between receiving the row access command signal and the subsequent column access command signal"; col. 14, ll. 12-14; Figs. 4A, 4B.
117	Pending	"the input command signal is a row access command signal"; col. 8, l. 65 – col. 9, l. 21.
		"logic element uses sequential and combinatorial logic procedures with at least one address bit of the set of input signals and the chip-select signal to generate a chip-select signal for the output command signal"; col. 17, l. 28 – col. 19, l. 52; col. 22, l. 15 – col. 23, l. 25; Figs. 3A, 3B.
118	Pending	"the logic element further uses the sequential and combinatorial logic procedures with the at least one address bit to generate a chip-select signal for a column access command signal subsequent to the row access command signal"; col. 17, l. 28 – col. 19, l. 52.
		"the memory module receives a second column access command signal between receiving the row access command signal and the subsequent column access command signal"; col. 14, ll. 12-14; Figs. 4A, 4B.

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REMARKS

Claims 1-118 are pending in this *inter partes* reexamination proceeding for consideration. New Claims 52-118 have been added, and Claims 1-51 remain as originally issued. While the Office Action for this merged proceeding ("the Office Action") rejects Claims 1-15 and 18-51 under various bases[1], the Patent Owner traverses the adopted grounds of rejection of Claims 1-15 and 18-51 and submits that all of the pending claims are patentable. The Patent Owner is also submitting herewith a "Declaration of Dr. Carl Sechen Under 37 C.F.R. § 1.132" ("the Sechen Declaration") in support of various points discussed in this Response.

I.   Introduction

As described more fully below, Patent Owner respectfully submits that original Claims 1-51, as well as new Claims 52-118,[2] are patentable over the prior art cited in the Office Action.

With respect to original independent claim 1, <u>none</u> of the cited prior art anticipates or renders obvious a "logic element receiving a set of input control signals … comprising … bank address signals … [for] generating a set of output control signals in response to the set of input control signals." As further specified in claim 1, the "set of input control signals" corresponds to a second number of DDR memory devices arranged in a second number of (e.g., logical) ranks and the "set of output control signals" corresponds to a first number of DDR memory devices arranged in a first number of (e.g., actual physical) ranks. Each of original independent claims 15, 28, and 39 recites similar features. The prior art does not disclose or suggest such features as recited in these original independent claims. Because of this significant deficiency in each cited prior art reference, Patent Owner respectfully submits that each ground of rejection adopted by the Examiner finding claims 1, 15, 28, and 39 anticipated or obvious over the prior art is overcome. All the remaining pending claims are dependent upon one of independent claims 1,

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[1] The "Summary of Action" of the Office Action states that Claim 21 is confirmed and that Claims 1-20 and 22-51 are rejected. However, a closer analysis of the rejections adopted by the Office Action show that Claims 16 and 17 have not been rejected and that each of Claims 1-15 and 18-51 has been rejected on one or more bases. Therefore, the patentability of Claims 16 and 17 has been confirmed.

[2] The Patent Owner submits that new Claims 52-118 do not add new matter and do not improperly broaden the claim scope of the claims. None of the new Claims 52-118 broaden the scope of these claims beyond the scope of all the other claims of the '912 patent. Therefore, pursuant to M.P.E.P. §§ 1412.03 and 2658(III)(A), these amendments are proper.

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15, 28, and 39, respectively, and are patentable over the cited prior art for at least the same reason.

Furthermore, none of the cited prior art anticipates or renders obvious, a "phase-lock loop device operatively coupled to ... the logic element," as required by original independent claims 1, 15, 28 and 39. Without the benefit of hindsight reconstruction of the invention using the '912 patent specification as a template, persons of ordinary skill in the art would not have been motivated, nor would they have found it obvious, to modify the devices taught in the cited prior art to satisfy this claim limitation. This reason alone is sufficient to overcome each ground of rejection adopted by the examiner against original independent claims 1, 15, 28 and 39. All remaining pending claims are dependent upon respective ones of independent claims 1, 15, 28, and 39, and are patentable over the cited prior art for at least the same reason.

As discussed in detail below, various dependent claims recite further limitations that are also not anticipated or rendered obvious by the cited prior art.

II.   Summary of the Claimed Invention

The '912 patent discloses and claims a memory module that includes DDR memory devices with certain attributes (e.g., memory capacity, number of rows and columns of memory locations) arranged in one memory configuration, but is able to operate in response to input signals from the computer system corresponding to DDR memory devices with different attributes arranged in a different memory configuration. For example, certain embodiments of the claimed invention include a memory module having four ranks of DDR memory devices each having a memory capacity (the actual, physical memory capacity), but able to operate in response to input signals corresponding to two ranks of DDR memory devices each having twice the actual, physical memory capacity (the logical memory capacity).

The claims of the '912 patent recite features that allow the memory module to achieve this goal in the context of DDR technology. As explained in detail below, such memory modules, with the claimed combinations of these features, have not previously been disclosed in the prior art, and are not obvious to persons of ordinary skill in view of the prior art.

III.   Secondary Considerations

With regard to the various rejections based on obviousness discussed herein, Patent Owner is submitting herewith a "Declaration of Christopher Lopes" ("the Lopes Declaration") and a "Declaration of Hyun Lee, Ph.D." ("the Lee Declaration"). The Lopes Declaration

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provides proof of the praise by others in the industry received by Netlist's HyperCloud™ memory modules due to its technical merits, as evidenced by quotations from various industry publications. The Lopes Declaration also provides proof of the industry acceptance received by Netlist's HyperCloud™ memory modules due to its technical merits, as evidenced by quotations from various Netlist customers. The Lee Declaration provides evidence that this praise and acceptance in the industry are, due to features and capabilities of the HyperCloud™ memory module which embody the claimed features of the '912 patent. This evidence of secondary considerations rebuts any *prima facie* case of obviousness that may be presented. Furthermore, Office personnel "must consider evidence secondary considerations of non-obviousness when determining whether an obviousness rejection should stand." *In re Huai-Hung Kao*, 639 F.3d 1057, 1066 (Fed. Cir. 2011).

IV.   Grounds 3 and 4: Anticipation and Obviousness In View of Amidi

Claims 1-11, 14, 15, 18-20, 22-25, 27-34, 36-46, 50, and 51 are rejected under 35 U.S.C. § 102(e) as being anticipated by Amidi.[3] Claims 1-15, 18-20, 23-25, 27-34, 36-43, 45-48, 50, and 51 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Amidi.[4] As discussed below, Amidi does not anticipate Claims 1-11, 14, 15, 18-20, 22-25, 27-34, 36-46, 50, and 51 since Amidi does not disclose each and every limitation recited by these claims. Further, Claims 1-15, 18-20, 23-25, 27-34, 36-43, 45-48, 50, and 51 are patentable over Amidi since the claimed features missing from Amidi are not rendered obvious by the knowledge of persons of ordinary skill in the art.

Generally, Amidi discloses a DDR memory module which includes a CPLD which receives a row or column address bit and two chip-select signals from the computer system to

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[3] The '0578 Request extensively relies upon disclosure from the JEDEC Standards in its proposed anticipation rejection under 35 U.S.C. § 102 based on Amidi. The Patent Owner submits that these rejections are more properly considered to be obviousness rejections under 35 U.S.C. § 103.

[4] The examiner of the '912 patent explicitly stated that its claims were patentable over Amidi ('912 patent Notice of Allowance at pp. 6-7) and Amidi is included in the list of cited references in the '912 patent ('912 patent at p. 2, 2nd column). These facts are in contrast to statements made in the '1339 Request at p. 27 ("nor has [Amidi] been applied to any claim of the ['912 patent]") and in the '0578 Request at p. 31 ("Amidi was not cited by the examiner during the prosecution of the '912 patent, and … Amidi was not before the Patent Office during the initial examination of the '912 patent and is not cited on the face of the '912 patent among the "prior art.").

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generate four chip-select signals by performing row address decoding or column address decoding. While Amidi is probably the closest reference to the claims of the '912 patent, it does not disclose or suggest the various claimed features discussed in detail below.

A. Amidi fails to disclose or render obvious a "logic element" that uses "bank address signals" to generate "output control signals" as required by the claims of the '912 patent

Each of Claims 1 and 28 recites "a circuit comprising a logic element and a register" and "the logic element receiv[es] a set of input control signals … comprising … bank address signals . . . [for] generating a set of output control signals in response to the set of input control signals." Similarly, Claim 15 recites that "the logic element receiv[es] a set of input signals … comprising … bank address signals … [for] generating a set of output signals in response to the set of input signals," and Claim 39 recites that "the logic element receives the bank address signals … [for] generating a plurality of output signals in response to the plurality of input signals."

1.   Broadest reasonable interpretation of "logic element"

Various portions of the three Requests seek to interpret the term "logic element" to be a conceptual construct that encompasses the combination of a decoding or conversion logic device (e.g., the CPLD of Amidi) and a separate register that receives the bank address signals (e.g., the register of Amidi). This interpretation is incorrect and contrary to the teachings of the '912 patent as would be understood by persons of ordinary skill in the art.

First, a logic element is understood by persons of ordinary skill in the art to be different than a state-holding device, such as a register. In other words, a register is strictly not a logic element. (Sechen Decl., ¶ 19.) The translation logic device and the register are disclosed in the prior art (e.g., Amidi) as being separate devices from one another, each operating on a corresponding different subset of the input signals received from the computer system (although there is some overlap between the two subsets) with different functions which produce different output signals transmitted to the memory devices, and having its operations timed to different clock signals (see, e.g., Amidi at ¶¶ 50, 58; Figs. 6A, 6B). For example, the translation logic device of Amidi (i.e., the CPLD) is disclosed as receiving the cs0, cs1, Add(n), CAS, RAS, WE, CLK0, and CLK0_N signals and utilizing Add(n), cs0, and cs1 to determine the selected rank (Amidi at ¶¶ 43, 50). The register disclosed by Amidi (i.e., the register) is disclosed as receiving the Add[n-1;0], RAS, CAS, WE, BA[1:0], and CKE, as well as CLK_0 and CLK_N from the

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PLL to synchronize the incoming address and control signals with respect to differential clock signals and to eliminate loading on the main controller (Amidi at ¶¶ 38, 50). This function of a register as a temporary data storage element for at least one clock cycle (e.g., its output signal value is a replica of its input signal value at the rising edge of its clock) is unambiguously well known and used in the art. Neither the registers disclosed by the '912 patent nor by Amidi, for example, are involved in translating functions to convert a first set of input signals into a set of output signals as required in the claims of the '912 patent. Moreover, they are inherently incapable of doing so. (Sechen Decl., ¶ 19.) Persons of ordinary skill in the art would not consider such functionally separate and different devices to be parts of the same "logic element." (Sechen Decl., ¶ 20.)

Second, the language of Claims 1, 15, 28, and 39 recites the "logic element" and the "register" as separate elements, and the '912 patent describes "the logic element" and "the register" as being distinct entities with distinct functions (see, e.g., '912 patent at col. 5, ll. 31-36; col. 6, ll. 55-63; col. 7, ll. 43-46). While the '912 patent discloses that these distinct entities may be parts of a single component ('912 patent at col. 5, ll. 37-42), such packaging does not merge or otherwise affect the distinct functions performed by the logic element and the register. Persons of ordinary skill in the art would still consider the logic element and the register to be distinct from one another, even if they were both contained in a single package since they have separate and distinct functionalities. (Sechen Decl., ¶ 20.) Thus, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the translation logic device and the register that passes signals onto the DRAM devices.

Amidi does not disclose or render obvious such a logic element. Instead, Amidi discloses (i) a register that receives the bank address signals and that transmits these bank address signals to the memory devices, and (ii) an emulator (e.g., a CPLD) that receives some input signals but that does <u>not</u> receive any bank address signals (Amidi at ¶¶ 50, 58; Figs. 6A, 6B). A register may include some simple logic that controls how signals are ordinarily temporarily stored for at least one clock cycle and outputted from the register (e.g., as is clearly shown and specified in detail in JEDEC standard JESD82-4B). Persons of ordinary skill would not interpret such a register's functionality to be that of a "logic element." (Sechen Decl., ¶¶ 19, 20.) Furthermore, as discussed above, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the functionality of the CPLD and such functionality of the register

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of Amidi. Thus, Amidi does not disclose or render obvious a logic element receiving a set of signals comprising bank address signals.

The '1339 Request seeks to use typographical errors in Amidi's figures to fabricate support for Amidi's disclosure of this claim interpretation. For example, the '1339 Request (e.g., at pp. 102, 109, 115, and 122) refers to Amidi's Fig. 7 and states that "[Amidi] discloses that the logic element (i.e., CPLD) determines the active bank based on address signals."[5] While Amidi's Figs. 5, 7, and 8 include the term "bank," it is clear from the context and the corresponding text (see, e.g., Amidi at ¶¶ 20, 43, 44, 49, 57, 62, 64) that these instances are typographical errors and are actually meant to refer to "rank." Throughout its specification, Amidi teaches that the extra address line and the two chip-select signals are used to determine which rank is selected, not bank. Thus, no portions of Amidi, including Fig. 7, disclose that the logic element receives the bank address signals, as recited by Claims 1, 15, 28, and 39.

Nor would it be obvious to persons of ordinary skill in the art to modify Amidi's system by providing the bank address signals to the logic element. Amidi does not discuss any rationale for making this modification, since the CPLD is disclosed by Amidi as being fully functional without having these bank address signals received by the CPLD. For example, Amidi at Fig. 8 and ¶¶ 64-70 discloses an internal circuitry of the CPLD that does not utilize the bank address signals at all. Amidi discloses that the <u>register</u> receives the input control signals, including the bank address signals, so that they can be clocked through the register to the DDR memory devices for their normal function of specifying the bank of memory locations from which data is to be read or written. (Sechen Decl., ¶ 23.) Providing such unneeded signals to the CPLD of Amidi would be seen by persons of ordinary skill in the art as introducing unnecessary complexity in designing the module without any concomitant benefits, and would be contrary to ordinary design practices (e.g., minimizing the number of interconnect signals and associated trace lengths). . Persons of ordinary skill in the art would not have been motivated to add the bank address signals in addition to the row and column address signals to Amidi's system to generate control signals for accessing actual physical memory locations. (Sechen Decl., ¶ 23.)

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[5] Note that the '1339 Request repeatedly uses the notation "i.e." to equate the "logic element" of the '912 claims to the CPLD of Amidi. This interpretation is the proper one, and is contrary to the improper claim interpretation used elsewhere by the three Requests that the "logic element" includes both Amidi's CPLD and its register.

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A rationale for such a modification of Amidi is also not provided by any of the other cited references or in the knowledge of persons of ordinary skill in the art.[6] As discussed more fully below, none of the cited references discloses utilizing the bank address signals for any other purpose except for merely clocking the bank address signals through the register to the memory devices for their normal function of specifying the bank from which data is to be read or written. Furthermore, for the reasons discussed with regard to the rejection based on Micron in view of Amidi below, persons of ordinary skill in the art would not find it obvious to produce a memory module that uses bank address signals to generate the output control signals, and such a memory module would not satisfy the recited features of the independent Claims 1, 15, 28, and 39.

In stark contrast to the teachings of Amidi, the claimed invention of the '912 patent provides the bank address signals to the <u>logic element</u> to determine which output control signals, including rank-selecting signals, to generate and transmit to the DDR memory devices (see, e.g., '912 patent at col. 17, l. 32 – col. 19, l. 52). (Sechen Decl., ¶ 24.) The bank address signals are not simply clocked through the logic element, as would be the case if the logic element provided the function of the register. Instead, the logic element provides translation procedures and structures that allow the memory module to properly execute back-to-back adjacent read commands or successive read commands that access memory locations across device boundaries, as discussed more fully below. These translation procedures and structures are not taught by Amidi or by any of the other cited references (Sechen Decl., ¶ 24), and would not have been known or foreseen by persons of ordinary skill in the art until after reading the '912 patent specification. (Sechen Decl., ¶ 24.) Therefore, persons of ordinary skill in the art would not have found it obvious to modify Amidi to produce the claimed invention.

Even if both the translation logic device and the register in Amidi, for example, are erroneously interpreted to be components of a larger "logic element," such a "logic element" still

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[6] The '1339 Request at p. 128 states that "it would have been obvious … to provide such input control signals to the logic element to improve the active bank/rank determination." However, the '1339 Request provides no support for this conclusory statement, such as a citation to prior art or a rationale known to persons of ordinary skill in the art for how and what type of "improvements" of the active bank/rank determination would be provided. The '0579 Request proposes rejections based on Micron in view of Amidi and Micron in view of Connolly, stating that bank address decoding would be obvious to persons of ordinary skill in the art. The flaws of this interpretation are discussed herein in Sections VII.B.1 and X.C.1.

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does not generate output control signals in response to input control signals, which include bank address signals, as required by the '912 patent claims.

Furthermore, such a "logic element" is not responsive at least in part to the bank address signals by generating rank-selecting signals (e.g., chip-select signals) (see, e.g., new Claims 52, 58, 64-67, 74, 77, 82, 87, 95, 97, 99, and 101) since the translation logic device that generates these signals in the proposed interpretation still does not receive the bank address signals, the register does. Such a "logic element" also does not generate the rank-selecting signals in response at least in part to the clock signals of the PLL device (see, e.g., new Claims 54, 57, 68, 79, 84, and 89). Further, new Claims 55, 59, 91, and 92 recite the distinct operations of the logic element and the register, making the claim interpretation proposed by the Requests inapplicable. In addition, as discussed below, the claimed invention including these features would not be obvious to persons of ordinary skill in the art. Therefore, these new claims are patentable despite this proposed interpretation of "logic element."

B.   **Amidi fails to anticipate or render obvious a PLL operatively coupled to the logic element as required by claims of the '912 patent**

Each of Claims 1, 15, 28, and 39 recites "the phase-lock loop device [is] operatively coupled to ... the logic element." Amidi does not disclose such a relationship between its phase-lock loop (PLL) device and its CPLD. Instead, Amidi at Figs. 6A and 6B discloses that the register receives clock signals from the PLL, and the CPLD receives clock signals from the computer system (see, also Amidi, ¶¶ 50, 58). Thus, Amidi does <u>not</u> disclose that the PLL is <u>operatively</u> coupled to the logic element.

1.   **Broadest reasonable interpretation of "operatively coupled" in the context of the '912 patent claims**

As disclosed by the '912 patent, "the phase-lock loop device 50 transmits clock signals to ... the logic element 40" ('912 patent, col. 5, ll. 28-31; see also, Figs. 1A, 1B). Therefore, persons skilled in the art understand that, consistent with the specification, the phrase "operatively coupled to" in the context of the '912 patent means that the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PLL 50. In other words, the output of the PLL 50 controls the operation of the logic element 40. (Sechen Decl., ¶ 15.)

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Both the '1339 Request and the '0578 Request seek to interpret the phrase "operatively coupled to" by ignoring the word "operatively."[7] For example, the '1339 Request at p. 104 and the '0578 Request at p. 960 state that this claim limitation is met by Amidi's disclosure at ¶ 50 that "a phase-lock loop (PLL) is coupled to the CPLD 604, the register 608 and the memory devices [and] relays the CLK_0 and CLK0_N signal to register 608 and memory devices 306." Notably, this passage of Amidi does <u>not</u> disclose that the CPLD receives clock signals from the PLL device. Instead, Amidi at Figs. 6A and 6B unambiguously show that the CPLD receives clock signals from the computer system (see, also Amidi, ¶¶ 50, 58). Therefore, Amidi does not have the generation of the chip-select signals by the logic element timed or otherwise responsive to the PLL clock signals, so Amidi does <u>not</u> disclose that the PLL device is <u>operatively</u> coupled to the logic element.

> 2. **It would not have been obvious to a POSITA to modify Amidi to arrive at the claimed invention of the '912 patent**

Absent using hindsight reconstruction of the invention using the '912 patent specification as a template, persons of ordinary skill in the art would not have considered modifying Amidi's system by operatively coupling the PLL clock signals to the logic element. None of the cited references, including Amidi, discusses any rationale for making this modification. Amidi discloses that its PLL device is used "to generate a zero-delay buffer" off of the input clock signals from the computer system (Amidi, ¶ 39). A zero-delay buffer is well known device that is ordinarily used to relay or buffer the input clock signals using many output clock drivers to transmit tuned and balanced replicas of the input clock signals to the DDR memory devices, by employing a PLL to match the phase of each of the output clock signals to the input clock signals. Various examples of zero-delay buffers comprising PLL circuitry have been previously described, manufactured, and sold by many companies (e.g., Altera, IDT, Cypress, Pericom) dating back to at least 1998. As shown in Figs. 6A, 6B, the output clock signals from the PLL device are transmitted to the register and to the memory devices, but not to the CPLD. Instead,

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[7] Such an interpretation improperly reads the limitation "operatively" out of the claims (see, M.P.E.P. § 2143.03 "All claim limitations must be considered"). Such an interpretation does not conform to the guidance from the Federal Circuit that construction of claim terms be consistent with the specification and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, Fed. Cir. 2009-1418.

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Amidi's CPLD receives the input clock signals from the computer system (Amidi, Figs. 6A, 6B). (Sechen Decl., ¶ 51.)

Amidi discloses that its CPLD is fully functional by being clocked by input clock signals received from the computer system, and Amidi does not discuss any alternatives or provide any reason for diverting from such a configuration. (Sechen Decl., ¶ 52.) Furthermore, the knowledge of persons of ordinary skill in the art would not lead them to divert from Amidi's configuration. In fact, the knowledge of persons of ordinary skill in the art, along with ordinary industry design practices, would lead to electrically connecting the CPLD of Amidi to the computer system input clock signals, and not to the output of the zero-delay buffer. (Sechen Decl., ¶ 52.)

First, it is well-known that the timing and waveform characteristics of signals propagating between the various components of the memory module are highly dependent on a complex set of variables, some of which are inter-related variables (e.g., the particular location and layout of the loads, circuit traces, and signal discontinuity points of the memory module). It is critically important that these variables are all properly controlled in order to avoid catastrophic failure of the memory module. For example, due to transmission line effects, as well as variations of signal trace design, variations of memory device layouts on the board, and variations in the number of loads per clock line, the output driver can see large variations in impedances, loading, signal path return currents, and terminations. This results in numerous issues (e.g., signal edge aberrations, reflections, amplitude problems, crosstalk, jitter, and ground/supply voltage bounce), all of which can lead to failure of the memory module resulting in failure of the computer system. These effects are more severe as the speed of operation increases. For this reason, the design of any new memory module entails a large amount of time and effort to tune the various design parameters and variables to ensure sufficient signal timing and waveform characteristics for proper operation.

Due to the large number of variables involved, exacerbated by the various interdependencies and other second order effects, it is not an easy task to design a memory module. Quite a number of fine-tuning iterations are required during the design process, encompassing a fair amount of trail and error, in order to obtain a working memory module design and then to optimize it. Even after the development of the JEDEC specification standards for memory modules, some manufactured and sold memory modules either failed to inter-operate

or produced intermittent failures that plagued the personal computer industry. Industry leaders (e.g., Intel) recognized the source of these errors and allocated resources to form a large consortium of industry leaders and research institutions to collaborate to resolve these system failures. For example, as early as 1998, the PC100 standard was born out of such a consortium and provided reference designs of memory modules complete with (i) bills of materials that specified prequalified parts, (ii) electrical schematics with every electrical connection point on a memory module, (iii) Gerber files that specify the complete layout of interconnecting traces within each printed circuit board (PCB) layer of the memory module, and (iv) the values and placement of resistors and capacitors onto the PCB. To ensure interoperability and system level performance, reference designs are continuously provided to DDR memory module manufacturers. There are only a small number of memory module reference designs (e.g., raw cards) per type of memory module that are specified by JEDEC standards (see, JEDEC 21-C at pp. 10-16, 29-35), since developing a new memory module entails significant time and effort. (Sechen Decl., ¶ 54.)

While expending such time and effort are commonplace in the design of a new memory module, persons of ordinary skill would not seek to do so unless absolutely necessary and they would try to keep such activities to a minimum. (Sechen Decl., ¶ 55.) In particular, if a person of ordinary skill in the art sought to add a CPLD to a memory module as disclosed by Amidi, they would begin with Amidi's disclosed configuration of timing the CPLD using the computer system input clock signals, and would tune the design parameters to try to achieve proper operation. Persons of ordinary skill in the art would know that operationally coupling the CPLD to the PLL device (i) would change the load on the PLL, degrading its performance, in other words, degrading the relationship between the PLL output clock and the computer system input clock signal, and (ii) would result in the aberration of the waveform characteristics of these PLL output clock signals propagating to the DRAM devices (e.g., slew rate, jitter, and skew). These changes in clock signal timing and waveform characteristics would be seen by a person of ordinary skill in the art to likely result in a high risk of the memory module not working at all, or operating intermittently. Therefore, such persons would not be tempted to make this change.

Second, making such a modification as proposed by the Requests goes against accepted practices in memory module design. Amidi's configuration in which (i) both the CPLD and the PLL device are timed to clock signals from the computer system, and (ii) the register and the

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DDR memory devices are timed to clock signals from the PLL device is in accordance with what a person of ordinary skill would immediately recognize as seeking to maintain the synchronous nature of the DDR memory module. (Sechen Decl., ¶ 56.) To modify Amidi's configuration by clocking the CPLD from the PLL device as recited in the claims would run against accepted and conventional industry practices. (Sechen Decl., ¶ 56.)

Third, the signal propagation delays through the CPLD (see, e.g., Fig. 8) would be recognized to be different from the delays through the register in Amidi's design, if for no other reason than that one is a logic device (the CPLD) and the other is not (the register). In order to synchronize the arrival of the "Signals to Memory Devices" in Fig. 6A of Amidi, one of ordinary skill in the art would immediately want to adjust the two clock arrival times, namely, the arrival at the CPLD and the arrival at the register. Indeed, two separate clocks are exactly what is depicted in Fig. 6A. Consequently, one of ordinary skill in the art would routinely believe that Amidi teaches that the CPLD should not receive the output of the PLL. (Sechen Decl., ¶ 57.)

Fourth, modifying a JEDEC memory module reference design by clocking the CPLD directly from the computer system input clock signals and not from the PLL output clock signals provides the flexibility that persons of ordinary skill in the art would expect to design, adjust, and tweak the memory module without having to change the already well balanced and matched traces of the PLL output clock signals. Otherwise, the inevitable tuning of the PLL device would be significantly more difficult to perform, and would result in a high risk of memory module failure or system failure. (Sechen Decl., ¶ 58.) For at least these reasons, providing the PLL clock signals to the CPLD would be seen by persons of ordinary skill in the art as introducing unnecessary complexity that can lead to failure. In contrast, providing the computer system input clock signals to the CPLD would be seen by persons of ordinary skill in the art as the obvious choice along with a low risk of failure since no changes to the critical PLL output clock signal paths is incurred. (Sechen Decl., ¶ 59.)

Therefore, for at least the reasons discussed above, persons of ordinary skill in the art would not have been prompted to modify Amidi to produce the claimed invention.

For at least the foregoing reasons, Patent Owner respectfully submits that grounds 3 and 4 for rejecting the '912 patent claims identified above have been overcome. Accordingly, Patent Owner respectfully requests withdrawal of these grounds of rejection.

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V.　Grounds 5, 6, 9, 11, 12 and 13: Obviousness Over Various Combinations of Prior Art

The proposed rejection of claims 1-15, 18-20, and 22-51 as obvious over Amidi and Dell 2 was adopted by the Examiner as Ground 5.

The proposed rejection of claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 as obvious over Amidi and JEDEC Standards was adopted by the Examiner as Ground 6.

The proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 as obvious over Dell 1 and JEDEC Standards was adopted by the Examiner as Ground 9.

The proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 as obvious over Wong and JEDEC Standards was adopted by the Examiner as Ground 11.

The proposed rejection of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 as obvious over Micron and Connolly was adopted by the Examiner as Ground 12.

The proposed rejection of claims 1, 3-4, 6-11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 as obvious over Micron and Amidi was adopted by the Examiner as Ground 13.

A.　None of the cited prior art discloses or render obvious a "logic element" that uses "bank address signals" to generate "output control signals" as required by the claims of the '912 patent

1.　Amidi and Dell 2 (Ground 5)

As discussed above, Amidi does not disclose or render obvious a memory module having a logic element that receives bank address signals to generate output signals as recited by independent Claims 1, 15, 28, and 39. Dell 2 does not cure the deficiencies of Amidi for at least the same reasons discussed above.

Generally, Dell 2[8] addresses the problem of using an M (e.g., 4) bank memory device in a computer system that only has addressing capability for N (e.g., 2) bank memory devices. Dell 2

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[8] The examiner of the '912 patent explicitly stated that its claims were patentable over Dell 2 ('912 patent Notice of Allowance at pp. 8-9), and Dell 2 is included in the list of cited references in the '912 patent ('912 patent at p. 2, 1st column). These facts are in contrast to statements made in the '1339 Request at p. 27 ("nor has [Amidi] been applied to any claim of the ['912 patent]") and at p. 159 ("[Amidi] and [Dell 2] were never … applied to any claim of the ['912 patent]").

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solves this problem by connecting or reassigning a row/column address bit to an additional bank address pin of the memory devices to use an M bank memory device in a computer system that has N bank addressing (Dell 2, col. 2, ll. 40-52). For example, the circuit "connect[s] the highest order address signal (in this case A12) to the BA1 input pin of the memory devices" (Dell 2, col. 8, ll. 29-32; Fig. 1A). This connection of a row/column address signal to a bank address pin permits the memory module to use memory devices having <u>more</u> internal banks, when the memory controller provides bank address signals that are only sufficient for accessing memory devices with <u>fewer</u> internal banks (Dell 2, col. 4, ll. 24-51).

As discussed above, Amidi does not disclose or render obvious a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39. Patent Owner further submits that persons of ordinary skill in the art would not find it obvious to modify Amidi using the system disclosed by Dell 2. Amidi and Dell 2 are directed to opposing problems. Amidi is concerned with using more ranks of <u>cheaper, low-capacity</u> memory devices in place of fewer ranks of <u>more expensive, higher-capacity</u> memory devices to achieve cost savings (see, Amidi at ¶ 8, 11). In contrast, Dell 2 is concerned with using memory devices with more internal banks, which are generally <u>more expensive</u> (Sechen Decl., ¶ 26), to replace cheaper memory devices with fewer internal banks (see, Dell 2 at col. 4, ll. 48-51). Using memory devices with more internal banks as disclosed by Dell 2 would be counterproductive to Amidi's goal of achieving cost savings, so persons of ordinary skill in the art would not find it obvious to modify Amidi using the disclosure of Dell 2.

Furthermore, Amidi and Dell 2 address their respective problems in different ways. Amidi addresses its problem by generating a larger number of chip-select signals for the larger number of ranks of memory devices using the smaller number of chip-select signals and an otherwise unused row/column address bit. In contrast, Dell 2 addresses its problem without generating any additional signals. Instead, Dell 2 merely connects a row/column address bit to an additional bank address pin. In other words, the row/column address bit is used differently by Amidi (i.e., decoding the row/column address bit along with the received chip-select signals to generate a larger number of chip-select signals) than by Dell 2 (i.e., the row/column address bit becoming a bank address bit). Because these solutions are significantly different from one another, persons of ordinary skill in the art would not find it obvious to modify Amidi using the disclosure of Dell 2. (Sechen Decl., ¶ 27.)

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The '1339 Request at p. 162 proposes a rationale for the combination of Amidi and Dell 2 by stating that it would have been obvious "to combine the methods for emulating larger RAMs using smaller RAMs disclosed in [Amidi] with the logic element disclosed in [Dell 2] to realize larger memory capacity at a lower cost." However, the '1339 Request does not explain what modification of Amidi, using the disclosure of Dell 2, would purportedly achieve this goal so as to be obvious to persons of ordinary skill in the art. Furthermore, such a rationale of cost savings is not applicable to the disclosure of Dell 2 since the M (e.g., 4) bank memory devices would be <u>more</u> expensive than the N (e.g., 2) bank memory devices, not less. (Sechen Decl., ¶ 26.) Therefore, the '1339 Request does not provide a reasonable rationale for persons of ordinary skill in the art to modify Amidi using the disclosure of Dell 2.

Even if, for the sake of argument, it would be obvious to modify Amidi in view of Dell 2 to provide Amidi's CPLD with bank address signals, which it is not, such a modification still would not be sufficient for modifying Amidi's CPLD to be responsive at least in part to the bank address signals by generating a set of output control signals (e.g., rank-selecting signals) since the logic of Amidi that generates these signals in the proposed combination still would not receive the bank address signals, the register would. In particular, Dell 2 does not disclose that the circuit is responsive in any way to the received bank address bits. Instead, the circuit of Dell 2 merely passes the received bank address bits onto the M bank memory devices, along with the additional bank address bits resulting from the reassignment.

Further, new Claims 55 and 59 recite that the logic element does not transmit bank address signals to the DDR memory devices, making the disclosure of Dell 2 inapplicable. Thus, the claimed invention including these features would not be obvious to persons of ordinary skill in the art for at least the reasons discussed above, so these new claims are patentable over Amidi in view of Dell 2.

2.   Amidi and JEDEC (Ground 6)

JEDEC 21-C does not cure the deficiency of Amidi with respect to the use of bank address signals discussed above. Generally, JEDEC 21-C defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs). The DIMMs disclosed by JEDEC 21-C are, by definition, conventional DIMMs conforming to the design standard of JEDEC 21-C.

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Patent Owner submits that JEDEC 21-C does not provide any additional disclosure or suggestion to modify Amidi to have its CPLD receive bank address signals such that persons of ordinary skill in the art would find it obvious to do so. For reasons similar to those discussed above with respect to Amidi, persons of ordinary skill would not interpret JEDEC 21-C's register as being a "logic element," so JEDEC 21-C does not include a logic element that receives a set of input control signals comprising bank address signals. While JEDEC 21-C's register does receive bank address signals, so does Amidi's register, so it is not clear what additional disclosure or suggestion JEDEC 21-C provides with regard to this claim feature that is not already disclosed or suggested by Amidi alone.

There is no disclosure in the cited references, including Amidi and JEDEC 21-C, that teaches or suggests that bank address signals can be used for the type of translation described by Amidi using row and column addresses. Neither Amidi nor JEDEC 21-C discusses any rationale for modifying Amidi's system by providing the bank address signals to the logic element. JEDEC 21-C does not have any logic that uses the bank address signals except for passing them onto the DDR memory devices via the register. The logic element of Amidi is disclosed as being fully functional without having these bank address signals received by the CPLD. For example, Amidi at Fig. 8 and ¶¶ 64-70 discloses an internal circuitry of the CPLD that does not utilize the bank address signals at all. Therefore, the rationale for the proposed modification cannot come from the cited references. (Sechen Decl., ¶ 29.)

Both Amidi and JEDEC 21-C disclose that the register receives the bank address signals so that they can be passed through to the DDR memory devices for their normal function of specifying the bank from which data is to be read or written. Conversely, by providing the bank address signals to the logic element as well, the claimed invention uses the bank address signals for a different function, namely, in determining which rank-selecting signal to generate and transmit to the DDR memory devices (Sechen Decl., ¶30), thereby allowing the memory module to properly execute back-to-back adjacent read commands or successive read accesses across device boundaries. This function was not foreseen by Amidi or by JEDEC 21-C and would not have been known or foreseen by persons of ordinary skill in the art to be useful. (Sechen Decl., ¶ 30)

Furthermore, the intended purpose of the JEDEC 21-C reference is to describe a DIMM that conforms to the JEDEC standard, and conformance to such industry standards is seen by

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persons of ordinary skill in the art to be a desirable goal to have success in the marketplace. (Sechen Decl., ¶ 31.) To the extent that the system disclosed by Amidi is not JEDEC-compliant, a DIMM made by the proposed combination of Amidi and JEDEC 21-C would not work for JEDEC 21-C's intended purpose. Therefore, persons of ordinary skill in the art would not have found it obvious to modify Amidi in view of JEDEC 21-C to produce the claimed invention.

3.   Dell 1 and JEDEC (Ground 9)

As discussed above, JEDEC 21-C does not disclose or suggest having a logic element receive the bank address signals, and Dell 1 does not cure the deficiencies of JEDEC 21-C. Generally, Dell 1[9] discloses a memory module with a plurality of DRAM devices and an ASIC chip. The DRAM devices are organized in two banks and are utilized in pairs (Dell 1, col. 3, l. 64 – col. 4, l. 10). The ASIC "receives the high order address bit A11, as well as the system RAS, from the system memory controller 20 and converts them to two RAS actuation signals RAS A and RAS B" (Dell 1, col, 4, ll. 28-32) with "RAS A being required to actuate one-half of the chip pair, and RAS B being required to actuate the other half of the chip pair" (Dell 1, col. 4, ll. 18-20). The DRAM devices of Dell 1 are not DDR memory devices, but extended data-out (EDO) memory devices. EDO memory devices do not have multiple internal banks of memory locations (Sechen Decl., ¶ 39), and are significantly different from the later-developed DDR memory devices that are recited in the claims of the '912 patent, as discussed more fully below.

The combination of Dell 1 and JEDEC 21-C does not disclose or render obvious a memory module having a logic element that receives bank address signals as required by the claims of the '912 patent. In particular, Dell 1 does not disclose or suggest a logic element receiving bank address signals, as acknowledged by the Office Action at p. 29. To the extent that the Office Action seeks to define the term "logic element" to be a conceptual construct that encompasses both the ASIC of Dell 1 and the register of JEDEC 21-C, Patent Owner traverses this interpretation for at least the same reasons discussed above. Thus, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the ASIC of Dell 1 and the register of JEDEC 21-C, even if the ASIC and the register were contained in the same package.

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[9] Dell 1 is included in the list of cited references in the '912 patent ('912 patent at p. 2, 1st column). This fact is in contrast to the statement made in the '0578 Request at p. 25 ("[Dell 1] was not before the Patent Office during the initial examination of the '912 patent").

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The only signals disclosed by Dell 1 as being received by its ASIC are RAS, CAS, and one row/column address bit (A11). The EDO memory devices used in Dell 1 do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so as discussed above, there is no need for Dell 1's memory module to receive such bank address signals. (Sechen Decl., ¶ 39.) The Office Action and the '0578 Request have not proposed any rationale for providing Dell 1's ASIC with bank address signals. Therefore, persons skilled in the art would not be aware of a rationale to transmit bank address signals to the memory module of Dell 1, let alone having Dell 1's ASIC receive such bank address signals.

JEDEC 21-C does not provide any additional disclosure or suggestion such that persons of ordinary skill in the art would find it obvious to modify Dell 1 to have its ASIC receive bank address signals. Even though JEDEC 21-C discloses a register that passes through bank address signals to the DDR memory devices, as discussed above, persons of ordinary skill would not interpret JEDEC 21-C's register as being a "logic element," so JEDEC 21-C does not include a logic element that receives a set of input control signals comprising bank address signals. (Sechen Decl., ¶ 40.) As discussed above, the claimed invention uses the bank address signals for a different function than does a register, which includes determining which rank-selecting signal to generate and transmit to the DDR memory devices. (Sechen Decl., ¶ 41.) This function is irrelevant to the EDO technology of Dell 1 since it does not use chip-select signals and doesn't have internal banks, so neither Dell 1 nor JEDEC 21-C provides a rationale for modifying Dell 1's system by sending bank address signals to the logic element. Therefore, claims reciting this feature are patentable over Dell 1 in view of JEDEC 21-C.

        a.   **A POSITA would not have combined Dell 1 with JEDEC 21-C**

As acknowledged by the Office Action at p. 29, Dell 1 does not disclose a memory module using DDR memory devices. Patent Owner submits that, due to the significant differences between DDR memory technology and Dell 1's EDO technology, persons of ordinary skill in the art would not find it obvious to replace the EDO memory devices of Dell 1 with the DDR memory devices of JEDEC 21-C, as proposed by the Office Action (e.g., for Claims 1, 15, 28, and 39, and various dependent claims).[10]

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[10] In proposing a motivation for the combination, the Office Action at p. 29 states that [i]t would have been obvious to one of ordinary skill in the art … to design the DIMM of Dell 1 in

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While DDR memory is an advance in memory technology with capabilities beyond those of previously-developed EDO memory technology, the significant differences between the two different protocols make substitution of DDR memory into Dell 1 impractical. These differences include but are not limited to: (i) memory organization (e.g., DDR memory devices have multiple selectable internal banks which are missing from EDO memory devices); (ii) different address and control signals (e.g., DDR technology uses bank address signals and chip-select signals that are not found in EDO technology); (iii) command signals/structure (e.g., DDR command protocol allows multiple chip-select signals to be asserted simultaneously, while EDO command protocol allows only one RAS to be asserted at a time); and (iv) EDO uses asynchronous operation, while DDR uses synchronous operation. (Sechen Decl., ¶ 105.) Modifying a device designed for one of these two protocols (e.g., Dell 1's EDO-compatible memory module) to incorporate features of the other of these two protocols (e.g., JEDEC 21-C's DDR devices) would result in a hybrid protocol, different from either EDO or DDR, that would require its own lengthy and costly system development. (Sechen Decl., ¶ 105.) Thus, these differences represent a huge technological hurdle that would prevent persons of ordinary skill in the art from considering substituting JEDEC 21-C's DDR memory devices for Dell 1's EDO memory devices. [(Sechen Decl., ¶ 105.) For example, properly accessing the multiple internal banks within DDR memory devices, not found in EDO memory devices, introduces significant complications that would require undue experimentation by persons of ordinary skill in the art if attempted without the disclosure of the '912 patent. (Sechen Decl., ¶ 106.) As another example, the differences between Dell 1's RAS signals in EDO technology and the chip-select signals in DDR technology are such that persons of ordinary skill in the art would not interpret Dell 1's RAS signals as chip-select signals, as proposed by the '0578 Request.[11] (Sechen Decl., ¶106.)

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compliance with the JEDEC standard to make it compatible with computer systems that expect DIMMs installed in the system to be standard compliant." However, persons of ordinary skill in the art would not seek to design a DIMM using EDO technology to conform to a DDR standard, such as JEDEC 21-C. EDO technology has its own set of industry standards, and if persons of ordinary skill in the art wished to make the Dell 1 memory module "standard compliant" as suggested by the Office Action, they would look to the EDO standards, not DDR standards.

[11] The Office Action at p. 7 acknowledges that RAS signals are not chip-select signals (in discussion of the QBMA reference). The '0578 Request also acknowledges that "[Dell 1] does not explicitly disclose the use of 'chip-select' signals (see, e.g., p. 205).

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In addition, EDO memory technology constrains command sequences for reading or writing data such that the row activation (RAS) command is immediately prior to the column access (CAS) command, without intervening RAS or CAS commands. Therefore, EDO technology is not capable of providing the benefits of executing back-to-back adjacent read commands across memory device boundaries or successive read accesses from different ranks of memory devices, as can DDR memory technology. (Sechen Decl., ¶ 107.)

The '0578 Request does not acknowledge these differences between DDR and EDO memory technologies, either by not addressing the differences, or, in multiple places, by incorrectly stating that Dell 1 explicitly references DDR technology or discloses the use of DDR technology.[12] The '0578 Request at p. 198 also states that "[t]he difference between the claimed invention and [Dell 1] is that [Dell 1] does not explicitly disclose the use of certain signals." This statement trivializes the significant differences between DDR and EDO memory technologies in a manner in which persons of ordinary skill in the art would not agree. (Sechen Decl., ¶ 108.)

Therefore, persons of ordinary skill in the art would not find it obvious to replace the EDO memory of Dell 1 with the DDR memory of JEDEC 21-C as proposed by the Office Action, so the claims of the '912 patent are allowable over Dell 1 in view of JEDEC 21-C at least on this basis. (Sechen Decl., ¶ 108.)

4.   Wong and JEDEC (Ground 11)

As discussed above, JEDEC 21-C fails to disclose or suggest using bank address in the manner required by the '912 patent claim. Wong does not cure this deficiency of JEDEC 21-C. Generally, Wong [13] discloses a memory module with a plurality of DRAM devices organized as an upper memory bank 1012 and a lower memory bank 1022 of DRAM memory elements 1002,

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[12] E.g., "One of ordinary skill in the art would be motivated to combine the teachings of [Dell 1] with the teachings of [JEDEC 21-C] because [Dell 1] explicitly references DDR DIMMs, and [JEDEC 21-C] define[s] specifications for DDR DIMMs" (p. 173); "[Dell 1] discloses the use of JEDEC compliant DDR DIMMS" (p. 198); "[Dell 1] discloses a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board" (p. 5 of Ex. CC-B). Dell 1 actually makes <u>no</u> mention of DDR DIMMs.

[13] Wong was included in the list of cited references in the '912 patent ('912 patent at p. 2, 1st column). This fact is in contrast to the statement made in the '0578 Request at p. 29 ("Wong was not before the Patent Office during the initial examination of the '912 patent").

with a buffer chip 1003, and a bank control circuit 2000.[14] The DRAM devices of Wong are not DDR memory devices, but EDO memory devices. As discussed above, EDO memory technology is significantly different from the later-developed DDR memory technology that is recited in the claims of the'912 patent. (Sechen Decl., ¶¶ 105-107.)

Wong discloses that the buffer chip 1003 receives data signals, address signals, and control signals and provides additional fan-out capability for these signals to the upper memory bank 1012 and the lower memory bank 1022 (Wong, col. 4, ll. 7-11 and 23-28). Wong further discloses that the bank control circuit 2000 receives a CAS0 signal, a RAS0 signal, and an address signal A13, and depending on the combination of these inputs, the bank control circuit decodes the address with either multiple RASUX signals to the memory devices of the upper memory bank or multiple RASLX signals to the memory devices of the lower memory bank (Wong, col. 4, ll. 33-38 and 60-63, col. 5, ll. 16-18).

The combination of Wong and JEDEC 21-C does not disclose or render obvious a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39 and various dependent claims. In particular, Wong does not disclose or suggest a logic element receiving bank address signals, as acknowledged by the Office Action at p. 36. To the extent that the Office Action seeks to define the term "logic element" to be a conceptual construct that encompasses both the bank control circuit of Wong and the register of JEDEC 21-C,[15] the Patent Owner traverses this interpretation for at least the same reasons discussed above in Section I.B. Thus, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the bank control circuit of Wong and the register of JEDEC 21-C, even if the bank control circuit and the register were contained in the same package.

The only signals disclosed by Wong as being received by its bank control circuit are RAS0, CAS0, and one row/column address bit (A13). The EDO memory devices used in Wong do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so as discussed above, there is no need for Wong's memory module to receive such signals. The Office Action and the '0578 Request have not

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[14] The upper and lower banks of Wong are not the internal banks that are found in DDR memory devices and that are accessed using bank address signals (as in the '912 patent).
[15] This interpretation is proposed by the '0578 Request (e.g., at p. 799).

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proposed any rationale for providing Dell 1's ASIC with bank address signals.[16] Therefore, persons skilled in the art would not be aware of a rationale to transmit bank address signals to the memory module of Wong, let alone having Wong's bank control circuit receive such bank address signals.

As discussed above, JEDEC 21-C does not provide any additional disclosure or suggestion such that persons of ordinary skill in the art would find it obvious to modify Wong to have its bank control circuit receive bank address signals, so neither Wong nor JEDEC 21-C provides a rationale for modifying Wong's system by sending bank address signals to the logic element. Therefore, claims reciting this feature are patentable over Wong in view of JEDEC 21-C.

a.   A POSITA would not have combined Wong with JEDEC 21-C

As acknowledged by the Office Action at p. 36, Wong does not disclose a memory module using chip-select signals. The Patent Owner submits that persons of ordinary skill in the art would not find it obvious to replace the EDO memory devices of Wong with the DDR memory devices of JEDEC 21-C, as suggested by the Office Action (e.g., for Claims 1, 15, 28, and 39, and various dependent claims). As discussed above, EDO memory technology has significant differences from DDR memory technology, such that the proposed modification would be impractical and would represent a huge technological hurdle that would prevent persons of ordinary skill in the art from considering substituting JEDEC 21-C's DDR memory devices for Wong's EDO memory devices.[17]

The '0578 Request does not acknowledge these differences between EDO and DDR memory technologies, either by not addressing the differences, or, in multiple places, by incorrectly stating that Wong explicitly references DDR technology or discloses the use of DDR

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[16] The '0579 Request proposes rejections based on Micron in view of Amidi and Micron in view of Connolly, stating that bank address decoding would be obvious to persons of ordinary skill in the art. The flaws of this interpretation are discussed herein in Sections VII.B.1 and X.C.1.

[17] In proposing a motivation for the combination, the Office Action at p. 37 states that [i]t would have been obvious to one of ordinary skill in the art … to design the DIMM of Wong in compliance with the JEDEC standard to make it compatible with computer systems that expect DIMMs installed in the system to be standard compliant." However, persons of ordinary skill in the art would not seek to design a DIMM using EDO technology to conform to a DDR standard, such as JEDEC 21-C. EDO technology has its own set of industry standards, and if persons of ordinary skill in the art wished to make the Wong memory module "standard compliant" as suggested by the Office Action, they would look to the EDO standards, not DDR standards.

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technology.[18] The '0578 Request at p. 815 also states that "[t]he difference between the claimed invention and Wong is that Wong does not explicitly disclose the use of certain signals." This statement trivializes the significant differences between DDR and EDO memory technologies in a manner in which persons of ordinary skill in the art would not agree. (Sechen Decl., ¶ 108, 110.)

Therefore, persons of ordinary skill in the art would not find it obvious to replace the EDO memory of Wong with the DDR memory of JEDEC 21-C as proposed by the Office Action, so the claims of the '912 patent are allowable over Wong in view of JEDEC 21-C at least on this basis.

5.   Micron and Connolly (Ground 12)

The combination of Micron and Connolly does not disclose or render obvious a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39 and various dependent claims.

Generally, Micron defines the electrical and mechanical features for the 1GB and 2GB (x72, ECC, DR) 184-pin Double Data Rate Synchronous DRAM Registered Dual In-Line Memory Modules (DDR SDRAM RDIMMs). The DIMMs disclosed by Micron are conventional RDIMMs conforming to the relevant JEDEC standards, including "JEDEC Standard JESD82," "JEDEC Standard JESD82-1A," and "the JEDEC MO document" (Micron at Table 12, note 1; Table 14, note 1; Fig. 7, note 2).

Connolly [19] is a continuation-in-part from Dell 1. Connolly includes substantially all of the disclosure of Dell 1, which as discussed above, discloses an EDO memory module that receives a system RAS and address bit from the system memory controller and converts them to two RAS actuation signals RAS A and RAS B. Connolly further discloses that the EDO memory module can convert a system CAS signal and another address bit into two CAS signals (see, Connolly, col. 9, ll. 7-8).

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[18] E.g., "One of ordinary skill in the art would be motivated to combine the teachings of Wong with the teachings of [JEDEC 21-C] because Wong explicitly references DDR DIMMs, and [JEDEC 21-C] define[s] specifications for DDR DIMMs" (p. 792); "Wong discloses the use of JEDEC compliant DDR DIMMS" (p. 815); "Wong discloses a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board" (p. 2 of Ex. CC-F). Wong actually makes <u>no</u> mention of DDR DIMMs.

[19] Connolly is included in the list of cited references in the '912 patent ('912 patent at p. 2, 1st column).

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Micron does not disclose or suggest a memory module having a logic element that receives bank address signals to generate output signals, contrary to the assertion in the Office Action at p. 42. Even though Micron discloses a register that passes bank address signals through to the DDR memory devices, persons of ordinary skill would not interpret Micron's register as being a "logic element," so Micron does not include a logic element that receives bank address signals. As acknowledged by the '0579 Request at p. G-5, "Micron does not disclose a distinct 'logic element' that receives the input control signals recited in the claim," which includes the bank address signals.

Connolly also does not disclose that its ASIC receives bank address signals. The only signals disclosed by Connolly as being received by its ASIC are RAS, CAS, and two row/column address bits. The EDO memory devices used in Connolly do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so there is no need for such signals for Connolly's EDO technology. For EDO technology, the ASIC of Connolly is disclosed as being fully functional without having these bank address signals received by the ASIC. Therefore, persons of ordinary skill in the art would not be aware of a rationale to transmit bank address signals to the memory module of Connolly, let alone having Connolly's ASIC receive such bank address signals. (Sechen Decl., ¶ 46.)

According to the '0579 Request at p. G-6, "one of ordinary skill in the art would include a logic element … where the logic element received bank address signals … so that the logic element could use the bank address … signals for control and command signal decode and remap." However, even if, for the sake of argument, there were a valid motivation to combine the teachings of Micron and Connolly, which there is not, this rationale for going further than Connolly's disclosure of row/column address conversion is speculative at best because there is no basis in the prior art or in the knowledge of persons of ordinary skill in the art to think that bank address signals could be used in this manner.[20]

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[20] Even though persons of ordinary skill in the art would know that DDR memory devices with different numbers of banks existed, as stated by the '0579 Request at p. G-6, this is insufficient rationale for concluding that such persons would extrapolate that bank address conversion could be performed using the disclosure of Connolly and would include the bank address signals as inputs to Connolly's ASIC.

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The only reason cited by the '0579 Request for Connolly's ASIC to receive bank address signals is for bank address conversion.[21]   However, there is no disclosure in the prior art, including Micron and Connolly, that teaches or suggests that bank address signals can be used for the type of conversion described by Connolly using row and column addresses, and the Office Action and the '0579 Request have suggested none. In addition, contrary to the characterization provided by the '0579 Declaration at ¶ 15, the bank address field is not treated in DDR technology in the same way that the row address and column address fields are. For example, bank address signals are used to supply certain initialization values to various control registers within the DDR DRAM devices (e.g., during a load mode register or extended mode register command). (Sechen Decl., ¶ 49.) Because of this additional initialization information that is multiplexed onto the bank address signals during certain DDR commands, persons of ordinary skill in the art contemplating the use of the bank address signals as inputs to Connolly's ASIC would know that failure would occur. Therefore, persons of ordinary skill in the art would not expect that using a bank address bit in Connolly's conversion logic would work. (Sechen Decl., ¶ 49.)

Furthermore, this reasoning proposed by the '0579 Request does not explain the claim features recited by Claims 1, 15, and 28 with regard to the logic element receiving at least four signals: at least one row/column address signal, at least two bank address signals, and at least one chip-select signal. Under the rationale proposed by the '0579 Declaration, if row/column address conversion of the at least one chip-select signal is being performed by Connolly's ASIC (so the DDR memory devices use all the bank address signals received by the memory module), there would be no need for the ASIC to also receive the bank address signals since they are not involved in the conversion. Similarly, if bank address conversion of the at least one chip-select signals is being performed by Connolly's ASIC, there would be no need for the ASIC to also

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[21] The '0579 Declaration at ¶ 10 states that even if the bank address signals are not involved in the conversion, they "can be optionally provided as an input at the discretion of the logic designer." For example, the '0579 Declaration at ¶ 15 states that "[t]he logic that implements the address and control signal conversion does not need to process the portion of the row address or column address fields that are in common between older and latest DRAM devices" (emphasis added). The Patent Owner submits that if a signal is not being used by a logic element, it makes little sense to route that signal to the logic element. Therefore, this rationale has no "rational underpinning to support the legal conclusion of obviousness" (*KSR* at 418 (quoting *In re Kahn* at 988)) of the claims.

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receive the at least one row/column address signal. The claim language recites that both "at least one row/column address signal" and "bank address signals" are received by the logic element. Therefore, at least for this reason, the rationale proposed by the '0579 Request is insufficient, and persons of ordinary skill in the art would not find providing all of these recited signals to Connolly's ASIC, as recited by Claims 1, 15, and 28, to be obvious.

As explained herein, the claimed invention goes beyond the proposed rationale with the realization that the bank address signals can be used for different functions than previously considered by the prior art, e.g., accounting for the possibility of having multiple ranks that have activated banks at any single moment. (Sechen Decl., ¶ 14.) Even during row/column address conversion, the claimed invention utilizes the bank address signals to determine which rank-selecting signals to generate and transmit to the DDR memory devices. (Sechen Decl., ¶¶ 87, 88.) In this way, the memory module can execute back-to-back adjacent read commands and successive read accesses from different ranks of DDR memory devices, for example. (Sechen Decl., ¶¶ 87, 88.) This function was not taught by Micron or by Connolly (Sechen Decl., ¶ 89) and would not have been known or foreseen by persons of ordinary skill in the art prior to reading the '912 patent. Patent Owner submits that persons skilled in the art would not have found this use of the bank address signals to be obvious.[22]

To the extent that the Office Action seeks to define the term "logic element" to be Micron's register or to be a conceptual construct that encompasses both the ASIC of Connolly and the Micron's register, the Patent Owner traverses this interpretation for at least the same reasons discussed above. Thus, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the ASIC of Connolly and the register of Micron, even if the ASIC and the register were contained in the same package.

     a.   **A POSITA would not have combined Micron and Connolly**

As discussed above with regard to Dell 1, EDO memory technology has significant differences from DDR memory technology, such that the proposed modification would be impractical and would represent a huge technological hurdle that would prevent persons of ordinary skill in the art from considering or utilizing the proposed combination. Thus, for at least similar reasons as those discussed above, actual application of Connolly's technique to modify

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[22] This function went unmentioned in the '0579 Request and the '0579 Declaration, indicating its non-obviousness.

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the DDR technology disclosure of Micron would have been beyond the skill of one of ordinary skill in the art (Sechen Decl., ¶¶ 47, 48) and, thus, would not have been obvious to persons of ordinary skill in the art. (See, *KSR* at 417; M.P.E.P. § 2143(C)).

Despite these differences between EDO and DDR addressing and command protocols, the Office Action at p. 44 asserts that it would have been obvious to one of ordinary skill in the art "to modify the design the DIMM of Micron to incorporate Connolly's technique." The '0579 Request at pp. 16-17 also minimizes these differences by asserting that "a person of ordinary skill in the art would have been able to design a module" by including elements of the design of Connolly into the memory module of Micron, and that despite any differences between such a combination and the claimed invention, the claims would be obvious. However, neither the Office Action nor the '0579 Request explains how the proposed combination would result in the claimed memory module. Further, this proposed combination of Micron in view of Connolly omits recited features of the claimed invention. When these recited features are properly considered, the Patent Owner submits that the combination of Micron and Connolly does not disclose or suggest the claimed invention.

5.   Micron and Amidi (Ground 13)

The combination of Micron and Amidi does not disclose or render obvious a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39 and various dependent claims. As discussed above for each reference separately, neither Micron nor Amidi disclose or suggest a logic element receiving bank address signals, as required by the claims of the '912 patent.

The Patent Owner further submits that the combination of Micron and Amidi does not provide any additional disclosure or suggestion such that persons of ordinary skill in the art would find it obvious to modify Micron or Amidi to include a logic element that receives bank address signals in the manner required by the '912 patent claims. For reasons similar to those discussed above with regard to Amidi, persons of ordinary skill would not interpret Micron's register as being a "logic element," so Micron does not include a logic element that receives a set of input control signals comprising bank address signals. While Micron's register does receive bank address signals, so does Amidi's register, so it is not clear what additional disclosure or suggestion Micron provides with regard to this claim feature that is not already disclosed or suggested by Amidi alone.

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The '0579 Request at p. H-7 acknowledges that "Micron does not disclose a distinct 'logic element' that receives the input control signals recited in the claim," but argues that it would be obvious to implement such a logic element in the registers of Micron. However, even if these distinct components of a logic element and a register were contained in a single package as proposed, such packaging does not merge or otherwise affect the distinct functions performed by the logic element and the register, so persons of ordinary skill in the art would still consider the logic element and the register to be distinct from one another. (Sechen Decl., ¶ 34.) Furthermore, even if the Micron's register were erroneously considered to be part of a "logic element," Micron still fails to disclose using bank address signals to generate output control signals as required by the '912 patent claims.

The only reason cited by the '0579 Request for Amidi's CPLD to receive bank address signals is bank address conversion.[23] However, there is no disclosure in the prior art, including Micron or Amidi, that teaches or suggests that bank address signals can be used for the type of conversion described by Amidi using row and column addresses. Therefore, the rationale for the modification cannot come from the prior art.

Contrary to the characterization provided by the '0579 Declaration at ¶ 15, the bank address field is not treated in DDR technology in the same way that the row address and column address fields are, as discussed above. (Sechen Decl., ¶ 49.) Because of this known distinction between bank addresses and row/column addresses, persons of ordinary skill in the art would not think of making the leap from Amidi's row/column address conversion to bank address conversion.

Furthermore, as discussed above, this reasoning proposed by the '0579 Request does not explain the claim features recited by Claims 1, 15, and 28 with regard to the logic element receiving at least four signals: at least one row/column address signal, at least two bank address

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[23] The '0579 Declaration at ¶ 21 states that even if the bank address signals are not involved in the conversion, they "can be optionally provided as an input at the discretion of the logic designer." For example, for conversion of DDR-1 memory devices (which all have two bank address bits), the '0579 Declaration at ¶ 26 states that "[a] person of ordinary skill in the art may still choose to route the bank address field of the DDR-1 devices as an input to the conversion logic, but it is not necessary for any purpose" (emphasis added). The Patent Owner submits that if a signal is not being used by a logic element, it makes little sense to route that signal to the logic element. Therefore, this rationale has no "rational underpinning to support the legal conclusion of obviousness" (*KSR* at 418 (quoting *In re Kahn* at 988)) of the claims.

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signals, and at least one chip-select signal. Under the rationale proposed by the '0579 Declaration, if row/column address conversion of the at least one chip-select signal is being performed by Connolly's ASIC (so the DDR memory devices use all the bank address signals received by the memory module), there would be no need for the ASIC to also receive the bank address signals since they are not involved in the conversion. Similarly, if bank address conversion of the at least one chip-select signals is being performed by Connolly's ASIC, there would be no need for the ASIC to also receive the at least one row/column address signal. The claim language recites that both "at least one row/column address signal" and "bank address signals" are received by the logic element. Therefore, at least for this reason, the rationale proposed by the '0579 Request is insufficient, and persons of ordinary skill in the art would not find providing all of these recited signals to Connolly's ASIC, as recited by Claims 1, 15, and 28, to be obvious.

B. **None of the cited prior art discloses or render obvious a "PLL operatively coupled to . . . the logic element" as required by the claims of the '912 patent**

1. **Amidi and Dell 2 (Ground 5)**

As discussed above, Amidi fails to disclose or render obvious a memory module having a PLL device operatively coupled to the logic element, as this requirement would be interpreted by persons of ordinary skill in the art in the context of the '912 patented invention. Dell 2 does not cure the deficiency of Amidi.

Dell 2 does not disclose or suggest using a PLL device, so Dell 2 cannot be relied upon for providing this claim feature missing from Amidi. Therefore, independent Claims 1, 15, 28, and 39 are patentable over the combination of Amidi and Dell 2.

2. **Amidi and JEDEC (Ground 6)**

As discussed above, Amidi does not disclose or render obvious a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. Patent Owner further submits that claims including this recited claim feature are not disclosed or rendered obvious by the combination of Amidi and JEDEC 21-C. While JEDEC 21-C discloses a DIMM having a PLL device operatively coupled to a register (as does Amidi), it does not disclose a logic element, let alone a logic element operatively coupled to the PLL device, so JEDEC 21-C cannot be relied upon for providing this claim feature missing from Amidi.

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Furthermore, while JEDEC 21-C discloses that the DDR memory devices and the register each receive clock signals from the PLL device, JEDEC 21-C does not disclose or suggest using PLL clock signals for a logic element of the DIMM. JEDEC 21-C does provide the guidance that "[t]he most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM" (JEDEC 21-C, p. 74). To achieve this goal, accepted practices in DRAM DIMM design would lead persons of ordinary skill in the art to have Amidi's CPLD timed to the system clock signals, not to the PLL clock signals. (Sechen Decl., ¶ 62.) In contrast, having the logic element timed to the PLL clock signals would be contrary to accepted practices in DRAM DIMM design. (Sechen Decl., ¶ 62.) Therefore, independent Claims 1, 15, 28, and 39 are patentable over the combination of Amidi and JEDEC 21-C.

3. Dell 1 and JEDEC (Ground 9)

As discussed above, JEDEC 21-C does not disclose a PLL device that is operatively coupled to the logic element, as required by the claims of the '912 patent. The combination of Dell 1 and JEDEC 21-C does not disclose or render obvious this requirement as recited by independent Claims 1, 15, 28, and 39. In particular, Dell 1 does not disclose or suggest this claim feature, as acknowledged by the Office Action at p. 29.

Persons of ordinary skill in the art would have Dell 1's ASIC timed to the system clock signals, and would not consider timing the ASIC to the PLL clock signals for various reasons as discussed above. (Sechen Decl., ¶ 65.) To the extent that the Office Action seeks to define the term "logic element" to be a conceptual construct that encompasses both the ASIC of Dell 1 and the register of JEDEC 21-C, Patent Owner traverses this interpretation for at least the same reasons discussed above. Furthermore, as discussed above, a POSITA would not have combined the EDO technology of Dell 1 with the DDR technology of JEDEC. Therefore, independent Claims 1, 15, 28, and 39 which include this recited claim feature are not disclosed or rendered obvious by the combination of Dell 1 and JEDEC 21-C.

4. Wong and JEDEC (Ground 11)

As discussed above, JEDEC 21-C does not disclose a PLL device that is operatively coupled to the logic element, as required by the claims of the '912 patent. The combination of Wong and JEDEC 21-C does not disclose or render obvious this requirement as recited by independent Claims 1, 15, 28, and 39. In particular, Wong does not disclose or suggest this claim feature, as acknowledged by the Office Action at p. 36.

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Persons of ordinary skill in the art would have Wong's control circuit timed to the system clock signals, and would not consider timing the control circuit to the PLL clock signals for various reasons as discussed above. (Sechen Decl., ¶ 66.) To the extent that the Office Action seeks to define the term "logic element" to be a conceptual construct that encompasses both the control circuit of Wong and the register of JEDEC 21-C, Patent Owner traverses this interpretation for at least the same reasons discussed above. Furthermore, as discussed above, a POSITA would not have combined the EDO technology of Wong with the DDR technology of JEDEC. Therefore, independent Claims 1, 15, 28, and 39 which include this recited claim feature are not disclosed or rendered obvious by the combination of Wong and JEDEC 21-C.

5.   Micron and Connolly (Ground 12)

Neither Micron nor Connolly individually, nor in combination, disclose or render obvious a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39.

Connolly makes no mention of a PLL device, and Micron does not disclose or suggest this claim feature, contrary to the assertion in the Office Action at p. 42. To the extent that the Office Action seeks to define the term "logic element" to be Micron's register or to be a conceptual construct that encompasses both the ASIC of Connolly and Micron's register, the Patent Owner traverses this interpretation for at least the same reasons discussed above. While Micron discloses a DIMM having a PLL device operatively coupled to a register, persons of ordinary skill would not interpret Micron's register as being a "logic element," so Micron does not include a PLL device operatively coupled to the logic element.

Furthermore, while Micron discloses that the DDR memory devices and the register each receive clock signals from the PLL device, Micron does not disclose or suggest using PLL clock signals for a logic element of the DIMM. In fact, contrary to the assertion made by the '0579 Request at p. G-12 that it would be obvious to persons of ordinary skill in the art to operatively coupling the PLL device to the logic element,[24] as discussed above, persons of ordinary skill in the art would have Connolly's ASIC timed to the system clock signals, and would not consider timing it to the PLL clock signals for various reasons. (Sechen Decl., ¶ 68.) Therefore,

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[24] While the '0579 Request cites the '0579 Declaration at ¶¶ 13-14 for this proposition, the '0579 Declaration provides no such support.

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independent Claims 1, 15, 28, and 39 which include this recited claim feature are not disclosed or rendered obvious by the combination of Micron and Connolly.

6.   Micron and Amidi (Ground 13)

As discussed above, neither Micron nor Amidi individually disclose or render obvious a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. The Patent Owner further submits that claims including this recited claim feature are not disclosed or rendered obvious by the combination of Micron and Amidi. While Micron discloses an RDIMM having a PLL device operatively coupled to a register (as does Amidi), it does not disclose a logic element, let alone a logic element operatively coupled to the PLL device.

Furthermore, while Micron discloses that the DDR memory devices and the register each receive clock signals from the PLL device, Micron does not disclose or suggest using PLL clock signals for a logic element of the DIMM. In fact, contrary to the assertion made by the '0579 Request at p. H-12 that it would be obvious to persons of ordinary skill in the art to operatively coupling the PLL device to the logic element,[25] as discussed above, there are multiple reasons that persons of ordinary skill would not make the proposed modification. Therefore, persons of ordinary skill in the art would not have been prompted to make the proposed modification of Micron or Amidi to produce the claimed invention, so independent Claims 1, 15, 28, and 39 which include this recited claim feature are not disclosed or rendered obvious by the combination of Micron and Amidi.

For at least the foregoing reasons, Patent Owner respectfully submits each of the grounds of rejection against independent claims 1, 15, 28 and 39 are overcome. Accordingly, each of these independent claims and the remaining pending dependent claims are patentable over the cited prior art of record.

V.   The Cited Prior Art Fails to Disclose Various Features of the Dependent Claims

In addition to the reasons discussed above with respect to the independent claims, the dependent claims recite various limitations which are also not anticipated or rendered obvious by the cited prior art. Examples of such various limitations are discussed below.

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[25] While the '0579 Request cites the '0579 Declaration at ¶¶ 13-14 for this proposition, the '0579 Declaration provides no such support.

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A.   None of the cited prior art discloses *signals received during row access subsequently used during column access*

Claim 21 recites that the circuit "is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure."[26] Also, each of new Claims 94-101 and 106-108 addresses the logic element receiving one or more bits or signals in conjunction with an activate command and using the bits or signals to generate rank-selecting signals during a subsequent read or write command.

1.   Amidi (Grounds 3 and 4)

The '0578 Request at pp. 1117-1118 cites Amidi at ¶ 61, the '1339 Request (e.g., at pp. 105-106) cites to Amidi at ¶¶ 37, 38, 50, and 57, and the Office Action points to register 608 in Figs. 6A and 6B of Amidi as disclosing this claim feature. However, these paragraphs and figures merely disclose conventional row access and subsequent column access for DDR memory in which the address and control signals for column access are independently provided by the computer system from those of row access. (Sechen Decl., ¶ 70.) While the register does temporarily store and transmit certain signals "to synchronize the incoming address and control signals with respect to differential clock signals" (Amidi, ¶ 38), the storage does not take place during a row access procedure with use occurring during a column access procedure. (Sechen Decl., ¶ 70.) Persons of ordinary skill in the art would not interpret such conventional operations of the register as somehow storing or buffering a signal received during a row access procedure for subsequent use to the DDR memory devices during a column access procedure. (Sechen Decl., ¶ 70.) Therefore, persons of ordinary skill in the art would not read Amidi as disclosing or rendering obvious such features, so these claims are not anticipated or rendered obvious by Amidi.

Furthermore, it would not be obvious to persons of ordinary skill in the art to modify Amidi to provide such claim features. Amidi does not provide a rationale for such a feature, and regarding the other cited references, either they do not disclose or suggest such a feature, or as discussed more fully below, persons of ordinary skill in the art would not be aware of a rationale to modify Amidi to provide such a feature.

2.   Amidi and Dell 2 (Ground 5)

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[26] While the '0578 Request and the '1339 Request proposed rejecting Claim 21, the Office Action at pp.17-18 and 20-22 explicitly declined to do so.

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As discussed above, Amidi does not disclose or suggest a circuit "configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure," as recited in original dependent claim 21 and new dependent new claims 94-101 and 106-108. Furthermore, persons of ordinary skill in the art would not be aware of a rationale to modify Amidi to include this feature. Dell 2 at col. 8, ll. 29-41 discloses that the highest order row address bit is received and reassigned to become a bank address bit at RAS time, and this reassigned bank address bit is stored to be re-sent at CAS time as well "to ensure that the correct bank is addressed." In contrast, Amidi receives the full bank address from the computer system during both RAS and CAS time, and Amidi provides it to the memory devices via the register (see, Amidi, ¶¶ 50, 58, Figs. 6A, 6B) without needing any bits stored from a previous operation. Therefore, as disclosed by Amidi, there is no reason to store the reassigned bank address bit during RAS time or to re-send it during CAS time as disclosed by Dell 2. (Sechen Decl., ¶ 73.)

Furthermore, as noted by the Office Action at p. 24, "[b]ank address signals are not re-mapped in Amidi's memory module" and the '1339 Request "does not make it clear how this teaching can be combined with Amidi" and fails to provide "any guidance as to how the teachings from the two references are to be combined to result in a memory module that discloses all of the limitations of claim 21." In addition, while the '1339 Request at p. 164 cites this disclosure of Dell 2 for this feature, it does not cite any rationale for why persons of ordinary skill in the art would modify Amidi to include this feature and increase the cost of the system. As explained by M.P.E.P. § 2141, "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (citing *KSR* at 418). Therefore, a sufficient case of obviousness has not been presented.

3.   Amidi and JEDEC (Ground 6)

As discussed above, Amidi does not disclose or suggest a circuit "configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure," as recited in original dependent claim 21 and new dependent new claims 94-101 and 106-108. Furthermore, persons of ordinary skill in the art would not be aware of a rationale to modify Amidi or JEDEC 21-C to include this feature. Both Amidi and JEDEC 21-C disclose conventional row access and subsequent column access for DDR memory in which the address and control signals for column access are independently provided from those for row

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access. (Sechen Decl., ¶ 74.) Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing or buffering a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure. (Sechen Decl., ¶ 74.) Therefore, neither Amidi nor JEDEC 21-C discloses or suggests this claim feature.

4.   Dell 1 and JEDEC (Ground 9)

As discussed above JEDEC 21-C fails to disclose or suggest a circuit "configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure," as recited in original dependent claim 21 and new dependent new claims 94-101 and 106-108. Dell 1 does not cure the deficiency of JEDEC 21-C.

Dell 1 discloses a conversion of a row address bit into a RAS signal, but does not disclose or suggest storing or buffering a signal for use during a subsequent column access procedure. (Sechen Decl., ¶ 77.) Therefore, neither Dell 1 nor JEDEC 21-C discloses or suggests this claim feature.

5.   Wong and JEDEC (Ground 11)

Wong does not disclose or suggest this claim feature, and as discussed above, neither does JEDEC 21-C. Wong discloses a conversion of a row address bit into a RAS signal, but does not disclose or suggest storing or buffering a signal for use during a subsequent column access procedure. (Sechen Decl., ¶ 78.) Therefore, neither Wong nor JEDEC 21-C discloses or suggests this claim feature.

6.   Micron and Connolly (Ground 12)

Neither Micron nor Connolly discloses or suggests a circuit "configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure," as recited in original dependent claim 21 and new dependent new claims 94-101 and 106-108. Micron discloses conventional row access and subsequent column access for DDR memory, in which the address and control signals for column access are independently provided from those for row access. Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing or buffering a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure. (Sechen Decl., ¶ 79.) Therefore, this claim feature is not disclosed or suggested by Micron.

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This claim feature is also not disclosed or suggested by Connolly, or by the combination of Micron and Connolly. The '0579 Request cites Connolly's Fig. 7 as disclosing that the SYS RAS signal is stored during a row access procedure for subsequent use during a column access procedure. The Office Action at p. 47 appears to adopt this rationale by stating that "SYS RAS stored in 90 is used to generate CAS L and CAS R." However, as acknowledged by the '0579 Request at p. G-29, latching of SYS RAS only occurs by "SYS_CAS going active (which will cause SYS_RAS to be latched)." Thus, Connolly's ASIC latches the SYS RAS signal when SYS CAS becomes activated (see, Connolly at col. 11, ll. 5-6). In a read/write operation, upon SYS CAS going active, the row access procedure is ended, and the subsequent column access procedure has begun. (Sechen Decl., ¶ 80.) Therefore, Connolly's ASIC does not store the SYS RAS during the row access procedure, so Connolly's treatment of the SYS RAS signal does not satisfy the claim feature of storing the input signal during a row access procedure for subsequent use during a column access procedure.

The '0579 Request also cites Connolly at col. 5, ll. 50-52 and Fig. 4 as disclosing that the address bit A11 is latched during a row access procedure so that "the address bit is A11 is freed and not required to stay in its state during the entire operation." However, while Connolly discloses latching and using the value of A11 to determine whether to make RAS A or RAS B active during a row access procedure, Connolly does not disclose or suggest that this latched address bit is used during a subsequent column access procedure. Therefore, Connolly's treatment of the address bit A11 also does not satisfy the claim feature of storing the input signal during a row access procedure for subsequent use during a column access procedure.

Even if one erroneously assumes it would be obvious to modify Micron and Connolly to utilize bank address decoding rather than row or address decoding, such a modification would not result in Connolly's ASIC storing a signal received during row access for use during column access. Bank address signals are received by the memory module in conjunction with both row access and column access, so there is no need to store the bank address signal from the row access procedure for use during the column access procedure. At least for this reason, claims reciting this feature are not obvious in view of the combination of Micron and Connolly.

7.   Micron and Amidi (Ground 13)

As discussed above, neither Micron nor Amidi individually disclose or suggest this claim feature. Furthermore, persons of ordinary skill in the art would not be aware of a rationale to

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modify Micron or Amidi to include this feature. Both Micron and Amidi disclose conventional row access and subsequent column access for DDR memory in which the address and control signals for column access are independently provided from those for row access. (Sechen Decl., ¶ 76.) Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing or buffering a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure. (Sechen Decl., ¶ 76.) Therefore, neither Micron nor Amidi, nor their combination, discloses or suggests this claim feature.

Even if one erroneously assumed it would be obvious to modify Amidi to utilize bank address decoding rather than row or address decoding, such a modification would not result in Amidi's CPLD storing a signal received during row access for use during column access. Bank address signals are received by the memory module in conjunction with both row access and column access, so there is no need to store the bank address signal from the row access procedure for use during the column access procedure. At least for this reason, claims reciting this feature are not obvious in view of the combination of Micron and Amidi.

B. **None of the cited prior art discloses *SPD device data characterizing the memory module as having different attributes***

Each of new Claims 56, 60-63, 75, 80, 81, 85, 86, 90, 91, and 109-111 addresses the memory module storing data characterizing the plurality of DDR memory devices as having attributes that it does not actually have. As described by the '912 patent at col. 9, ll. 24-37, the plurality of DDR memory devices of conventional memory modules have various attributes, and data characterizing these attributes is stored in non-volatile memory (e.g., a serial-presence detect (SPD) device) which are communicated to the BIOS of the computer system so the memory controller can use this data to send appropriate address, control, and command signals to operate the DDR memory devices correctly. In certain embodiments of the claimed invention, instead of characterizing the actual, physical attributes of the plurality of DDR memory devices, the stored data characterizes attributes of the "logical" plurality of DDR memory devices (see, e.g., the '912 patent at col. 11, ll. 36-38). Persons skilled in the art would understand that the "attributes" of the plurality of DDR memory devices (see, e.g., Claim 56) are the physical attributes that the plurality of DDR memory devices actually has, and would understand that the stored data characterizes the plurality of DDR memory devices as having different attributes, and it is these

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different attributes, not the actual, physical attributes, which are communicated to the computer system.

1.   Amidi (Grounds 3 and 4)

While Amidi discloses a memory module having an SPD device that is a "simple I2C interface EEPROM to hold information regarding memory module for BIOS during the power-up sequence" (see, e.g., Amidi, ¶ 40), nowhere does Amidi disclose or render obvious that the data stored by the SPD device characterizes the plurality of DDR memory devices as having attributes different from its actual, physical attributes. Therefore, these claims are not anticipated or rendered obvious by Amidi.

2.   Amidi and Dell 2 (Ground 5)

As discussed above, Amidi does not disclose or suggest this claim feature. Furthermore, Dell 2 does not disclose or suggest this feature, either alone or in combination with Amidi, so these claims would not be obvious to persons of ordinary skill in the art. Dell 2 at col. 6, l. 66 – col. 7, l. 13 discloses a negotiation process between the system controller and the memory module in which the system controller reads presence detect (PD) data from an EEPROM of the memory module and the module's ASIC logic device stores updated PD data in volatile memory. Dell 2 at col. 7, ll. 15-17 explains that "modified or requested PD data will not be written to the EEPROM 30 because it is desirable not to lose the original PD data therein."[27] For the system of Dell 2 to operate as disclosed, it utilizes the original PD from the EEPROM to determine "whether the initial operating modes and functions of the memory module 20 are compatible with system level requirements" (Dell 2 at col. 9, ll. 5-11 and Fig. 2). Thus, the EEPROM must contain PD data corresponding to the actual memory module, not "data [that] characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices," as recited by Claim 56, for example. Therefore, claims reciting this feature are patentable over Amidi in view of Dell 2.

3.   Amidi and JEDEC (Ground 6)

As discussed above, Amidi does not disclose or suggest this claim feature. Furthermore, JEDEC 21-C does not disclose or suggest this feature, either alone or in combination with Amidi,

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[27] While Dell 2 contemplates writing the modified PD data to non-volatile memory, such writable memory is necessarily not "read-only" as recited by the relevant claims of the '912 patent.

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so these claims would not be obvious to persons of ordinary skill in the art. While JEDEC 21-C discloses a serial presence detect (SPD) device, it does not disclose or suggest that the data stored by the SPD device is anything except a characterization of the actual, physical attributes of the plurality of DDR memory devices of the DIMM. In fact, to have the data characterize the plurality of DDR memory devices as having any attributes different from its actual attributes would likely cause fatal errors when the computer's memory controller attempts to access the memory module, making the memory module disclosed by JEDEC 21-C inoperative for its intended purpose. Therefore, claims reciting this feature are patentable over Amidi in view of JEDEC 21-C.

4.   Dell 1 and JEDEC (Ground 9)

Dell 1 does not disclose an SPD device, so it does not disclose or suggest this claim feature. Furthermore, as discussed above, JEDEC 21-C also does not disclose or suggest this feature, so these claims would not be obvious to persons of ordinary skill in the art. Therefore, claims reciting this feature are patentable over Dell 1 in view of JEDEC 21-C.

5.   Wong and JEDEC (Ground 11)

Wong does not disclose an SPD device, so it does not disclose or suggest this claim feature. Furthermore, as discussed above, JEDEC 21-C also does not disclose or suggest this feature, so these claims would not be obvious to persons of ordinary skill in the art. Therefore, claims reciting this feature are patentable over Wong in view of JEDEC 21-C.

6.   Micron and Connolly (Ground 12)

Connolly does not disclose an SPD device, so it does not disclose or suggest this claim feature. While Micron discloses a serial presence detect (SPD) device, it does not disclose or suggest that the data stored by the SPD device is anything except a characterization of the actual attributes of the plurality of DDR memory devices of the DIMM. In fact, to have the data characterize the plurality of DDR memory devices as having any attributes different from its actual attributes would likely cause fatal errors when the computer's memory controller attempts to access the memory module, making the memory module disclosed by Micron inoperative for its intended purpose. Therefore, claims reciting this feature are patentable over Micron in view of Connolly.

7.   Micron and Amidi (Ground 13)

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As discussed above, Amidi does not disclose or suggest this claim feature. Furthermore, Micron does not disclose or suggest this feature, either alone or in combination with Amidi, so these claims would not be obvious to persons of ordinary skill in the art. While Micron discloses a serial presence detect (SPD) device, it does not disclose or suggest that the data stored by the SPD device is anything except a characterization of the actual, physical attributes of the plurality of DDR memory devices of the DIMM. In fact, to have the data characterize the plurality of DDR memory devices as having any attributes different from its actual attributes would likely cause fatal errors when the computer's memory controller attempts to access the memory module, making the memory module disclosed by Micron inoperative for its intended purpose. Therefore, claims reciting this feature are patentable over Micron in view of Amidi.

C.   **None of the cited prior art discloses or enables** *successive or back-to-back adjacent read commands from different DDR devices*

New Claims 64, 69, 102, and 103 address the memory module performing "successive read accesses from different ranks of DDR memory devices" and each of new Claims 65, 70, 78, 83, 88, 104, and 105 address the memory module performing "back-to-back adjacent read commands which cross DDR memory device boundaries."

1.   **Amidi (Grounds 3 and 4)**

Amidi does not disclose or render obvious a memory module that is capable of performing "successive read accesses from different ranks of DDR memory devices" or "back-to-back adjacent read commands which cross DDR memory device boundaries." In fact, as discussed in detail below, the disclosure of Amidi does not address the issue of successive or adjacent read commands at all and it does not disclose a system which can correctly handle such command sequences. Therefore, these claims are not anticipated or rendered obvious by Amidi.

With regard to row address decoding, Amidi discloses that its CPLD receives some of the input control signals from the computer system, namely, chip-select signals (cs0, cs1), address bit Add(n), and command signal bits (CAS, RAS, WE). Amidi further discloses that its register receives some of the input control signals, namely, address bits Add[n-1:0], command signal bits (RAS, CAS, WE), and bank address bits BA[1:0] (Amidi at ¶ 50, Figs. 6A, 6B). Note that Amidi does not disclose that the CPLD 604 receives the bank address bits BA[1:0].

As a result, the memory module disclosed by Amidi and shown by Figure 6A will not be able to correctly control the various ranks of DDR memory devices under circumstances that

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must be handled by an operational DDR memory module. Because the CPLD does not receive the bank address bits BA[1:0], the CPLD will not have enough information to know what chip-select signals to generate for successive or adjacent read accesses and/or write accesses. (Sechen Decl., ¶ 92.) For example, to perform a read operation from the DDR memory devices of a memory module, an activate command signal is first issued to activate the bank and row identified by the bank address and the row address, respectively, along with the appropriate chip-select signal to select the rank containing the bank and row to be activated. (Sechen Decl., ¶ 92.) During row address decoding as disclosed by Amidi at Fig. 6A and ¶¶ 49-52, to issue the activate command signal, the CPLD receives the row address bit Add(n) (e.g., A12) and the chip-select signals (cs0, cs1), and outputs the corresponding chip-select signals (rcs0, rcs1, rcs2, rcs3) according to the truth table of Fig. 5. The chip-select signals from the CPLD are sent to the DDR memory devices so that only the identified bank and row for the selected rank are activated. (Sechen Decl., ¶ 92.)

To complete the read operation, a read command signal must also be issued separately to the DDR memory devices sometime after the activate command signal. (Sechen Decl., ¶ 93.) For this read command signal, the column address signal is provided by the computer system to identify the column of the activated bank and row from which the data is to be read. (Sechen Decl., ¶ 93.) However, the correct physical rank has to be selected by the read command signal as well. (Sechen Decl., ¶ 93.) For DDR memory, the activate command signal does not have to immediately precede the subsequent corresponding read command signal. In addition, there can be multiple ranks that have activated banks at any given time, each activated by an activate command which activates one bank and one row for one selected rank. (Sechen Decl., ¶ 93.) As a result, there can be intervening activate command signals and/or other command signals corresponding to other banks and rows of the DDR memory devices between a particular activate command signal and its corresponding read command signal. For example, there will concurrently be multiple physical ranks with active banks and two or more of the read access commands that complete the read operation from these ranks will follow one another (e.g., successive read accesses from different ranks of DDR memory devices or back-to-back adjacent read commands which cross DDR memory device boundaries). (Sechen Decl., ¶ 94.) An operational memory module comprising DDR memory devices is required to be able to handle such circumstances. (Sechen Decl., ¶ 94.)

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Each of these read command signals needs to identify which physical rank is to be read by including the appropriate chip-select signal in the read command signal. (Sechen Decl., ¶ 95.) In conventional memory modules, it is a simple matter to do so since the appropriate chip-select signal is provided by the computer system. In this way, regardless of any intervening command signals, the read command signal is able to read data from the appropriate column of the previously-activated bank and row. (Sechen Decl., ¶ 95.)

However, in Amidi's memory module, the appropriate chip-select signals are supposed to be generated by the CPLD. But the read command signal does not include the row address bit needed for the CPLD to determine the correct physical rank to be selected, since this address bit is only available in the row address, not in the column address. (Sechen Decl., ¶ 96.) In particular, while the needed address bit Add(n) (e.g., A12) is provided by the computer system with the activate command signal, it is <u>not</u> provided by the computer system with the read command signal. (Sechen Decl., ¶ 96.) The CPLD disclosed by Amidi cannot generate the chip-select signals for the read command signal to appropriately correspond to the previously-activated bank and row. (Sechen Decl., ¶ 96.) Therefore, the system disclosed by Amidi would not work for its intended purpose of providing an operable and reliable DDR memory module. (Sechen Decl., ¶ 96.) In particular, the system disclosed by Amidi will not properly perform "successive read accesses from different ranks of DDR memory devices" or "back-to-back adjacent read commands which cross DDR memory device boundaries."

In contrast, these command sequences are described in the '912 patent, along with a DDR memory module that is able to correctly handle such command sequences. In the DDR memory module of the '912 patent, the logic element 40 receives the bank address signals (e.g., BA_0-BA_m) from the computer system (see, Figure 1A and col. 7, ll. 35-53), particularly both during activate commands and during read/write commands. (Sechen Decl., ¶ 97.) As a result, the logic element 40 has all the necessary information to generate the appropriate chip-select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) for use with both the activate command signal and the read/write command signal. (Sechen Decl., ¶ 97.) For example, for row address decoding, the '912 patent discloses that the logic element 40 receives the row address bit (A_{n+1}), the chip-select signals (CS_0, CS_1), and bank address signals (e.g., BA_0-BA_m) (see, the '912 patent at Figure 1A and col. 7, ll. 35-53). For the activate command signal, the logic element 40 generates the appropriate chip-select signals in response to the input chip-select signals (CS_0, CS_1), the row address bit

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(A_{n+1}), and the command signal (e.g., using the logic table of Table 1 of the '912 patent). For the read command signal, the logic element latches the value of the row address bit during the activate command for the selected bank (see, the '912 patent at col. 9, ll. 18-21). Thus, by using the "one-to-one-to-one" correspondence between an activated bank, an activated row, and the selected logical rank, the logic element of the '912 patent is able to generate the appropriate chip-select signal for the read command signal to correspond to the previously-activated bank and row using the bank address signals from both the activate command and from the read access command. (Sechen Decl., ¶ 97.) Thus, the memory module disclosed and claimed by the '912 patent will not suffer from the problem of missing information of Amidi's memory module. (Sechen Decl., ¶ 97.)

None of the cited references, including Amidi, discloses or suggests the underlying problem with Amidi's disclosed system. Furthermore, identification of the problem, as well as identifying and implementing its solution, would be outside the knowledge, experience, and capabilities of persons of ordinary skill in the art. (Sechen Decl., ¶ 98.) The statements made by the Requesters that such a solution is obvious are without factual support and are merely improper exercises in hindsight, based on the '912 patent disclosure. Nowhere does the prior art point to such a solution, and as described in (Sechen Decl., ¶ 98), such a solution would be outside the knowledge and abilities of persons of ordinary skill in the art. Therefore, Amidi's disclosure is not enabling for the subject matter of the claims of the '912 patent, and the solution to this lack of enablement and its implementation would not be obvious to persons of ordinary skill in the art. In particular, Amidi does not disclose or render obvious a DDR memory module as recited in claims that recite this feature.

2. Amidi and Dell 2 (Ground 5)

As discussed above, Amidi does not disclose or render obvious a memory module that is capable of performing such operations. Furthermore, Dell 2 also does not disclose or render obvious, either alone or in combination with Amidi, a memory module that is capable of performing such operations. Therefore, these claims are not rendered obvious by Amidi in view of Dell 2.

3. Amidi and JEDEC (Ground 6)

As discussed above, Amidi does not disclose or render obvious a memory module that is capable of performing such operations. The memory module of JEDEC 21-C presumably is

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capable of performing such operations, since it is expected of standard DDR memory modules. (Sechen Decl., ¶ 99.) However, the prior art and the knowledge of persons of ordinary skill in the art do not provide enabling guidance to persons or ordinary skill in the art regarding how to perform such operations upon combining the teachings of Amidi and JEDEC 21-C. (Sechen Decl., ¶ 99.) The combination of Amidi and JEDEC 21-C certainly does not disclose or suggest the techniques disclosed by the '912 patent. Therefore, these claims are not rendered obvious by Amidi in view of JEDEC 21-C.

4.   Dell 1 and JEDEC (Ground 9)

Dell 1 does not disclose or render obvious a memory module that is capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands. (Sechen Decl., ¶ 101.) The memory module of JEDEC 21-C presumably is capable of performing such operations, since it is expected of standard DDR memory modules. However, the prior art and the knowledge of persons of ordinary skill in the art do not provide enabling guidance to persons of ordinary skill in the art regarding how to perform such operations upon combining the teachings of Dell 1 and JEDEC 21-C. (Sechen Decl., ¶ 101.) The combination of Dell 1 and JEDEC 21-C certainly does not disclose or suggest the techniques disclosed by the '912 patent. Therefore, these claims are not rendered obvious by Dell 1 in view of JEDEC 21-C.

5.   Wong and JEDEC (Ground 11)

Wong does not disclose or render obvious a memory module that is capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands. (Sechen Decl., ¶ 102.) The memory module of JEDEC 21-C presumably is capable of performing such operations, since it is expected of standard DDR memory modules. However, the prior art and the knowledge of persons of ordinary skill in the art do not provide enabling guidance to persons of ordinary skill in the art regarding how to perform such operations upon combining the teachings of Wong and JEDEC 21-C. (Sechen Decl., ¶ 102.) The combination of Wong and JEDEC 21-C certainly does

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not disclose or suggest the techniques disclosed by the '912 patent. Therefore, these claims are not rendered obvious by Wong in view of JEDEC 21-C.

6.   Micron and Connolly (Ground 12)

Connolly does not disclose or render obvious a memory module that is capable of performing such operations since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands, so it is not capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices. (Sechen Decl., ¶ 103.) The memory module of Micron presumably is capable of performing such operations, since it is expected of standard DDR memory modules. However, the prior art and the knowledge of persons of ordinary skill in the art do not provide enabling guidance to persons of ordinary skill in the art regarding how to perform such operations upon combining the teachings of Micron and Connolly. (Sechen Decl., ¶ 103.) The combination of Micron and Connolly certainly does not disclose or suggest the techniques disclosed by the '912 patent. Therefore, claims reciting this feature are not rendered obvious by Micron in view of Connolly.

7.   Micron and Amidi (Ground 13)

As discussed above, Amidi does not disclose or render obvious a memory module that is capable of performing such operations.   The memory module of Micron presumably is presumably capable of performing such operations, since it is expected of standard DDR memory modules. However, the prior art and the knowledge of persons of ordinary skill in the art do not provide enabling guidance to persons of ordinary skill in the art regarding how to perform such operations upon combining the teachings of Micron and Amidi. (Sechen Decl., ¶ 100.) The combination of Micron and Amidi certainly does not disclose or suggest the techniques disclosed by the '912 patent. Therefore, these claims are not rendered obvious by Micron in view of Amidi.

VI.   Patent Owner does not Acquiesce to Issues not Discussed Above

In this Response, Patent Owner respectfully traverses the characterizations of the '912 patent (including but not limited to its claims, prosecution history, support found in the priority documents, and examiner's reasons for allowance) and the cited references made in the '1339 Request, the '0578 Request, and the '0579 Request, including in any appendices, exhibits,

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declarations, or claim charts submitted with these Requests, as well as in the Office Action. However, for the sake of brevity, Patent Owner has omitted a point-by-point rebuttal and has focused attention on claim features that are not disclosed or rendered obvious by the cited references. The decision to not directly address in this Response any specific points made in the Requests or in the Office Action regarding these rejections does not indicate that Patent Owner agrees with or acquiesces to these specific points.

Patent Owner discusses above only some of the claim features of the '912 patent for the sake of brevity in this Response. These discussions should not be interpreted as Patent Owner asserting or acquiescing that the claims are not disclosed or rendered obvious because of only these features. Furthermore, Patent Owner submits that when ascertaining the differences between the prior art and the claims at issue, the obviousness analysis must not be constrained to merely these differences themselves, but must consider "whether the claimed invention as a whole would have been obvious" (M.P.E.P. § 2141.02 (emphasis in original)).

In addition, Patent Owner discusses various claims in the sections above in groups for the sake of brevity. These discussions should not be interpreted as Patent Owner asserting or acquiescing that these grouped claims should rise or fall together, that the recitations of one or more claims of a group should be interpreted to affect the interpretation of other claims of the group, or that the paraphrased description of the group's recitation provided above should be read as somehow affecting the interpretation of the claims. Instead, the patentability of each of these claims individually depends on whether its language, including that of the claims from which it depends, using its broadest reasonable interpretation in light of the specification as it would be interpreted by one of ordinary skill in the art, would be patentable over the prior art.

Patent Owner also respectfully disagrees with any claim construction of the Office Action to the extent that it reads the claim terms in a manner that is not reasonably consistent with the specification or that is different from how they would be read in light of the specification as it would be interpreted by persons of ordinary skill in the art. Patent Owner reserves the right to clarify the appropriate interpretation of these and other claim terms under the appropriate legal standards in this reexamination or any subsequent reexamination and/or litigation proceedings.

Finally, Patent Owner notes that the obviousness analysis is a separate inquiry from that of anticipation and a *prima facie* case of obviousness requires that each of the *Graham* factors be addressed, rather than mere conclusory statements that because claims are anticipated, they are

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necessarily obvious.[28] In some instances, the Examiner appears to summarily conclude that a claim is obvious if anticipated. For example, the Office Action at p. 22 states that "[w]ith respect to claims 1-15, 18-22 [*sic*], 23-25, 27-34, 36-43, 45-48, 50, and 51, see the rejection of these claims [as obvious in view of Amidi] above." However, the asserted basis for the obviousness rejections of Claims 1-15, 18-20, 22-25, 27-34, 36-45, 47, 48, 50, and 51 in view of Amidi is "[b]ecause these claims are anticipated by Amidi, they are necessarily obvious over Amidi" (Office Action at p. 21). Therefore, the rejections of Claims 1-15, 18-20, 23-25, 27-34, 36-43, 45-48, 50, and 51 as being obvious in view of Amidi and Dell 2, and similar conclusions of obviousness with respect to other combinations, are insufficient since they are not based on an analysis of each of the *Graham* factors, as required, to provide factual support for a proper *prima facie* conclusion of obviousness.

VII.   Information Disclosure Statement

Submitted concurrently herewith is an Information Disclosure Statement citing new references. While Patent Owner does not believe that these references will affect the patentability of the pending claims, Patent Owner respectfully requests the Examiner to consider the pending claims in connection with these references in order to make them of record.

VIII.   Co-Pending Applications and Reexaminations of Assignee

Patent Owner notes that each of the following pending U.S. patent applications and the U.S. patents under the following reexaminations claims a priority benefit to one or more U.S. patent applications in the priority claim of the '912 patent. Patent Owner further notes that other co-pending applications are listed in the Information Disclosure Statement.

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[28] See, *Cohesive Technologies, Inc. v. Waters Corp.*, 543 F.3d 1351, 1363 (Fed. Cir. 2008)("Despite the often quoted maxim that anticipation is the 'epitome of obviousness ...', novelty under 35 U.S.C. § 102 and non-obviousness under 35 U.S.C. § 103 are separate conditions of patentability.") (citations omitted). Under a proper obviousness analysis, the factors of *Graham v. John Deere Co.*, 383 U.S. 1 (1966) must be assessed: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) the secondary considerations. M.P.E.P. § 2141 provides guidance for such a proper obviousness analysis in view of KSR *Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007). Proper rejections on obviousness "cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (*In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

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Appl. No.	Filing Date	Attorney Docket No.	Title
13/154,172	06/06/2011	NETL.018P1C5	Circuit for Providing Chip-Select Signals to a Plurality of Ranks of a DDR Memory Module
13/032,470	02/22/2011	NETL.018P2C5	Circuit for Memory Module
12/912,623	10/26/2010	NETL.018CPCCC2	Memory Module Decoder
95/000,546; 95/000,577	05/11/2010; 10/20/2010	NETL.018RX4; NETL.018RX5	*Inter Partes* Reexamination of U.S. Pat. No. 7,289,386
95/001,381	06/09/2010	NETL.018RX2	*Inter Partes* Reexamination of U.S. Pat. No. 7,532,537
95/001,337	06/04/2010	NETL.018RX3	*Inter Partes* Reexamination of U.S. Pat. No. 7,636,274

Patent Owner notes that cited references, office actions, responses and notices of allowance currently exist or will exist for the above-referenced matters. Patent Owner also understands that the Examiner has access to sophisticated online Patent Office computing systems that provide ready access to, for example, specification and drawing publications, pending claims and complete file histories, including, for example, cited art, office actions, responses, and notices of allowance.

XIV. Conclusion

The foregoing compels the conclusion that rejected Claims 1-51 are patentable over the prior art. Furthermore, new Claims 52-118 are also patentable over the prior art. Patent Owner should not be deemed to have acquiesced in any factual or legal conclusion in connection with any issues by such issue not having been specifically addressed herein.
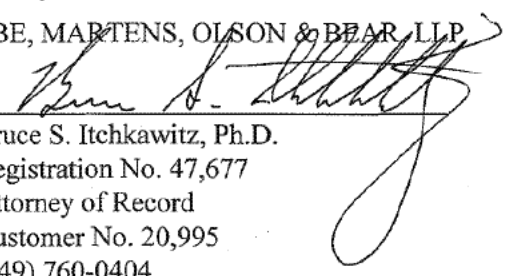
In view of the foregoing, Patent Owner respectfully requests that Claims 1-118 be allowed.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: ___7/5/11___   By: _____

Bruce S. Itchkawitz, Ph.D.
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

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Page 1   Lee Declaration

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Netlist, Inc.

Inter Partes Reexamination Proceeding

Control Nos. 95/000,578, 95/000,579, 95/001,339

Filed: October 20, 2010, October 21, 2010, June 8, 2010

For: U.S. Patent No. 7,619,912

DECLARATION OF HYUN LEE, PH.D.

I, Hyun Lee, Ph.D., declare that:

1. I am currently employed as Vice President, Chief Technical Officer, and Acting Vice President of Research and Development at Netlist, Inc. As a result of my position and responsibilities at Netlist, I have a detailed understanding of Netlist's HyperCloud™ series of memory modules, their capabilities and the technical basis for these capabilities, and their uses by our customers. Attached as Tab HL-A is a true and accurate copy of my curriculum vitae.

2. Netlist is a publicly-traded company on the Nasdaq exchange, and is the owner of U.S. Patent No. 7,619,912 ("the '912 patent"), currently the subject of the above-identified *inter partes* reexamination proceeding. I have no financial interest in the '912 patent, beyond owning stock in Netlist. As an employee of Netlist, I receive a salary from Netlist, but this salary is not dependent on the outcome of the above-identified *inter partes* reexamination proceeding. In addition, I do not receive any royalties, bonuses, or other types of compensation based on the outcome of the above-identified *inter partes* reexamination proceeding.

3. I have been asked by Netlist to provide this declaration to explain the connection between various capabilities of Netlist's HyperCloud™ series of memory modules that our customers have found valuable and the claimed invention of the '912 patent.

4. I have reviewed the '912 patent, including its claims as issued, as well as the new claims being submitted in the Response to the April 4, 2011 Office Action being filed in the above-captioned *inter partes* reexamination proceeding.

5. Attached to this declaration are the following documents:

    - **Tab HL-B**: "HyperCloud™ 8GB & 16GB DDR3 RDIMMs," Netlist, Inc., 2010, product brief.

    - **Tab HL-C**: "3-to-1 VMs-per-Server Ratio Improvement with HyperCloud™ Memory," Netlist, Inc., 2010, white paper.

- **Tab HL-D**: "HyperCloud™ Memory Accelerates Simulation Performance 21%," Netlist, Inc., 2010, white paper.

- **Tab HL-E**: "Mastering EDA Environments with High Performance Memory Technology," Chris Bell, Scott Clark & Ryan Radcliff, Deopli Corp., 2011, white paper.

6.   A central feature of Netlist's HyperCloud™ memory module is its capability to provide more memory density or memory capacity using lower-cost, lower memory capacity DRAM devices.   Memory modules with higher memory capacities are continually desired by the computing community since such higher memory capacities provide improvements in system performance by allowing the computer system to reduce the frequency at which it needs to access the solid-state drive or hard-disk drive.   For example, VM servers support up to 256 virtual machines, each of which acts as a tightly isolated software container that can run its own operating system and applications as if it were a physical computer, and each virtual machine needs about 1GB to 2GB of local memory space.   Therefore, if the VM server has a total of 16GB of local memory space accessible to the CPU, to run more than 8 machines concurrently, the CPU must repeatedly transfer data to and from the solid-state or hard disk storage medium. Executing these data transfers take a significant amount of CPU time; in addition, the data transfers themselves effectively slow down the VM server performance.   These repeated accesses of the solid-state or hard disk storage medium would effectively defeat the purpose of having the VM server. Thus, having lower-cost, high-capacity memory allows the VM server to run more virtual machines, which improves the overall usage and performance of the computer system.

7.   There are two conventional ways to increase the memory capacity of a memory module. The memory module can be populated with DRAM devices which each have a higher memory capacity, thereby increasing the total memory capacity of the memory module. However, the price of higher capacity DRAM devices can be significantly more expensive than lower capacity DRAM devices, particularly at times when DRAM devices having the higher memory capacities are first introduced, since they are then sold at a premium reflecting their scarcity and complexity. For example, currently, the price of a 4-Gb DRAM device is more than twice the cost of a 2-Gb DRAM device. As the higher-capacity DRAM devices become commoditized, this premium or price differential of cost per bit disappears. In other instances, the desired memory capacity per DRAM device (e.g., 8-Gb) may not yet exist.

8.   Alternatively, the memory capacity of a memory module can be increased by increasing the number of DRAM devices per memory module, e.g., increasing the number of ranks. However, computer systems generally are limited in the number of chip-select signals that they can support per system channel. For example, for a computer system that supports at most a total of 8 chip-selects per system channel (e.g., Intel's Nehalem processor), the system can support only two four-rank memory modules per system channel, even if the system has additional slots in which to insert additional memory modules.

9.   Netlist's HyperCloud™ memory modules have the capability of "rank multiplication" by which the HyperCloud™ memory module presents itself to the memory controller as

having fewer ranks of DRAM devices than the module actually has. For example, a HyperCloud™ memory module having four physical ranks of DRAM devices presents itself to the computer system as having only two ranks, or even one rank, of DRAM devices. Therefore, since the HyperCloud™ memory module uses fewer chip-select signals from the system, more memory can be accessed per system channel.

10. The "rank multiplication" technology of Netlist's HyperCloud™ memory modules then allows the memory module to provide a given memory capacity by using more DRAM devices each having a lower memory capacity. For example, an example conventional memory module having 16GB of memory capacity may have 32 4-Gb DRAM devices arranged in two ranks. In contrast, an example HyperCloud™ memory module having 16GB of memory capacity has 64 2-Gb DRAM devices arranged in four ranks. Since the 2-Gb DRAM devices are significantly less than one-half the cost of 4-Gb DRAM devices, the HyperCloud™ memory module can provide the 16GB memory capacity for lower cost.

11. In addition, the "rank multiplication" technology of Netlist's HyperCloud™ memory modules also can allow the memory module to provide more memory capacity than would otherwise be available in conventional memory modules. For example, conventional 8-Gb DRAM devices are not yet available, so conventional memory modules with 32GB of memory capacity using two ranks of such DRAM devices are also not yet available. However, the HyperCloud™ memory module can provide 32GB of memory capacity by having 64 4-Gb DRAM devices arranged in four physical ranks which are presented as 2 ranks to the computer system. Thus, in this case, being able to construct the higher-capacity DIMM while using existing, lower-capacity (e.g., 4-Gb) DRAM devices brings unprecedented benefit to the computer system performance as well as financial advantages.

12. By logically presenting itself as having fewer ranks, thereby using fewer chip-select signals, Netlist's HyperCloud™ memory module also can increase the number of memory modules that can be accessed using the system channel's limited number of available chip-select signals. For example, Intel's Romley platform has 10 chip-select signals per system channel, so it can only populate each channel with two four-rank memory modules. However, using the HyperCloud™ memory module, each system channel can be populated with 3 HyperCloud™ memory modules per channel.

13. The technical benefits of the HyperCloud™ "rank multiplication" technology are further described in the various exhibits to this declaration. The "HyperCloud™ 8GB & 16 GB DDR3 RDIMMs" product brief describes that:

> Netlist HyperCloud memory allows 18 DIMMs per 2P server to be populated achieving the maximum density and greatest memory bandwidth vs JEDEC RDIMMs.
>
> HyperCloud rank multiplication technology presents two virtual ranks (four physical ranks) or one virtual rank (two physical ranks) to the Memory Controller Hub (MCH).

(Tab HL-B at 2.) The product brief and other product descriptions use the term "virtual ranks" to denote the logical ranks. The words "virtual" and "logical" are interchangeably
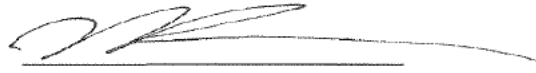
used in these documents since the word "virtual" is more familiar terminology to the customers.

14.   Similarly, both the "3-to-1 VMs-per-Server Ratio Improvement with HyperCloud™ Memory" and the "HyperCloud™ Memory Accelerates Simulation Performance 21%" white papers describe that "Netlist's HyperCloud™ virtual rank technology "enables memory capacity to be doubled through Rank Multiplication." (Tab HL-C at 3; Tab HL-D at 2.) Further, the "Mastering EDA Environments with High Performance Memory Technology" white paper describes that "HyperCloud™ memory utilizes an ASIC chipset that incorporates Netlist's patented rank multiplication and load reduction technology" and that "[r]ank multiplication increases memory capacity in servers" enabling "4-physical ranks to be presented as 2 virtual ranks (vRanks) to the CPU." (Tab HL-E at 4.)

15.   This "rank multiplication" technology is embodied in the claims of the '912 patent. For example, paraphrasing Claim 1 of the '912 patent, Claim 1 recites a memory module that comprises a first number of memory devices arranged in a first number of ranks. The memory module also comprises a logic element that receives input signals from the computer system corresponding to a second number of memory devices arranged in a second number of ranks. The second number of ranks is less than the first number of ranks, and the second number of memory devices smaller than the first number of memory devices. The logic element generates output signals that correspond to the first number of memory devices arranged in the first number of ranks. In this way, Claim 1 recites the "rank multiplication" technology by which the memory module presents two ranks to the computer system although it actually has four physical ranks of memory devices.

16.   Other claims of the '912 patent recite various features of the HyperCloud™ memory module, including some that allow it to achieve this "rank multiplication." For example, Claim 1 also recites various input signals that are used by the logic element in generating the output signals. Other claims cover other aspects of the HyperCloud™ memory module.

17.   Netlist's customers receive value from using HyperCloud™ memory modules by virtue of the capabilities of these memory modules that are not found elsewhere in the industry. I understand that a declaration by Christopher Lopes ("Lopes Declaration"), Netlist's Vice President of Sales, is being submitted in the above-captioned *inter partes* reexamination in which statements from various Netlist customers and others in the relevant industry are presented.

18.   The benefits, advantages, and values being described by Netlist's customers and others in the relevant industry in Mr. Lopes' declaration are directly attributable to the "rank multiplication" capabilities of HyperCloud™ memory modules, as I described above. In addition, the "rank multiplication" capabilities of HyperCloud™ memory module are embodied in the claims of the '912 patent, as I have described above.

19.   For example, Netlist customer Cirrascale Corp. describes HyperCloud™ memory modules as improving "simulation productivity for [Cirrascale's] customers while supporting the increased test demands of memory intensive EDA applications" and that

HyperCloud ensures that [Cirrascale is] maximizing server utilization, which in turn helps [Cirrascale] to run more complex simulation models than ever before on a 2P server." (Lopes Declaration at ¶ 15). Also, using HyperCloud™ memory modules, Cirrascale's simulation runtimes for such memory intensive applications can be reduced on average by 15% (Lopes Declaration at ¶ 16). In addition, Netlist customer, MSC Software Corp., has achieved simulation times reduced by 21% (Lopes Declaration, ¶ 12) and Netlist customer, Red Bull Racing Formula 1 Team, has achieved 60% greater server utilization using HyperCloud™ memory modules (Lopes Declaration, ¶ 14). HyperCloud™ memory modules are able to provide these improvements by virtue of its "rank multiplication" capabilities, which permit these customers to run more memory intensive applications concurrently with fewer accesses being made to hard disk storage, thereby avoiding the associated delays and slowing of latency time.

20. I acknowledge the duty to disclose information that is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

21. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the reexamined patent issuing from the above-identified *inter partes* reexamination proceeding.

Dated: ___7/8/2011___   _____

                                                   Hyun Lee, Ph.D.

11525105

Tab HL-A

Hyun Lee

████████████

████████████

████████████

SPECIAL SKILLS

Managerial Skills

- Team building, Conflict Management
- Development of Business Plan
- Development of MRDs, and answering various RFQs.
- Daily responsibilities encompass project definition, project specification, resource allocation, scheduling, and execution to plan.
- Project management and resource planning
- Ongoing success building moral and skill sets of design team
- Excellent customer relationship building.

Technical Skills

- IP development including:
  Functional Specification, Cost Analysis, Scheduling, Design Specification, Data Sheet, RTL development, Test-Plan/Test-Bench Development, User Guideline (Manual) with GUI, Implementation Guideline, Integration Guideline, FPGA prototype support, Design validation Guideline, Embedded software development, Testability Guideline, Customer Support, Errata Track, Customer Specified Feature Addition, New/Updated-version Release
- UWB based communication system – Wireless Home and Small-Office Network
- DDR3 Memory controller – High Speed, Low Cost, Low power DIMM development
- ASIC/SoC architecture/design/verification/validation/test plan
- SoC platform development for testability - Bus Architectures, DMA, Performance monitor
- DFT, MBIST, SCAN, LBIST (Logic BIST), IDDQ, ATPG, Bed-of-Nail, JTAG, ATE
- Shared memory architecture
- Failure analysis.
- Error-Tolerant Design
- High speed synchronous/asynchronous pipeline designs
- High performance/Low Voltage memories, Custom and semi-custom circuits
- Design of Ethernet MAC / Switch architectures
- WiMedia System, MAC and MAC/PHY Interface design/verification
- Memory Controller design
- WUSB design
- Third party IP integration into SoCs, and verification/validation
- Low Voltage, Low power, High performance pseudo-digital circuit design
- Verilog & VHDL system modeling for verification
- Pseudo-Analog Circuit design
- Mixed signal design
- Oscillator, DLL, Sense-Amps, pseudo-digital PLL (U.S. Patent 5,416,446).
- Wireless and Wired USB, USB OTG, InterChip-USB, ULPI Interface, ASIC and IP development. Industry specification contributions in several of these areas
- Background in Device Physics
- Unix shell, AWK
- Reverse engineering from either GDS or silicon.

Areas of Research and Development

Wireless SOHO Home Network, Wireless Personal Area Network, UWB/WiMedia, WUSB, Ethernet, SoC, High-Density/High-Performance DDR2/DDR3 RDIMM, Low-Power Memory, Microprocessor, DSP, ASIC, Pseudo-Analog Circuits, Low-Power Circuits, High Performance Circuit, DFT, Error-Tolerant Design, Failure Analysis, Shared/Distribute Memory System, DMA, Data Driven Machines, SoC methodologies, USB, ULPI, IC-USB, Device Characterizations, Mixed Signal Interfaces, System Performance Ananlysis

WORK EXPERIENCE

Netlist, Irvine, CA
02/2007 --Present – Director & Chief Architect
- Responsible for developing a DDR3 ASIC chipset that would increase the speed (30%) and reduce the power of server memory subsystems by (15%) – responsible for Business Plan, Cost Analysis, Data Sheet, Design Spec, ASIC vendor Selection and interface, DIMM board design, manufacturability, Marketing support
- Responsible for developing a self-test DIMM -- test cost reduction by more than 50%
- Responsible for concept-to-product -- DDR3 LR-DIMM that allows to double the server memory space without any hardware or BIOS changes

QualComm, San Diego, CA
02/2006 – 2/2007 – Technical Staff
- Responsible for integrating and testing USB into various cell phone platform – responsible for Interfacing IP vendor, IP feature specification, FPGA validation, IP integration Guideline, IP test procedure, IP Timing, Supporting Chip-Set design teams in San Diego, Israel and India, Supporting Embedded Software development team

I-Conext Technologies, Ladera Ranch, CA
09/2005 — UWB/WUSB CTO
- Responsible for developing business plans, VC presentations
- Responsible for High speed (1.4Gbps) UWB chipset architecture and design specification for HOSO application
- Responsible for developing the DAA (Detect & Avoid) technology.

Transdimension, Irvine, CA
09/2002 – 9/2005 –Senior Manager, ASIC/IP development
- WUSB/ USB-OTG (On-The-Go) development – Responsibilities include definition, scheduling, design and verification management, backend (layout and fabrication) interface.
- USB-OTG, ULPI (UTMI+ Low Pin Interface), WUSB working group member
- USB-IP development – Responsible for developing the USB2.0 FS and HS Softcore-IP, and supporting customers including HP, Motorola, Qualcomm, Freescale, Agere

Conexant Systems, Newport Beach, CA
10/2000 – 09/2002 – Manager, High performance SoC platform, IP components development group
- Universal Network SoC platform design, performance analysis, verification and test.
- SoC IP Components development – BIST logic, MBITS, DMA, USB Host Controller Interface, 3DES
- ARM support ARM7, ARM940T, ARM926EJS and ARM926EJS testchip development

LUCENT Technologies, Bell Labs, Allentown, PA
01/2000 – 10/2000 – Analog Circuit Design group
- 12 bit DAC for optical switch mirror
- Optical Network Switching Systems – Terra bit switch

02/1998 – 01/2000 – High performance DSP – system design, evaluation, validation
- SoC-IP integration/verification for High Performance Multi-Processor Bi-directional Bus
- Star*Core DSP ISA design verification
- Performance evaluation of the next generation process technology.
- Evaluation of CAE tools and development of advanced ASIC design methodology

1994 - 02/1998 – Project team leader / Technical manager of a multi-port Ethernet Data Link Integrated Circuit development team
- Managed 3 Ethernet projects (LUC5M01 – 10/100/1000M MAC; LUC3M08 – 10/100M Octal MAC; LUC3R04 – 10/100M Quad Repeater)
- LUC3M08 – Architecture, design and verification/validation of Octal 10/100M bit Ethernet MAC
- ATT1MX10 – Architecture, design and verification/validation of Quad 10M bit Ethernet MAC
- DMASI (DMA interface for a 100 VG MAC) – Shared memory architecture

1988 -1994 – Hardware Team Leader
- AT&T Hobbit 32 bit RISC processor – Implementation and validation
- Integer Execution Unit – Custom data path design
- Mobile Tablet Notebook Computer

UNYSIS, BlueBell, PA
1984 - 1988 – Staff Engineer
- Liberty System – Architected and implemented 2 Cache chips for a medium size main frame computer

AT&T Bell Labs, Allentown, PA
1980 – 1984 – ASIC designer
- Designed 4 ASIC chips including a full custom embedded SRAM
- Developed a test board for X-tal Oscillator
- Developed an equation for fault coverage computation

University of Michigan, AnnArbor, MI
1979 – 1980 – TA for Engineering Mathematics

IBM, Burlington, VT
1978 – 1979 – Associate Engineer
- Developed 1st IBM Standard Cell Library

PAPERS
IEEE ASIC'99, "Design of Ultra Low Power Pseudo-Asynchronous SRAM"
IEEE International Symposium of Information Theory '95, "Error-and-Erasure Decoding of Binary Cyclic Code up to Actual Minimum Distance"
IEEE ASIC'94, "A Digital CMOS Programmable Clock Generator"
KSEA NE Regional Conference '94, "Microprocessor Architecture"
IEEE ASIC'93 "CMOS I/O Transceiver with 3V/5V Lever Converter and N-Tub Voltage Generator"
IEEE COMPCON '93, "HOBBIT, High Performance, Low-Power Microprocessor"
IEEE Computer Element Mesa Workshop '93 "ATT9201X Personal Communicator System Chip Set"
Microprocessor-Memory Tie (NEC & AT&T conference) '93. "Digital Programmable Frequency Generator"

PATENTS
Granted
- "Method and apparatus for transferring multi-source/multi-sink control signals using a difference signaling technique" – U.S. Patent 7,383,455
- "Method and apparatus for distributing a self-synchronized clock to nodes on a chip" – U.S. Patent 7,174,475
- "Virtually Parallel Multiplier-accumulator" – 7,080,113
- "Bi-directional bus repeater for communications on a chip" -- U.S. Patent 6,834,318
- "On chip method and apparatus for transmission of multiple bits using quantized voltage levels" -- U.S. Patent 6,794,899
- "Method and apparatus for distributing multi-source/multi-sink control signals among nodes on a chip" – U.S. Patent 6,754,748
- "Method and apparatus for using a bus as a data storage node" -- U.S. Patent 6,725,305
- "Virtual parallel multiplier-accumulator" -- U.S. Patent 6,622,153
- "Data bus method and apparatus providing variable data rates using a smart bus arbiter" – U.S. Patent 6,611,893
- "Clock gated bus keeper" -- U.S. Patent 6,484,267
- "SRAM method and apparatus" -- U.S. Patent 6,282,137
- "Multi-port Register/Memory Cell with Pre-Set" – U.S. Patent 6,185,533
- "Ultra Low Voltage SRAM Cell" – U.S. Patent 6,108,233
- "VDD Sensor and Power Switch" – U.S. Patent 5,457,414
- "Digital Programmable Frequency Generator" - U.S. Patent 5,416,446
- "Integrated Circuit Having a Boosted Node" – U.S. Patent 5,289,025

Pending
- "Self-synchronized Clock distribution scheme in a SoC using DLL with remote clock feedback"
- "Self Correcting SRAM"
- "Method to Support Simultaneous Wireless Connection of Multiple Media Components"
- "A Method of reducing interference among Wireless Networks by Intentionally violating the communication protocol"
- "Method of Improving Wireless Communication QoS by means of Automatic Packet Sizing and Forward Error Correcting Based on the Dynamic Error Rate Forecast"
- "A Method of Detecting and Avoiding Interference Among Wireless Networks by Dynamically Estimating the Noise Level from the UWB Packet Failure Rate, and Synchronously Switching into an Unoccupied Channel"
- "Method of increasing the wireless communication range using wireless repeater/amplifier/router"

- "Method of Constructing Wireless High Speed Backbone Connection that Unifies Various Wired/Wireless Network Clusters by means of Employing the Smart/Adaptive Antenna Technique and Dynamically Creating Concurrent Data Pipelines"
- "Improving Wireless QoS by Hardware Packet Sizing, Data Rate Modulation, and Transmit Power Controlling Based on the Accumulated Packet Drop Rate"
- "A Method of Maximizing the information Access Rate from/to Storage Units in Wired/Wireless Networks"
- "Self-Modulated Liquid Cooling Loop for Electronic Systems"
- "Programmable Isolation Switch with Impedance Matching Termination and Self Adjusting Damper"
- "Self Adjusting Damper"
- "Memory Board with Self-Testing Capability"
- "Method of increasing addressable memory space in a memory board"

EDUCATION

1991-1995 – Ph.D. Lehigh University – Information Theory ("On Minimum Distance Determination and Error-and-Erasure Decoding of Cyclic Codes")
1988-1991 – Course work at Lehigh University – Solid State Device Physics
1986-1988 – Course work at University of Penn. – Solid State Device Physics
1986 – Course work at Drexel University – RISC Architectures
1883-1986 – Course work at Lehigh University – Solid State Device and Optical Devices
1979-1980 – MSEE, University of Michigan
1974-1978 – BSEE, University of Michigan

MEMBERSHIPS

Current:
        JEDEC
Previous:
        WUSB – WG member
        ULPI-USB – Promoter
        IC (Inter Chip) USB -- Contributor
        IEEE ASIC Technical Committee '94 – present
        Tau Beta Pi, Eta Kappa Nu, KSEA

AWARDS

Conexant 'First Award", 2001
Lucent "Worldwide Team Award", 1997
Magna Cum Laude, 1978
Dean's List, U of Michigan, 1975-1978
U of Michigan Scholarship 1979,1989

REFERENCES

Available upon request

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Samsung Electronics Co., Ltd.
Ex. 1010, p. 1556

SAM-NET-293_00027827

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NETLIST

SUPERMICRO
Qualified for Supermicro servers

HyperCloud™ 8GB & 16GB DDR3 RDIMMs

The performance choice for cloud computing, virtualization, database acceleration, and high performance computing.
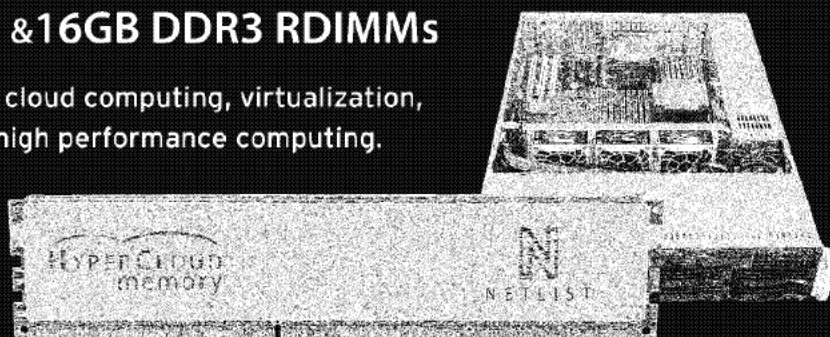
Scalable Virtual Machine Environments Need High-Capacity, High-Speed Memory

The ability to host a growing number of virtual machines (VMs) running memory intensive applications on each physical server is a critical element in the design and operation of today's advanced data centers. Performance optimization of VM servers requires high-capacity and high-speed memory to enhance on-demand scalability while controlling costs.

Because every virtual machine on the host reserves a portion of the available system memory to support its users and applications, the amount of memory required increases with the number of VMs hosted.

HyperCloud memory satisfies these demands by increasing virtualization performance and enables more VMs per physical server and more memory per VM. Data centers deploying HyperCloud achieve higher consolidation ratios, lowering TCO by maximizing server utilization.

HyperCloud Advantage

Achieve 2x Memory Configurations
- Increase virtual machine performance
- Increase number of virtual machines per server
- Reduce datacenter TCO with improved consolidation ratios

Achieve 50% Performance Improvement
- Enable up to 288GB DRAM capacity in 2P servers
- 1333MT/s speed for maximum memory bandwidth and application performance
- 8GB & 16GB 2 vRank RDIMM options

Supercharged, Scalable, On-demand
- Virtualized datacenters
- High performance computing
- Database and Memcached

www.netlist.com/hypercloud

HYPERCLOUD memory

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HyperCloud™ Memory
8GB &16GB DDR3 RDIMMs

NETLIST

Virtualized Memory Configurations
2P Intel® Xeon® 5600 (Westmere EP) Server

Maximize System Memory Performance with Netlist's HyperCloud

Netlist HyperCloud memory allows 18 DIMMs per 2P server to be populated achieving the maximum density and greatest memory bandwidth vs JEDEC RDIMMs.

HyperCloud rank multiplication technology presents two virtual ranks (four physical ranks) or one virtual rank (two physical ranks) to the Memory Controller Hub (MCH).
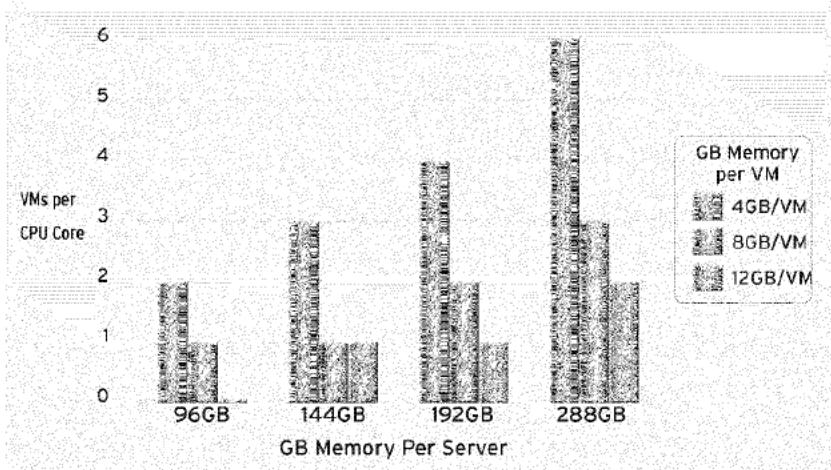
96GB configuration does not have enough memory to support 12GB/VM.
144GB configuration can support 1.5 VMs with 8GB/VM, example was rounded down to 1.
192GB configuration can support 1.5 VMs with 12GB/VM, example was rounded down to 1.

HyperCloud Memory Ordering Information

Memory Description	Supermicro Part Number	Netlist Part Number
8GB 1333/1066MHz 2Rx8(2Gb) Planar LP	MEM-DR380L-NL01-MM017	NMD1G7G32507HD10
16GB 1333/1066MHz 2Rx4 (2x2Gb) DDP Planar LP	MEM-DR316L-NL01-MM017	NMD2G7G3510BHD10
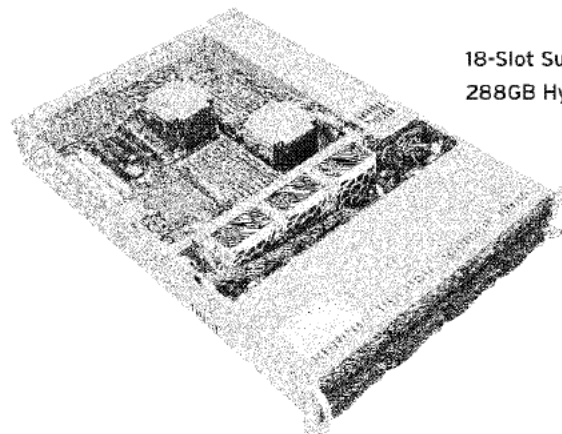
18-Slot Supermicro server with 288GB HyperCloud memory.

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NETLIST

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HyperCloud™ Memory
8GB &16GB DDR3 RDIMMs – Qualified for Supermicro Servers

NETLIST

HyperCloud System Configurations

Server	System Detail		Supported Memory Configurations			
	Processors	DIMM Slots	8GB @ 1333MT/s	8GB @ 1066MT/s	16GB @ 1333MT/s	16GB @ 1066MT/s
SYS-6026TT-BTF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-6026T-NTR+-GS015	2	18	96GB	144GB	192GB	288GB
SYS-6016T-6RF2+-GS015	2	18	96GB	144GB	192GB	288GB
SYS-6026T-6RF2+-GS015	2	18	96GB	144GB	192GB	288GB
SYS-6016T-6F-GS015	2	12	96GB	96GB	192GB	192GB
SYS-6026T-6RF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-2026T-6RF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-6036T-6RF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-7046T-6F-GS015	2	12	96GB	96GB	192GB	192GB
SYS-2026TT-H6IBQRF/H6IBXRF/H6RF-MM017	2	12	96GB	96GB	192GB	192GB
SYS-2026TT-HIBQRF/HIBXRF/HTRF-MM017	2	12	96GB	96GB	192GB	192GB
SYS-6026TT-HIBQ(R)F/HIBX(R)F/HBT(R)F-MM017	2	12	96GB	96GB	192GB	192GB
SYS-6026TT-D6IBQRF/D6IBXRF/D6RF-MM017	2	12	96GB	96GB	192GB	192GB
SYS-6026TT-HDIBQRF/HDIBXRF/HDTRF-MM017	2	12	96GB	96GB	192GB	192GB
SYS-6016T-GIBQF/GIBXF/GTF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-1026TT-IBQF/IBXF/TF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-6016TT-IBQF/IBXF/TF-GS015	2	12	96GB	96GB	192GB	192GB
SYS-6026TT-BIBQ(R)F/BIBX(R)F/BT(R)F-MM017	2	12	96GB	96GB	192GB	192GB
SYS-6026TT-IBQF/IBXF/TF-MM017	2	12	96GB	96GB	192GB	192GB

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Samsung Electronics Co., Ltd.
Ex. 1010, p. 1560

SAM-NET-293_00027831

Tab HL-C

3-to-1 VMs-per-Server Ratio Improvement
with HyperCloud™ Memory
Over 66% Total Cost of Ownership Savings

Scalable Datacenters Need High-Capacity, High-Speed Memory

The ability to host a growing number of virtual machines (VMs) running memory intensive applications on each physical server is a critical element in the design and operation of today's advanced data centers. Performance optimization of VM servers requires high-capacity and high-speed memory to enhance on-demand scalability while controlling costs.

Because every virtual machine on the host reserves a portion of the available system memory to support it's users and applications, the amount of DRAM memory required increases with the number of VMs hosted.

A major problem is the inability of JEDEC RDIMMs to support memory capacities over 96GB at 1066MT/s, or beyond 192GB at any speed in 2P servers.

This forces datacenter operators to either deploy more physical servers, each with limited memory to maintain high speed, or increase memory per server and suffer performance degradation.

HyperCloud memory eliminates the trade off by enabling beyond 96GB, up to 288GB, of memory running at speeds from 1066MT/s to 1333MT/s.
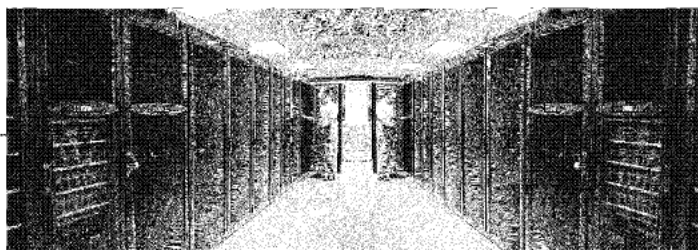
Optimized virtualization & improved consolidation ratios maximize utilization and improve TCO.

NETLIST

HYPERCLOUD memory

HyperCloud Leadership

HyperCloud is the industry's first standards-based memory designed to overcome the inherent memory and speed limitations in today's 64-bit processors.

Using HyperCloud memory to triple the amount of full-speed memory per 2P server from 96GB to 288GB, the number of systems required to support a given level of VMs can be reduced by 66 percent.

The use of HyperCloud technology enables IT Managers to increase VM density. This increased utilization drives down both capital expenditures and data center TCO.

The Drive to Virtualize

The trend toward virtualization of servers is driven by a combination of the demand to support more diverse applications and the costly deployment and management of the underlying hardware and software.

The solution is the deployment of virtual environments or VMs that support multiple applications and users though fewer servers. However, in virtual environments every end-user and every customer of a commercial data services center expect to receive sustained high-performance as if they had dedicated physical hardware and software. Similarly, applications hosted on any of the VMs need to run at-speed, without incurring any degradation due to other VMs sharing the same physical CPU.

Multi-Core CPUs Demand More Memory

Over the short time since the introduction of dual-core CPUs, the number of internal cores has jumped to four and now to six cores. For example, the Intel® Xeon® 5600 (Westmere EP)

server can include as many as 12 cores in a two-processor configuration with six cores per CPU.

This availability of multi-core CPUs is one of the key factors driving the trend of a greater number of VM deployments. For example, in typical virtualization scenarios, four to six VMs are provisioned for each core.

Assuming a requirement of 4GB per VM and five VMs per core, a 2P system with four cores per CPU would require 160GB of RAM. With the same assumptions, a 6-core 2P system would need 240GB and a 12-core 2-socket host would require 480GB to support five VMs per core at 4GB per VM.

Processor	CPU Sockets	CPU Cores	VMs/ Core	GB/VM	Memory Required	
Intel® Xeon® 7400 Series	2	2	2.5	2GB	20GB	Memory Barrier
Intel® Xeon® 5500 Series	2	4	5	4GB	160GB	
Intel® Xeon® 5600 Series	2	6	5	4GB	240GB	Hyper-Cloud Enabled
AMD Opteron® 6000 Series	2	12	5	4GB	480GB	

Figure 2. HyperCloud removes the memory barrier for multi-core servers.

JEDEC Memory: Barriers and Speed Limits

Due to memory channel loading limitations, JEDEC memory cannot support more than 192GB, which creates a *memory barrier* to full performance. Furthermore, channel restrictions reveal the inability of JEDEC RDIMMs to support memory capacities over 96GB at 1066MT/s or beyond 192GB at any speed[1], thereby adding a *speed limit* as well. ([1] Per Intel guidelines.)

More Memory Produces Greater Performance

In addition to supporting a much larger number of 4GB VMs per server, higher server memory capacities also give data
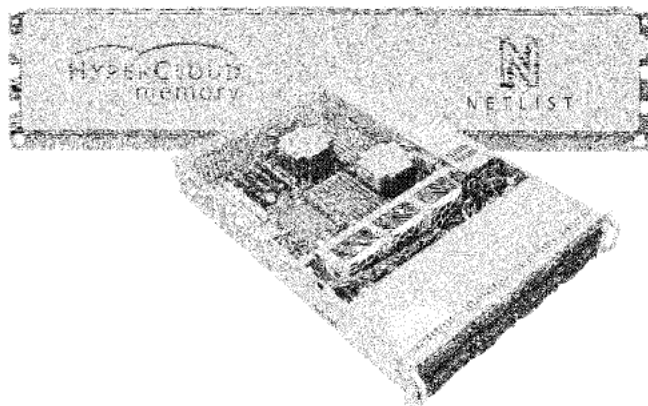
Figure 1. Dual processor server configured with 288GB HyperCloud memory.

Maximum Virtualization Optimization

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center managers the flexibility to provision more memory per VM, resulting in performance boosts. As shown in Figure 3, a 288GB server can be configured to support either six 4GB, three 8GB or two 12GB VMs per core. In contrast, a 96GB server can only support two 4GB VMs or one 8GB VM per core.
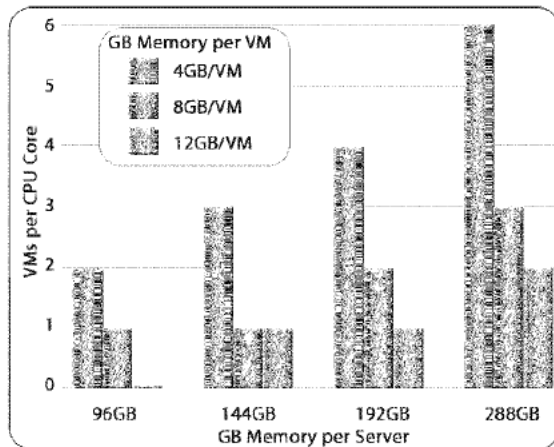

Figure 3. VM memory options in a multi-core server using HyperCloud memory. (2P Intel® Xeon® 5600 Server)

The Virtualization Performance Advantage

HyperCloud memory uses a patented design and proprietary ASICs to overcome both the over-96GB *speed limit and* the 192GB *memory barrier.* Netlist's virtual rank technology enables memory capacity to be doubled through Rank Multiplication while maintaining speed performance by implementing Load Reduction.

Providing an Economic Advantage

The positive economic impacts from improved consolidation ratios are considerable. The movement to virtualized systems brings the obvious to the forefront – doing more with less.

Improved consolidation ratios results in more compute power per square foot, less power usage, lower capital expenditures and operating expenses, and fewer personnel resources required for datacenter management.

Capital Expenditures Reduced

Implementing HyperCloud memory can increase by threefold the number of VMs per server – unleashing untapped power in currently deployed servers. Applications will run faster and more applications can be served to users.

Software Cost Reductions

Additional software licenses, configuration tools, and management software are not required to take advantage of the 3x performance improvement.

Savings in Operating Expenses

Physical consolidation eliminates real deployment, facility, power, and other support costs of the reduced number of systems. Moreover, management staff does not have to be increased to maintain servers with increased efficiency.

Facility Cost Control

Physical expansion will continue to meet growing needs of today's businesses; however, the pace can be controlled with dramatic performance increases from more efficient datacenters.

Low-Voltage Power Savings

Power demands are a top consideration of every industry. Not only do HyperCloud-enabled consolidation improvements help reduce the demand for additional power plugs, Netlist is in the forefront of low-voltage memory systems. Low-voltage HyperCloud(1.35 volt) is designed for the next generation of low power servers. This low-voltage memory requires 20% less power than 1.5 volt memory modules and maintains its performance advantage.

Delivering the Datacenter Advantage

HyperCloud memory is enabling unprecedented scalability and performance in virtualized servers:

- Delivering more memory per 2P server
- Providing more GBs memory per VM
- Enabling more VMs per core
- Increasing consolidation ratios
- Increasing application performance
- Reducing capital expenses and TCO

No other memory solution has the industry-leading capabilities and system solutions of HyperCloud Memory from Netlist.

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About Netlist

Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for the server and high-performance computing and communications markets. The Company's memory subsystems are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, and telecommunication equipment.

Netlist pioneered ideas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via 4-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

With state-of-the-art design, ISO- and OSHAS-certified manufacturing and testing facilities in the U.S., and qualified contract manufacturers in China, Netlist produces more than one million memory subsystem modules annually. Netlist's strategy is to marry its unique board-level expertise with a thorough understanding of semiconductor building blocks and system-level applications to deliver performance, cost, and time-to-market advantages to OEMs.

Netlist was founded in 2000 and is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China. For more information, visit the company's website at www.netlist.com.

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Tab HL-D

HyperCloud™ Memory Accelerates Simulation Performance 21%
Demonstrated with MSC Nastran™ Finite Element Analysis Software

High-Performance Computing Requires Both Memory Capacity and Speed

HighPerformanceComputing(HPC)applications, such as Finite Element Analysis (FEA) require not only advanced multi-core CPU processing power; they also need to have high capacity levels of memory and sustained memory access speed. As detailed in this paper, HyperCloud technology enables memory capacities up to 288GB with 1066-1333 MT/s speeds.

For scientific modeling and engineering workloads, the ability to run faster with HyperCloud means that users can run more simulations in less time and also can run more complex simulations. Without HyperCloud, such simulation workloads often require multi-node computing clusters and additional software licenses. Some complex models still cannot be simulated without enough core memory.

HyperCloud overcomes these limitations by making up to 288GB of memory available to Intel's and up to 384GB of memory to AMD's advanced multi-core CPUs, while also enabling 1066-1333 MT/s access speeds for even the largest server memory configuration.

Performance gain over 8GB RDIMMs

144GB	192GB	288GB
12%	16%	21%
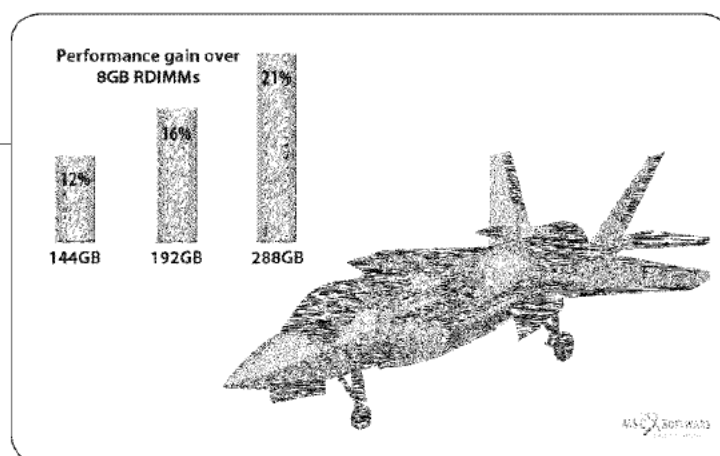
FEA images courtesy of MSC Software.

NETLIST

MSC Software

Complex Simulations Require Powerful Hardware

Today, manufacturers of everything from automotive and aircraft parts to complex assemblies rely on Finite Element Analysis (FEA) software to simulate how their designs will function in the real world. FEA programs analyze the structural response to factors such as stress, strain, vibration, displacement and temperature, enabling designers to address these issues before the first physical parts are created.

Engineers and analysts using virtual prototyping are challenged to produce results fast enough to impact design decisions and accurate enough to give their companies and management the confidence to move ahead with physical prototypes. The most advanced FEA software, such as MSC's Nastran FEA solver, can provide data that is reliable and accurate enough to be certified by the FAA and other regulatory agencies.
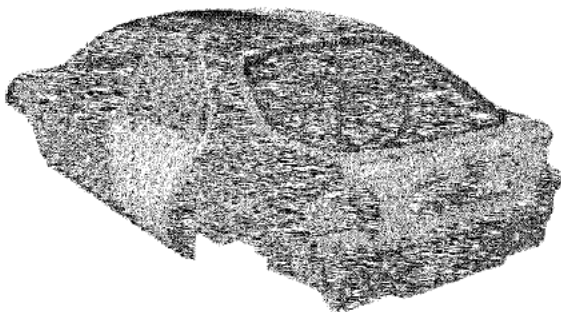
Figure 1. MSC Nastran model

Automotive models can have from 10 to 20 million Degrees of Freedom (DOFs) that must be calculated to accurately create each simulation. Therefore today's advanced FEA programs are among the most demanding applications in the world, requiring the highest performance possible from the underlying computer hardware.

HyperCloud Doubles Memory Capacity While Maintaining Memory Speed

The amount of available memory is a critical factor for achieving optimal performance because of the huge number of calculations that must be solved in every FEA analysis or simulation project.

HyperCloud is the industry's first RDIMM compatible memory designed specifically to overcome the bottlenecks manifested in today's 64-bit processors due to their inherent memory capacity and speed limitations.

Today's advanced CPUs, such as Intel's Xeon 5500 and 5600 series processors, cannot run at optimal performance because of the speed penalties incurred with JEDEC RDIMM configurations

of more than 96GB. In these configurations, memory channel loading requires the access speed to be downgraded from 1066 or 1333 MT/s to only 800 MT/s. With JEDEC RDIMMs, 288GB is not achievable at any speed.

In contrast, HyperCloud memory uses a patented architecture and advanced ASICs to overcome these memory limitations, allowing each memory channel to be populated with the maximum density and highest memory bandwidth.
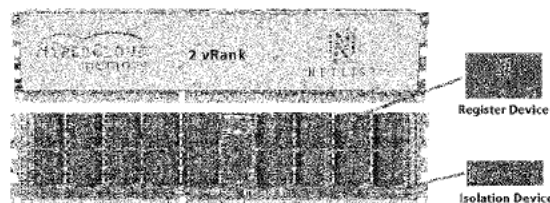

Figure 2. HyperCloud RDIMM with patented ASICs.

HyperCloud's virtual rank function enables memory capacity to be doubled through Rank Multiplication while maintaining performance through Load Reduction.

The highest full-speed memory capacity using JEDEC RDIMMs is 96GB at 1066 or 1333 MT/s and the maximum speed at 192GB is 800 MT/s. HyperCloud memory breaks these capacity and speed barriers, delivering up to 288GB or 384GB at 1066-1333 MT/s.

Netlist's HyperCloud technology enables MSC Nastran FEA software to improve performance by 21 percent, allowing users to get the most out of their software and investments, without incurring the speed and productivity degradations that are inherent with slower speed JEDEC memory.

Overview of the Testing Methodology

MSC's performance team ran Nastran Finite Element Analysis (FEA) simulations using a library of their customer's most complex models to determine which memory factors (capacity and speed) influenced overall performance, measuring elapsed simulation run time and cache misses.

Model complexity for FEA simulation is typically determined by the Degrees of Freedom (DOF) in the model, such as the number of coordinates required to accurately define a mesh representing all of the physical attributes of the parts and assemblies. DOF also include other thermodynamic variables such as pressure, temperature, material composition, etc.

Test Platform:

The test platform consisted of a single Intel Nehalem dual-processor server with two sockets, X5670 2.93GHz 6-core processors, 5 SATA disk RAID0 file system rated at 320MB/s write & 430MB/s read, and up to 288GB physical memory. System software was Red Hat Enterprise Linux Server 5.3

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Application Software:

The application software tested included MD-2010 (using MSC's newest math kernel), MSC Nastran and the newest software release, MSC Nastran ACMS for Automated Component Mode Synthesis.

Test Models:

The two primary test models used were:
- Automobile engine block with 15.2 million DOF
- Automobile body with 7.2 million DOF

Additional tests were also conducted on a variety of individual parts and complex models with Degrees of Freedom ranging from 600,000 DOF to 24 million DOF.
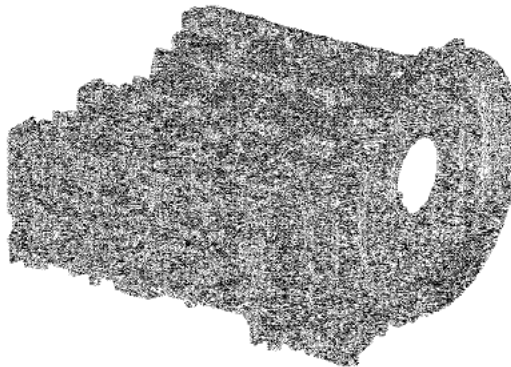
Figure 3. MSC Nastran model

Elapsed Time vs. Available Memory

Figure 4 shows results for the first test scenario in which the amount of available memory was varied from a low of 96GB to the HyperCloud "full memory" of 288GB. (This was accomplished by using the Nastran ACMS and SGI FFIO function to limit cache available to each of the four MPI threads.)
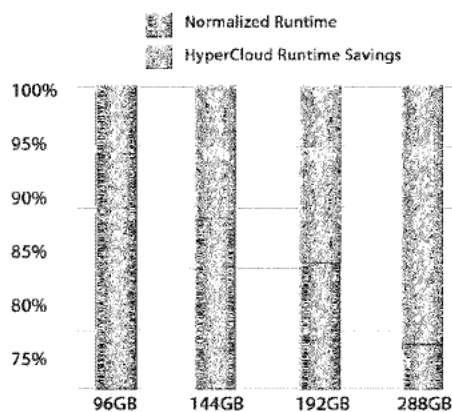
Figure 4. HyperCloud simulation runtime savings

The significant difference is due primarily to HyperCloud's ability to eliminate the high level of I/O wait times incurred for processing the large scratch files (80GB each) for the four MPI threads. With 288GB of HyperCloud memory available to the system, there was little or no wait time.

The speed improvement for the 288GB HyperCloud configuration is more than 21% faster than the 96GB configuration. This result demonstrates HyperCloud's ability to deliver superior performance for a range of memory configurations over 96GB.

Leveraging Full-Speed Memory Access Advantages of 1066MHz over 800MHz

For comparison purposes, the same tests were run at both 800 MHz and 1066MHz for all server memory capacities. This enabled an evaluation of the advantages of HyperCloud's ability to maintain 1066 MT/s speeds for all capacity levels.
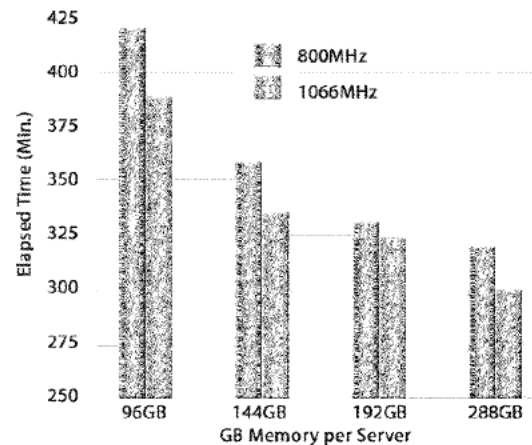

Figure 5. HyperCloud runtime speed benefit

Figure 5 illustrates the HyperCloud speed advantage for memory capacities beyond 96GB. Running memory access at 1066 MT/s provides additional performance advantages over 800 MT/s for all of the different memory capacities.

In situations where the ability to run simulations faster means boosting productivity levels, every minute saved is valuable. By maintaining 1066 MT/s memory speed for even the largest memory capacities, HyperCloud assures faster results and the ability to run more simulations in a given amount of time.

The ability to deliver both higher memory capacities and speed performance makes HyperCloud an ideal alternative for deploying high performance, cost-effective systems for virtually any simulation or modeling challenge.

3

Minimizing Read Cache Misses

The second area of focus for testing on the Engine Block model was to evaluate the frequency of missed attempts to access the system's read cache. In this test as well, the HyperCloud 288GB configuration provided a dramatic performance edge.

As show in Figure 6, the 288GB configuration eliminated 99.7% of read cache misses while the 192GB and 144GB eliminated 81% and 63% respectively of read cache misses compared to the 96GB JEDEC RDIMM configuration.
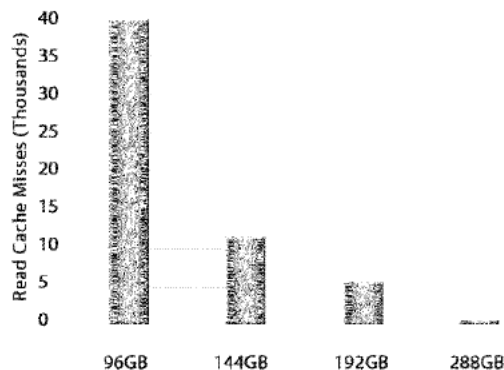

Figure 6. Read Cache misses with HyperCloud

Read Cache misses play a critical role in overall performance because a follow-up attempt by the CPU is required whenever a miss occurs. For example, when the FFIO page size is set to 16MB, as in the test case, an additional 16MB I/O record has to be fetched from the file system to memory every time that there is a Read Cache miss, thereby diverting CPU time and system resources from actual computation activity.

By completely eliminating system's read cache misses with the 288GB configuration, HyperCloud not only allows engineers to run complex simulation models faster—It enables them to perform more simulations in a given amount of time, thereby improving productivity as well as allowing for additional testing of critical parts and assemblies. Since the I/O can be kept in core, the larger memory capacities can, in some cases, enable complex jobs to run which could not be run with less memory.

Providing Large-Capacity High-Speed Core Memory for Multi-Core CPUs

Another major benefit of HyperCloud memory is the capability to take full advantage of the on-going evolution of multi-core CPU architectures.

Over a relatively short time since the introduction of multi-core CPUs, the number of internal cores has jumped to 4, 6 and even 12 in AMD's Opteron 6000 series processors. With Intel's Xeon

5600 processor series as many as 12 cores are available in a two-processor system, 6 cores per CPU.

With every additional core needing more memory to maximize the full computational speed potential, system memory requirements are doubling along with the core count.

By enabling up to 288GB of memory at a full-speed 1067 MT/s access rate, HyperCloud eliminates memory bottlenecks, enabling multi-core processors to run at maximum performance.

Optimizing Software and Hardware Interaction for Maximum Performance

For computationally-intensive programs such as MCS Software's Nastran FEA and other complex simulation solutions, the interrelationships between software and underlying hardware can play a critical role for achieving optimal performance.

By supporting multi-core processors with large capacity high speed memory, HyperCloud gives software and system designers flexibility to tune the hardware-software for maximum performance. For example, very large models can be run in core rather than parsed in and out, thereby allowing computations to proceed in an unblocked flow.

The HyperCloud Advantage

By increasing CPU memory without compromising access speed, HyperCloud technology:

- Improves simulation runtimes by over 21 percent
- Eliminates over 99% of I/O cache misses
- Enables memory of up to 288GB (Intel) and 384GB (AMD) to run at 1067 & 1333 MT/s
- Reduces I/O wait times for large models
- Overcomes memory bottlenecks to optimize performance of complex FEA simulations

HyperCloud-enabled servers have shown dramatic benchmark-runtime improvements and increased simulation efficiency over memory constrained servers. These performance increases allow more simulations in less time, thereby increasing productivity of man and machine.

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Tab HL-E

MASTERING EDA ENVIRONMENTS WITH HIGH PERFORMANCE MEMORY TECHNOLOGY

by

Chris Bell, Scott Clark & Ryan Radcliff

Deopli Corporation

Executive Summary

As semiconductor companies continue to evolve with the development of new technology, Moore's law (i.e., transistor count doubling every two years) continues to hold true. The trend is forcing the software and systems used to design these semiconductors to expand their use of memory in alignment with the increased gate count.

As an example, Electronic Design Automation (EDA) jobs that used to require 4GB of memory now require 8GB just to complete, while jobs that once needed 128GB of memory to run successfully now require 256GB and beyond. Compound never-ending growth in memory demand with steadfast developments in processor technology (as processor count scales with multi-core technology), and we can conclude that systems are woefully behind in memory capacity, as well as performance. This lag represents a growing risk for EDA environments, as costs stand to balloon to geometric proportion.

Constraints in advancing memory design are the result of many factors. We will explore how memory technology is currently designed, how its cost is derived, and the barriers that exist in designing larger, and more cost effective, capacity. Throughout this process, the inherent need for denser, and faster memory will become clear.

Moreover, this paper shows how HyperCloud™ memory from Netlist, Inc., can help overcome these constraints by adding 288GB DRAM running at 1333 MT/s. This can enable 15% improvement in an EDA job runtime.

> *To put it plainly, expensive EDA tools that are typically memory hungry will run faster with HyperCloud. A workload run with Hypercloud memory will create opportunities to either use fewer licenses (i.e., saving cost), or allow more workload to run in the same time.*
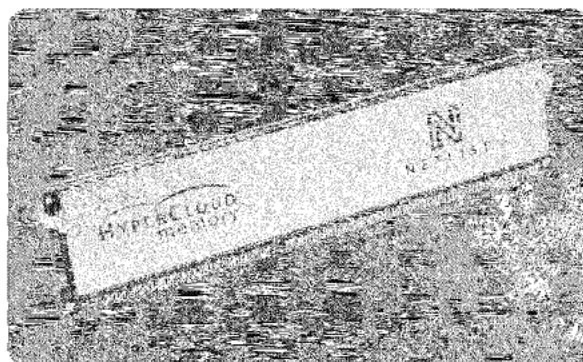
EDA's Thirst for Better Memory

To date, memory technology development follows a pattern very similar to Intel's "tick-tock" evolutionary cycle: semiconductor companies perform what is called a "geometry shrink," fitting transistors and connectors closer to create an additional level of capacity. This results in the same technology fitting a smaller footprint on the same chip, but with increased programming potential. Historically, geometry shrinking has been accomplished in one-year cycles, while a second year is spent leveraging the newly available programming space (i.e., transistors) for additional features and capabilities. The cycle then repeats with a geometry shrink - the "tick-tock" describing the "shrink-add" part of the process.
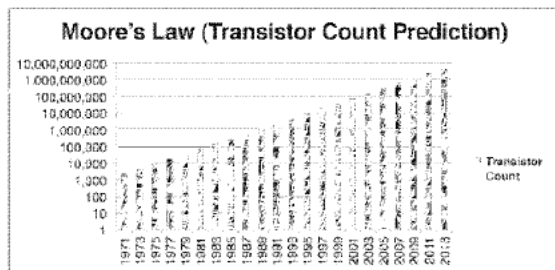
Figure 1. Moore's Law illustrated: Transistor counts double every 24 months.

Though Moore's original prediction of transistor count doubling every 18 months was long ago adjusted to every 24 months, Moore's Law is alive and very present in technology development today. The graph above reflects this - from 2300 transistors in 1971 to the anticipated 1.2 billion-transistor mark in 2009 (Opteron - Istanbul, Power7, Westmere). Looking forward, the prediction aims at 2.5 billion-transistor projects this year (2011) and ~5 billion transistors in 2013.

To support this trend, surrounding factors in EDA technology must adapt to Moore's Law and expand as well, and memory is no exception.

When a geometry shrink is performed, there is a nonlinear correlation based on chip dimension. Shrinking from 130nm to 65nm seems like a doubling of available capacity, but in actuality, available capacity quadruples. This means that there is four times the work required, provided the process of designing the chip remains the same (in actuality, more work will be required). Furthermore, going from 130nm to 90nm would equate to twice the workload, and require twice the capacity, across the board (e.g., storage, memory, processing capability resources).

Next, observe the performance gap that continues to develop between processor and memory technology. In Figure 2, processor performance continues to grow at 60% per year, and while (there are limitations in DRAM capacity as a result of the

8-rank limitation on the CPUs memory channel; you need a 2R RDIMM to populate all 3 DIMM slots in a channel. Hard Drive capacities keep pace, memory performance only grows at 9% per year. *(Computer Architecture,* Henenessey and Patterson, third edition, p. 391)
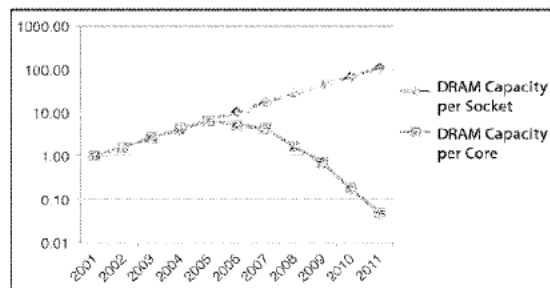

Figure 2. Memory capacity per socket and core illustrating the continuing performance gap between processor and memory technology.

This discrepancy indicates that we cannot afford to miss an opportunity to pull as much performance out of memory subsystems as possible.

The bad news does not stop there: the following chart shows that core counts have practically gone viral. Thus, demand has feverishly grown for memory capacities, and their performance, to follow suit.
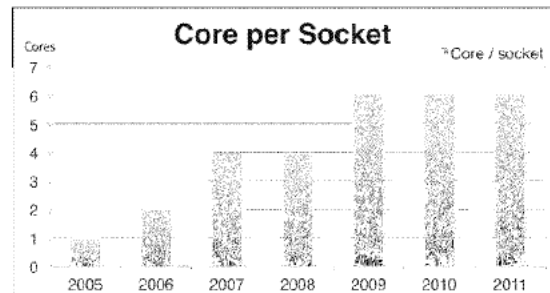

Figure 3. Increasing number of processor cores per socket on newer chipsets.

Not only must memory capacities keep pace, but they also need to multiply by the core count per socket as shown in Figure 3.

From a visual perspective, under-performing memory has obvious cost and performance implications. We'll explore constraints in memory design at a deeper level, focusing on DIMMs (i.e., dual in-line memory modules). More specifically we will focus on, Intel's Westmere-EP 64-bit architecture, because it is currently the best performing processor for overall EDA workloads. A server motherboard architecture typically consists of 3 memory channels per socket and 3 DIMMs per channel (DPC) for a maximum supported memory footprint.

Note: By specification from Intel, 1 & 2DPC run at 1333 MT/s and 3DPC runs at 800 MT/s.

The Driving Components of Memory Performance

Distance and Loading Restrictions - Due to space and wire-length restrictions on motherboards, the number of DIMM slots is limited to 3 for each channel.

Speed Limitation - A memory bandwidth limitation of 800MT/s is encountered with 3DPCs due to channel loading. When more DIMMs are populated per channel the digital signal begins to distort, due to the increased loading, causing the CPU to decrease the speed thereby minimizing the distortion.

Cost - To obtain larger memory configurations, it is logical to increase the density of the individual chips (e.g., one 16GB DIMM has twice the capacity of a 8GB DIMM) using the same socket. However, memory prices are not linear - doubling the density typically quadruples the price.

Registered or Unbuffered Types - Registered memory has an additional register to buffer the control signals, facilitating larger configurations. Unbuffered memory has slightly lower latency (i.e., less than 1%) when used with only one DIMM per channel, but cannot be combined more than two ranks deep. Using two DIMMs per channel actually reverses that penalty with interleaving, and the RDIMMS are faster.

Swap Space - If a process needs more memory than the system has available in populated RAM, the operating system's virtual memory manager will allocate more space using disks for swap space. For a high performance system, this is a very last resort, since the memory speed we have focused on is in the 6400 to 10600 MB/s range. A typical 7200-RPM hard disk can only sustain about 3 MB/s under optimum conditions. Seek time to find the location to read/ write in RAM is instantaneous, where a hard disk can be tens of milliseconds.

Rank Limitation - Each channel contains up to 8 'ranks' of memory. A rank is a group of chips that are addressed together as a set 64 bits wide, with an additional 8 bits for ECC error correction. The CPU can only address 8-ranks per channel which limits a channel to being populated with two 4-rank DIMMs. Today's industry has switched to the term 'rank' instead of 'bank' when referring to DIMM modules.

A Closer Look at DIMM Density

Among constraints in memory design, DIMM density presents the largest hurdle. First, memory manufacturers stack multiple groups of DRAMs on one DIMM to increase density. Two groups are referred to as 'dual-rank,' while four is 'quadrank.' Each rank has a separate pin for the 'Chip Select' function to access that rank. Therefore, the sockets must be uniquely connected. The first socket (i.e., farthest from the CPU, and populated first)

occupies chip selects 0-3; the second socket 4-7, and the third socket reuses 2 and 3. Thus, two quad-rank DIMMs use all 8 chip selects, leaving the third socket completely unused.

The individual chips that go onto a DIMM are available in various densities and organizations. The density is defined as the quantity of memory bits, while the organization is how the arrays of bits are arranged (e.g., a 1G chip could be arranged as 256Mx4, 128Mx8 or 64Mx16). The DIMM has a databus width of 64 bits (plus another 8 for ECC if used). Therefore, a rank of memory needs sixteen x4 chips (plus two for ECC), eight x8 chips (plus 1 for ECC), or four x16 (plus a x8 or two x4 for ECC). Since the x4 example is using 16 chips, they can be half as dense as the x8 case to reach the same total capacity for the DIMM. However, they consume twice the physical space.

In addition, densities are not linear in cost, so a 1Gb chip is more than twice the cost of a 512Mb chip. See Figure 4 for three different ways to arrive at the 1GB total capacity of a DIMM. Furthermore, adding more chips adds to heat produced, and increases the cost of manufacturing. The standard LP form-factor DIMM has room for 18 chips per side, with 36 as the usual maximum per DIMM.

Number of Chips	Chip Organization	Chip Density	Ranks
36	64Mx4	256M	2
18	64Mx8	512	2
18	128Mx4	512M	1

Figure 4. Three 1GB DIMM configurations, showing different ways to produce 1GB total capacity.

One trick used to gain space for more (i.e., less dense) chips is to stack them in a second layer on the DIMM (in addition to both sides), using special chips with a slightly different control pin. Thus, the chips share the same pins. This method adds some cost to the chip, and a lot of extra cost in manufacturing, but allows up to 72 chips on one DIMM.

Traditional ECC can correct a single-bit error in an 8-byte word, and detect a two-bit error. If a whole chip went bad, that would be 4 (or 8 or 16) bits at a time, so the ECC algorithm could possibly miss completely. However, IBM introduced a technology they called "Chipkill" (also called SDDC [Single Device Data Correction] by Intel) that uses the distributed ideas from disk RAID and makes the ECC data/checksum interleaved over 4 words. Now with a x4 chip, only one bit will be used for each calculation, enabling full correction for even an entire chip going bad. However, with x8 or x16 chips, some whole-chip detection ability is lost. The different chip organizations should be comparable in cost, but the x8 are about 10% cheaper due to very high volumes in the consumer PC market.

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Samsung Electronics Co., Ltd.
Ex. 1010, p. 1574

SAM-NET-293_00027845

HyperCloud Solves Memory Bottleneck

Netlist has developed a new memory technology, known as HyperCloud™ memory, that addresses the issues associated with memory bottlenecks. HyperCloud™ memory utilizes an ASIC chipset that incorporates Netlist's patented rank multiplication and load reduction technology shown in Figure 5.
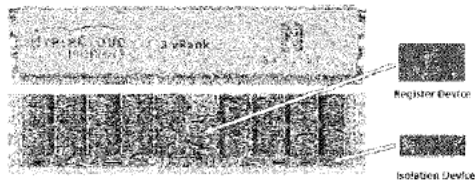

Figure 5. HyperCloud™ Memory provides load reduction and rank multiplication for high speed, high density memory.

The register device contains the rank multiplication functionality and the isolation devices perform the load reduction between the DRAM and the CPU.

Rank Multiplication - Rank multiplication increases memory capacity in servers. The rank multiplication functionality enables 4-physical ranks to be presented as 2 virtual ranks (vRanks) to the CPU. Three, 2 vRank (4 physical rank) DIMMs can be populated per channel with rank multiplication thus enabling population of the third slot on the memory channels.

Load Reduction - Load reduction increases memory bandwidth in servers. The load reduction functionality "cleans" up the distortions in the digital signal due to increased channel loading thereby allowing the CPU to maintain the 1333 MT/s speed with increased loading. Three DIMMs can be populated in a channel while maintaining the 1333 MT/s on each channel. Now 288GB can loaded in a 2P server running 1333 MT/s.

HyperCloud Benchmarks

Netlist's HyperCloud DIMMs were tested as a possible solution for systems responsible for chip design. The memory modules were tested on a Cirrascale VB1325 Server with 288GB HyperCloud RAM running at 800 MTs/ and 1333 MT/s. A tool was selected that exercises a great deal of memory, but with relatively little CPU load (and no disk I/O), to test how memory speed affects compute performance. Figure 6 shows the results. The first choice was the test number, which is related to the mathematical operations used. We chose a simple set that excludes the fancier MMX or SSE instructions, and simply adds and multiplies. The graph displays the block size (in kilobytes) on the X-axis, and the total memory speed (in Megabytes/second) on the Y-axis. The three plots are the number of concurrent processes (2, 4 and 8).

Note: Ramspeed/SMP was written specifically to test memory performance. It contains options to modify the running parameters, so we had to choose an appropriate configuration.

The affect of caches can be observed by varying the block size of the memory tests (as shown on the X-axis, in Kb/block). This particular CPU has three levels of on-chip cache, which can be seen with drops near 64Kb, 512Kb, and 4Mb. In addition, the interaction between multiple cores can be seen, as the relative speeds converge when accessing main memory.

Memory Test Conditions

System:
Cirrascale VB1325
Dual Xeon X5660 CPUs running at 2.80 GHz
Cache: L1 = 384 Kbytes, L2 = 1536 Kbytes,
L3 = 12288 Kbytes

Memory:
HyperCloud-8: Netlist 8Gb 2Rx8 PC3-10600R-9-10-22
HyperCloud-16: Netlist 16Gb 2Rx4 PC3-10600R-9-10-22

Tools:
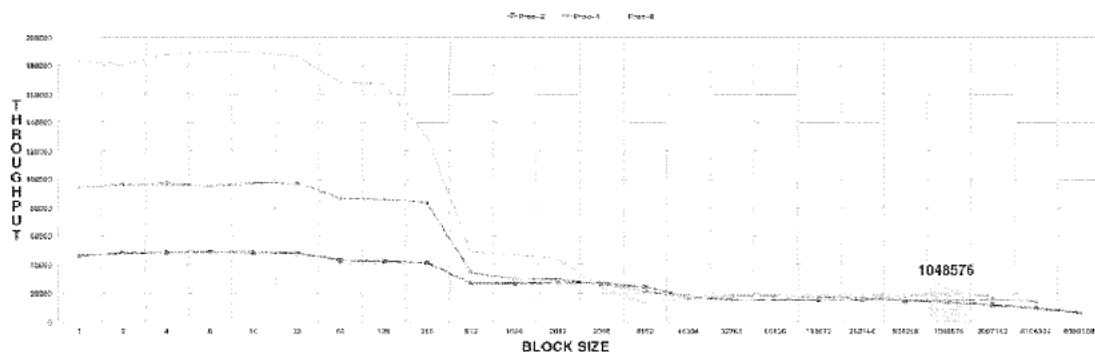Ramspeed/SMP version 3.5.0
CentOS 5.5
Linux Distribution

Figure 6. HyperCloud DIMM Test Results. The 1048576 block size is used as the basis for additional test results.

The L1 (32K data) and L2 (256K) cache is dedicated to each core, so as the number of processes increases, the total memory speed increases linearly (on the left-hand side of the graph). The L3 cache (12MB) is shared over the 6 cores in a CPU chip, and the third plateau does not have as much benefit from the 8 cores, since they are all sharing the cache. Above the 16MB block size (16384 on the graph), the effects of cache are overwhelmed, and all three lines settle to a fairly consistent level. This represents the speed of the memory system. Therefore, because high memory use is the intent, a point larger than 16MB is chosen. This ensures no cache was involved, while large memory utilization is represented by selecting 1024K (which is 1048576 on the graph) for the block size. In addition, the highest concurrency (i.e., 8 processes) is chosen to utilize both CPU chips.

Connecting HyperCloud to EDA

To put it plainly: expensive, typically memory hungry EDA tools will run faster as a result of HyperCloud. Since most, if not all, of the major EDA vendors exercise statements in their contracts that prevent publishing benchmark runs of their tools, we opted to use a theoretical memory benchmark tool. As a companion, we note the tools that have memory intensive characteristics, as well as the part of the design flow in which their memory heavy runs appear. Mileage may vary, depending on the specifics of the design and quantity of memory used. Semiconductor design companies should be able to measure the memory I/O of their tool runs. Measure the process listing (i.e., output of the ps command) to determine if the RSS entry for the tool run process is a significant percentage of the total memory size. If so, fit the memory intensive profile to benefit from faster memory at that capacity. A workload running with Hypercloud will create opportunities to either use fewer licenses (i.e., saving cost) or allow more workload to run (e.g., tests that were previously exempted due to lack of time and/ or licenses). This additional workload then delivers a higher yielding part, due to the increased chances of catching mistakes prior to tapeout.
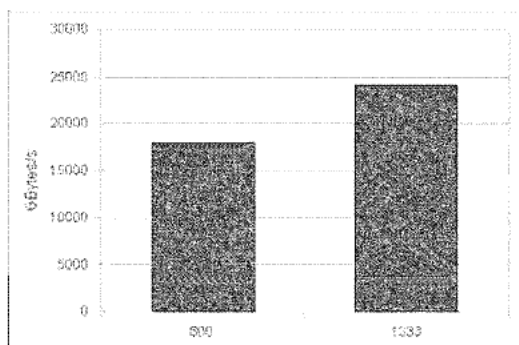

Figure 7. 67% benefit with HyperCloud memory at 1333MT/s versus 800MT/s

HyperCloud enables a system to run at 1333MT/s, which is 67% greater than 800MT/s. Figure 7 shows the results of the Ramspeed benchmark using HyperCloud memory both at the default 800MT/s and the full speed of 1333MT/s with 288GB capacity.

Note: A typical server does not utilize the full 67% advantage but, still runs 34% faster.

The specific facets of EDA design flow that would benefit from larger footprint, faster memory access speeds are defined in Figure 8. The first step toward implementation is to define the overall design flow and the time allocations for each phase:
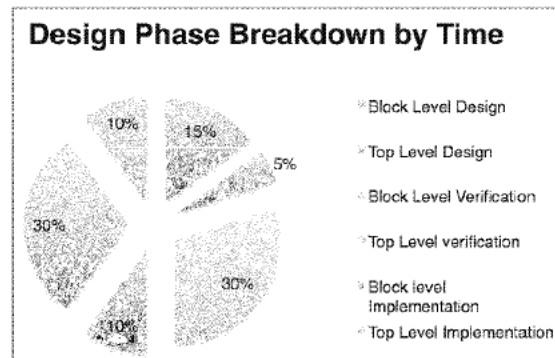

Figure 8. EDA Design Flow Breakdown, with block-level design, verification, and implementation (75% total) being memory hungry phases.

As illustrated, select parts of block-level verification and implementation are memory hungry, as are most facets of Top-Level design, verification, and implementation.

Specific tools that must be considered, from this perspective, are those used in expensive, top-level verification and implementation steps:

- Apache Design Automation Redhawk
- Cadence Affirma
- Cadence Celtic
- Cadence SOC_Encounter
- Cadence UltraSIM
- Mentor Calibre
- Mentor TestKompress
- Synopsys Formality
- Synopsys HSIM
- Synopsys ICC
- Synopsys Primetime
- Synopsys Star_RCXT

These tools have cost vectors in the hundreds of thousands of dollars per seat range, and with ~20% of the design, possess memory intensive work profiles. Given large, required memory footprint, "filling all banks" is usually implied. This traditionally means running at 800 MT/s speeds with modern

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processors (e.g., Nehalem, Westmere). However, if we speed up to 1333 MT, that would yield a 60% mathematical increase. This is measured to be 34% in a real memory test, and since we have selected only memory intensive runs to speed up, we can assume that they spend >50% of their time accessing data in memory. Therefore, we conservatively estimate improvement to be 15% over the entire run - based on the improvement we have created in the memory architecture.

In closing, this increase is a conservative estimate, and reality may show even greater benefit. With even this estimate, we can look at implications for cost avoidance (i.e. avoiding additional spending on more licenses as workloads continue to increase), that can significantly reduce software costs in an EDA environment.

Summary

By supporting multi-core processors with large capacity high speed memory, HyperCloud gives EDA professionals flexibility to run hardware and EDA software with increased server utilization thereby reducing design time and increasing design productivity. In summary this paper has shown HyperCloud memory can enable:

- 15% improvement in an EDA job runtime
- 288GB RAM in a 2P server running at 1333 MT/s
- Increased design productivity
- Reduced EDA software expenditures.

References

Ramspeed/SMP [http://alasir.com/software/ramspeed/] •

- Intel's Tick-Tock Model [http://www.intel.com/technology/tick-tock/ index.htm] •
- Intel Xeon Processor 5500 Series Datasheet, Volume 2 (April 2009) [http://www.intel.com/Assets/en_US/PDF/datasheet/321322. pdf] \
- Intel Xeon Processor 5600 Series Datasheet, Volume 2 (March 2010) [http://www.intel.com/Assets/en_US/PDF/datasheet/323370. pdf]

Cirrascale

The benchmarks were conducted on a Cirrascale VB1325 Server with 288GB HyperCloud RAM running 1333 MT/s.

Cirrascale is a premier developer of build-to-order, independent blade-based high performance computing and storage data center infrastructures.

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            Poway, CA 92064
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About Deopli

Deopli is one of the foremost thought leaders in the EDA infrastructure and cloud computing space. Composed of highly- trained personnel, equipped with technology and experience, operating under principles of self-sufficiency, technical competence, speed, efficiency and close teamwork. Providing advisory and consulting services to EDA companies with respect to their HPC environments, they also conduct specialized operations including reconnaissance, strategy definition, tactical definition and resource training. In addition, Deopli executes non-operational, high-risk tasks to achieve significant strategic objectives. Deopli is headquartered in Irvine, California. For more information, visit **www.deopli.com**.

DEOPLI

About Netlist

Founded in 2000 and headquartered in Irvine, California, Netlist is the leading provider of high-performance modular memory subsystems to the world's premier OEMs. Netlist specializes in bridging the widening gap between the system OEM's requirements and the capabilities of the IC manufacturer. Our patented memory subsystem technologies overcome density, performance, and cost limitations, effectively blending commodity components with their inherent deficiencies into highly reliable, optimized memory solutions. Netlist pioneered ideas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via 4-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory. For more information, visit **www.netlist.com**.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Netlist, Inc.

Inter Partes Reexamination Proceeding

Control Nos. 95/000,578, 95/000,579, 95/001,339

Filed: October 20, 2010, October 21, 2010, June 8, 2010

For: U.S. Patent No. 7,619,912

DECLARATION OF CHRISTOPHER LOPES

I, Christopher Lopes, hereby declare that:

I. BACKGROUND

1.   I have been asked to provide this declaration in connection with the above-identified reexamination of U.S. Patent No. 7,619,912 ("the '912 Patent").

2.   Netlist, Inc., the owner of the '912 Patent, is a publicly-traded company on the Nasdaq exchange. I have no financial interest in the '912 patent, beyond owning stock in Netlist. As an employee of Netlist, I receive a salary from Netlist, but this salary does not depend on the outcome of this reexamination. In addition, I do not receive any royalties, bonuses, or other types of compensation based on the outcome of this reexamination.

3.   I co-founded Netlist in 2000, and I currently serve as Netlist's Vice President of Sales. I have a Bachelor of Science degree in Electrical Engineering from California State University, Sacramento and a Master of Business Administration degree from Santa Clara University. I have 29 years of sales management, applications, and design experience with companies including Toshiba America, Philips Semiconductor, LSI Logic, Xicor, and Lockheed Missiles & Space, where I began my career as a systems design engineer.

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II. MATERIALS CONSIDERED

4.   I have read and am familiar with the following articles. A copy of each article is provided as a tab to this declaration, as indicated.

- **Tab CL-A**: Patrick Barnard, *Netlist Demonstrating its Innovative HyperCloud Memory Solution at INTEROP*, infoTECH Spotlight (Oct. 21, 2010), http://it.tmcnet.com/topics/it/articles/110529-netlist-demonstrating-its-innovative-hypercloud-memory-solution-interop.htm

- **Tab CL-B**: David Berlind, *Interop in Advance: HyperCloud Claims to Overcome Server's Natural RAM Limits*, InformationWeek (Oct. 11, 2010), http://www.informationweek.com/news/hardware/virtual/227701137

- **Tab CL-C**: Timothy Prickett Morgan, *Netlist's HyperCloud Gets Wall Street's Blessing*, The Register (Mar. 23, 2010), http://www.theregister.co.uk/2010/03/23/netlist_public_float/

- **Tab CL-D**: Sebastian Pop, *First-Ever 16GB, 2 Virtual Rank Memory Module Developed by Netlist*, Softpedia (Nov. 12, 2009), http://news.softpedia.com/news/First-Ever-16GB-2-Virtual-Rank-Memory-Module-Developed-by-Netlist-126838.shtml

- **Tab CL-E**: *World's First Virtual Rank Memory for Data Centers*, ZNet India (Nov. 12, 2009), http://news.znetindia.com/worlds-first-virtual-rank-memory-for-data-centers.html

- **Tab CL-F**: Timothy Prickett Morgan, *Netlist Goes Virtual and Dense with Server Memory*, The Register (Nov. 11, 2009), http://www.theregister.co.uk/2009/11/11/netlist_hypercloud_memory/

- **Tab CL-G**: *HyperCloud Is the New Buzzword: Stock Up 45%*, World Market Media (Nov. 12, 2009), http://www.worldmarketmedia.com/779/section.aspx/505/post/nlst-netlist-inc-nasdaq-last-193-39m-marketcap

- **Tab CL-H**: Mike Fratto, *Netlist Demonstrates New HyperCloud Memory Modules at Supercomputing 09*, Network Computing (Nov. 16, 2009),

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http://www.networkcomputing.com/servers-storage/netlist-demonstrates-new-hypercloud-memory-modules-at-supercomputing-09.php

- **Tab CL-I**: *Supermicro Qualifies Netlist's HyperCloud Memory on High-Density Servers*, Cloud Computing Journal (Apr. 12, 2010), http://cloudcomputing.sys-con.com/node/1351166/print

- **Tab CL-J**: *Wall Street News Alert: Trade Alert: NLST, FRPT*, Financial Tech Spotlight (Jun. 14, 2010), http://financial.tmcnet.com//human-capital-management/news/2010/06/14/4844836.htm

- **Tab CL-K**: Ashley Montgomery, *Netlist Inc. (NASDAQ: NLST) $74M (MarketCap) Trading at +20%*, World Market Media (Jun. 14, 2010), http://www.worldmarketmedia.com/779/section.aspx/1829/netlist-inc-nasdaq-nlst-74m-marketcap-trading-at-20

- **Tab CL-L**: *Netlist Accelerates MSC Software Simulation Performance*, Desktop Engineering (Oct. 11, 2010), http://www.deskeng.com/articles/ aaayta.htm

- **Tab CL-M**: David Marshall, *Netlist's HyperCloud Memory Approved for MDS Micro's Cloud Matrix*, VMblog.com (Nov. 15, 2010), http://vmblog.com/archive/2010/11/15/netlist-s-hypercloud-memory-approved-for-mds-micro-s-cloud-matrix.aspx

- **Tab CL-N**: *Red Bull Racing Revs Up Formula 1 Race Car Simulations with Netlist's HyperCloud Memory*, Breitbart (Dec. 15, 2010), http://www.breitbart.com/article.php?id=xprnw.20101215.LA17830&show_article=1

- **Tab CL-O**: *Cirrascale Qualifies HyperCloud Memory on Blade Server*, Cirrascale (Apr. 28, 2011), http://www.cirrascale.com/press/PR042811.pdf

III. PRAISE OF HYPERCLOUD™ MEMORY BY OTHERS

5.   Many industry publications have praised the technical merits of HyperCloud™ memory modules. For instance, these publications have noted:

- "Basically [HyperCloud is] a new approach to overcoming the memory and speed limitations of today's 64-bit processors." (Tab CL-A at 1–2.) HyperCloud™ memory "can yield huge cost savings for data center operators: Not only can they run three times the number of VMs [virtual machines] per server, reducing the overall number of physical machines needed and cutting power consumption, they will also get better performance out of those machines." (*Id.* at 2.)

- "The memory silicon itself may be a commodity . . . but what Netlist has done in Hypercloud is certainly not." (Tab CL-B at 1.)

- "Generally, as fatter DDR1, DDR2, and DDR3 memory modules are added to a machine or more memory slots are added to it, the clock speed for those modules has to be lowered. The important thing about the HyperCloud memory is that servers and their operating systems can use twice as much memory running at full speed, and the server iron is none the wiser that any of this is going on." (Tab CL-C at 1.)

- "The HyperCloud is the first ever invented 16GB, 2 virtual rank (vRank) memory module for servers. Utilizing Netlist's patented rank multiplication ASIC technology to fully populate three memory channels with 16 GB vRank RDIMMs (double-data-rate three, registered dual in-line memory modules), the module allows 384 Gigabytes (GB) of dynamic random access memory (DRAM) to be populated in a single dual socket server. In doing so, this (DDR3 RDIMM) improved data center utilization above any levels previously attained." (Tab CL-D at 1.)

- "Data Centers across the world would be advantaged by the latest memory module, HyperCloud that'd make possible 384 GB of DRAM in a dual socket server! Something that was never heard of before!" (Tab CL-E at 1.) "HyperCloud . . . harnesses Netlist Inc's proprietary rank multiplication ASIC technology to fully populate three memory channels with *16GB vRank RDIMMs*. 4 physical ranks are hidden from the memory controller hub and presented as 2 vRanks. *Dual socket serves can then be fully filled in with 24 16GB 2 vRank RDIMMs producing a total capacity of 384GB!"* (*Id.*, emphasis in original.) "HyperCloud is surely going to give a new lease of life to data centers across the world." (*Id.*)

- "The HyperCloud 2 vRank DDR3 DIMMs have two special ASICs. The first, a register device, presents four physical ranks of memory as two virtual ones to the memory controller on an x64 processor (it works with either Xeon or Opteron processors, and any DDR3 memory controller, for that matter). This allows the doubling-up of memory modules per channel." (Tab CL-F at 2.) "You can bet that more than one server maker will be lining up to give the product as spin as they try to push Cisco back into its networking space." (*Id.*)

6.   Steve Conway, research vice president of technical computing at International Data Corporation (IDC), the leading provider of market intelligence for the IT industry, recognized that, in "HPC [high-performance computing] datacenters, servers are typically under-utilized due to memory bandwidth and memory capacity bottlenecks. Netlist is addressing these limitations with its new high-performing DDR3 RDIMM solution, called HyperCloud . . . [which] is designed to improve server productivity and application performance, especially for memory-intensive applications and workloads." (Tab CL-G at 1.)

7.   Mike Gill, vice president of industry-standard servers at Hewlett-Packard Co. (HP), has also praised HyperCloud™ memory, commenting: "Customers running memory intensive computing environments, such as virtualization, cloud computing, and HPC applications, are often limited by memory bottlenecks in their servers. . . .   The Netlist technology on HP industry-standard servers increases server memory capacity and bandwidth to enhance application performance in converged infrastructures." (Tab CL-H at 1.)

8.   Furthermore, last year, the Orange County High-Tech Innovation Awards named Netlist as a finalist in the "Innovative Product/Technology" category for its HyperCloud™ memory submission. *TechAmerica Orange County 2010 High-Tech Innovation Awards RECAP*, TechAmerica.org, http://www.techamerica.org/htaoc (last visited Jul. 5, 2011).

9.   Each of these sources directs its praise to the technical merits of HyperCloud™ memory and makes it clear that this praise of HyperCloud™ memory is a testament to the performance of its technological capabilities. It is not the result of substantial marketing, sales, promotions, or pricing discounts. In fact, because HyperCloud™ memory provides capabilities not found elsewhere, Netlist can charge a *premium* for HyperCloud™ memory. (*See* Tab CL-F

at 2, "Netlist will be making the first batches of HyperCloud memory using Hynix memory chips, and . . . the plan is to charge a slight premium [20 to 30 percent] . . . for this memory compared to the prevailing spot prices for unvirtualized 4GB and 8GB DDR3 memory modules. The company can probably charge more for the 16GB modules, since no one has these yet.")

IV. INDUSTRY ACCEPTANCE OF HYPERCLOUD™ MEMORY

10.   In April 2010, Super Micro Computers, Inc. (Supermicro) qualified HyperCloud™ memory for use with Supermicro's high-density servers. (Tab CL-I at 1.) Supermicro praised the HyperCloud™ product, commenting that, "[w]ith Netlist's HyperCloud memory, our servers empower customers to improve their productivity and to support memory-intensive applications such as cloud computing and virtualization . . . . HyperCloud helps us to uniquely position our high memory footprint servers with unprecedented levels of performance in these growth markets." (*Id.*)

11.   Netlist then announced that HyperCloud™ memory had been selected to run on servers manufactured by Viglen Ltd. for HPC applications. (Tab CL-J at 1.) Viglen is a leading British manufacturer of IT solutions within the education and public sector. (*Id.*) Viglen commended HyperCloud™ memory as "uniquely increas[ing] aggregate memory bandwidth within our servers to support our customer's [*sic*] workload demands without memory bottlenecks . . . ." (*Id.*) Viglen further noted that HyperCloud memory "improves simulation times with large data sets and increases overall server utilization in HPC applications." (*Id.* at 2.) By incorporating HyperCloud DIMMs into Viglen servers, Viglen increased data throughput by 57%. (Tab CL-K at 1.)

12.   In October 2010, MSC.Software Corporation, a leading provider of simulation solutions, reported that HyperCloud memory accelerated the performance of its Finite Element Analysis (FEA) simulations. (Tab CL-L at 1.) MSC announced: "Using HyperCloud with our Nastran FEA simulations enables us to eliminate the high levels of input/output wait times and run complex simulations, with large models, greater than 15 million degrees of freedom, faster." (*Id.*) MSC further explained that this "has led to an overall increase in productivity and the ability to conduct more simulations at a given time per server." (*Id.*) In fact, by overcoming

memory constraints due to the large number of floating point calculations and large models in simulation projects, HyperCloud™ memory reduced simulation times for MSC applications by 21%. (*Id.*)

13.   The following month, VMware, Inc, which manufactures platforms for virtualization and cloud infrastructure, reiterated that Netlist's HyperCloud™ memory "is unique in that it directly addresses the memory slowness that customers face on a server platform with a large amount of memory." (Tab CL-M at 1.) VMware further stated HyperCloud™ memory allows customers "to maintain the faster speeds." (*Id.*)

14.   Later that year, the Red Bull Racing Formula One Team began using HyperCloud™ memory in its HP DL380 servers running memory-intensive ANSYS computational fluid dynamics (CFD) software to solve complex problems involving fluid flow. (Tab CL-N at 1.) Red Bull Racing explained that, "[u]sing HyperCloud with our CFD simulations allows us to significantly increase our Formula 1 design productivity. With HyperCloud, we achieve 60 percent greater server utilization and are now running multiple jobs per machine." (*Id.*)

15.   In April 2011, Cirrascale Corporation, the leading provider of scalable blade-based cloud solutions, qualified 8GB and 16GB HyperCloud™ memory for use with Cirrascale's VB1325 server blade. (Tab CL-O at 1.) Cirrascale is currently in production with the VB1325 server blade, offering 8GB and 16GB HyperCloud™ memory. (*Id.* at 2.) The HyperCloud™ memory in this environment supports memory-intensive applications, such as electronic design automation (EDA) and HPC simulations. (*Id.* at 1.) Cirrascale announced that incorporating HyperCloud™ memory allows Cirrascale "to improve simulation productivity for our customers while supporting the increased test demands of memory intensive EDA applications . . . ." (*Id.*) Cirrascale also stated that, "HyperCloud ensures that we are maximizing server utilization, which in turn helps us to run more complex simulation models than ever before on a 2P server. The integration of HyperCloud positions us to support and develop new levels of HPC with increased performance gains for our customers on industry standard servers." (*Id.*)

16.   Deopli Corporation Corporation, which consults with EDA companies regarding their HPC environments, benchmarked Cirrascale's HyperCloud™ memory-configured server as

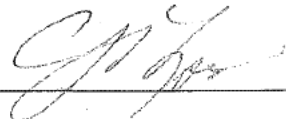Page 8   Lopes Declaration

showing significant performance improvements. (*Id.*) After completing the benchmark study,
Deopli remarked that with "Cirrascale's HyperCloud configuration, simulation runtimes of
memory intensive applications can be reduced on average by 15%. This has the potential to
accelerate key portions of the design cycle, thereby reducing design risk and delivering more
efficient use of the very expensive backend tools during System On Chip runs." (*Id.*)

      17.   As each of these industry providers have noted, and I agree, it is the technical
merits and superior performance of HyperCloud™ memory that resulted in the industry
providers' acceptance and praise for the product.

      18.   I acknowledge the duty to disclose information that is material to patentability as
defined in Title 37, Code of Federal Regulations, § 1.56.

      19.   I hereby declare that all statements made herein of my own knowledge are true
and that all statements made on information and belief are believed to be true; and further that
these statements were made with the knowledge that willful false statements and the like so made
are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United
States Code and that such willful, false statements may jeopardize the validity of the reexamined
patent issuing from the above-identified *inter partes* reexamination proceeding.

Date: 7/5/11

Christopher Lopes

11502873

Tab CL-A

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October 21, 2010

Netlist Demonstrating its Innovative HyperCloud Memory Solution at INTEROP

By Patrick Barnard
Group Managing Editor, TMCnet

Virtualization is driving new levels of efficiency and performance in the data center. For example it has changed the approach to disaster recovery: It's no longer necessary to install and maintain additional server boxes for redundancy – "virtual machines" can be readily backed up to any physical server in any location, reducing the need for investment in additional physical servers for failover. This, in turn, is driving consolidation – instead of having two dozen physical servers in a data center for redundancy, an operator can deploy just a handful of high density, high performance machines, each running numerous virtual machines, and gain new efficiencies in computing and energy consumption. Having larger boxes with more ports suddenly makes sense, whereas before it didn't.

Sprint

But putting more virtual machines per server requires greater core memory per server. Providing ample memory for High Performance Computing in virtualized environments, for example, has been a challenge, as applications such as Finite Element Analysis (FEA), used primarily for engineering of complex machines such as planes and automobiles, requires high capacity levels of memory as well as sustained memory access speed. Typically in order to run simulations using FEA you'd need multi-node computing clusters and additional software licenses. Running these resource intensive applications requires greater core memory as it is – thus it is easy to see how running these applications in a virtualized environment can seriously tax the host server.

Irvine Calif.-based Netlist has developed a new approach to boosting server memory with its new HyperCloud Memory offering. The company claims this new technology facilitates memory capacities up to 288GB for Intel (News - Alert) Xeon CPUs and up to 384GB for AMD's advanced multicore CPUs, with 1066-1333MT/s speeds. Basically it's a new approach to

http://it.tmcnet.com/topics/it/articles/110529-netlist-demonstrating-its-innovative-hypercloud-memory-solution-interop.htm

Tab CL-A
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overcoming the memory and speed limitations of today's 64-bit processors.

This company claims this solves the limitations of JEDEC RDIMMs to support memory capacities over 96GB at 1066MT/s or beyond 192 GB at any speed in 2P servers.

Yesterday at Interop (News - Alert) New York I spoke briefly with Paul Duran, director of marketing for Netlist, Inc. who explained how the company's new HyperCloud Memory solution works. I have to admit he got a little too technical for me, making it challenging for me to put this into laymen's terms, but basically it is a memory module that: "delivers cloud scale server virtualizaton with maximum memory performance -- accelerates HPC analytic and simulation runtime performance -- and breaks traditional memory capacity and speed barriers, doubling system memory."

Duran said with this new product data center operators increase the number of virtual machines per server by a magnitude of 3 to 1. It's an innovative approach he said to increasing the amount of DRAM memory required to run virtual machines – thus it is another approach for increasing performance and reducing the number of physical servers needed (i.e. consolidation).

With its ability to literally triple the amount of full-speed memory for a 2P server, this product promises to reduce the number of systems needed to support virtualized machines by as much as 66 percent. This, in turn, enables data center operators to increase VM density, thus leading to data centers that are many times more efficient.

As Duran explained, HyperCloud Memory uses a patented design and proprietary ASICs to overcome the limitations of today's CPUs. The company's "virtual rank" technology enables memory capacity to be doubled through Rank Multiplication while maintaining speed performance through Load Reduction.

This can yield huge cost savings for data center operators: Not only can they run three times the number of VMs per server, reducing the overall number of physical machines needed and cutting power consumption, they will also get better performance out of those machines. This consolidation also reduces the number of software licenses that would normally need to be purchased.

The company is demonstrating the power of its HyperCloud memory technology this week at Interop by running 100 virtual machines on a single, fully loaded, 24-slot 2P server with 384GB of DRAM. Specifically it is using an HP DL385 G7 dual socket server with AMD's (News - Alert) Opteron 8-core CPUs and 24 memory slots. Fitted with 24 16GB, 2vRank HyperCloud DIMMs, the servers are running vSphere virtualization software from VMware with 100 virtual machines, Linux, and Microsoft (News - Alert)-based host software.

For more information, visit www.netlist.com.

Patrick Barnard is Group Managing Editor, TMCnet, focusing mainly on call and contact center technologies. He also compiles and regularly contributes to TMCnet e-Newsletters in the areas of robotics, IT and customer interaction solutions. To read more of Patrick's articles, please visit his columnist page.

Edited by Patrick Barnard

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Tab CL-B

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Interop In Advance: HyperCloud Claims To Overcome Server's Natural RAM Limits

Although it's relatively uncertified, a new type of RDIMM from Netlist targets memory bottlenecks, particularly in virtual machine-based consolidation exercises where a server's processors can support more VMs than its memory can.

By David Berlind InformationWeek
October 11, 2010 08:47 PM

Interop NYC 2010 (Oct 18-22) begins one week from today and in this final stretch before the show, *InformationWeek* will be posting highlights for attendees to watch for (it's not too late to register). One of those highlights will be server RAM from a company called Netlist. But it's not just any RAM. Netlist claims that this memory -- called "Hypercloud" -- is uniquely qualified to address the needs of cloud computing and datacenter consolidation (particularly where virtualization is in play).

The memory silicon itself may be a commodity (and Netlist claims Hypercloud's prices fluctuate accordingly), but what Netlist has done in Hypercloud is certainly not.

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At Cloud Connect 2011 in Silicon Valley, TechWeb's David Berlind gets a demonstration of CA's recently acquired

To understand Netlist's innovation, you first need to understand the math that goes into determining the maximum amount of memory that can be inserted into a server. It starts with the number of sockets into which a server's microprocessors are inserted. Many of today's Intel Xeon-based servers have two sockets. Each socket has a total of three channels for memory for a total of 6 channels. Each channel has three slots into which an RDIMM (registered dual in-line memory module) memory card can be inserted for a total of what on first blush appears to be a capacity of 18 RDIMMs per two-socket server.

Anyone who has taken Memory 101 also knows that the memory cards that go into a memory channel's slots cannot be mixed and matched. They must be identical. This is true, even of most notebook computers. The net effect of this "rule" is that the most amount of memory that can be loaded into a single memory channel is 32 G-Bytes.

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The largest capacity RDIMM from companies like Dell has 16 G-Bytes of RAM on board. If one of those is used in the first of

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3Tera AppLogic graphical private cloud deployment tool.

three slots and another (matching one) is used in the second of three slots, the memory channel will be maxed out at that point. The third slot is unusable because of another limitation per memory channel: the maximum number of 64-bit wide data areas or "ranks." Today's 16 G-Byte memory cards (like the aforementioned Dell product) are quad ranked cards; they have four ranks each. Unfortunately, memory channels can only handle eight ranks at a time. In other words, once the first two (of three slots) are occupied by four-rank cards, the rank limitation of the channel has been reached and the third slot must remain unoccupied.

Sadly, conventional efforts to make use of the third slot don't add up. For example, if you fall back to three 2-rank cards (each of which would be 8 G-bytes because the number of ranks is being halved), the most amount of memory that could be packed onto a channel would be 24 G-Bytes (3 slots x 8 G-Bytes = 24 G-Bytes) -- 8 G-Bytes less than the 32 G-Bytes that could be achieved with just two 16 G-Byte RDIMMs.

With each of the six channels (remember, there's three channels for each of the two sockets) being limited to two 16 G-Byte RDIMMs, the net effect is that the server can only take 12 RDIMMs (instead of 18, even though there are 18 physical slots). Six RDIMM slots (one per channel) must go unused and the maximum amount of memory that can be packed into the server works out to be 192 G-Bytes (12 RDIMMs x 16 G-Bytes per RDIMM).

Enter Netlist with HyperCloud.

According to Netlist director of business development Paul Duran, the company's HyperCloud 16 G-Byte RDIMM's appear to the system as two-rank RDIMMs instead of four-rank RDIMMs. "We make four physical ranks look like two virtual ranks to the CPU, and that's how you get double your memory" said Duran.

With HyperCloud RDIMMs occupying two of a channel's three slots, the memory controller only sees a total of four ranks (50% of the eight-rank max per channel). By creating such an illusion to a server, the third slot on each of the six channels can have another 16 G-Byte HyperCloud RDIMM inserted into it. The net result is that the server's maximum memory is increased by 96 G-Bytes (6 channels x 16 G-Bytes) from 196 G-Bytes to 288 G-Bytes.

But according to Duran, the benefits of HyperCloud don't stop there. Another well-known physical limitation of Intel's current memory architecture has to do with the power requirements of each conventional RDIMM. With only one RDIMM occupying the first of a memory channel's three slots, that memory channel can run at its maximum rated speed of 1333 MHz. But as soon as a second RDIMM is loaded onto the channel, the speed drops to 1066 MHz and when a third RDIMM is deployed, the speed drops even further to 800 MHz. "192 total G-Bytes per server at 1066 MHz is what everyone runs" said Duran (upon further inspection, the aforelinked Dell RDIMM is indeed rated at 1066 MHz).

According to Duran, for those relying on highly virtualized systems -- the operators of public or private clouds or just those IT managers who are using virtualization to consolidate their datacenters -- the ability to jump to 288 G-Bytes of memory running at 1333 MHz significantly changes the extent to which such a maxed-out server becomes a consolidation target.

"For example, an Intel XEON 5600 Westmere-based system will have 6 processor cores in each of its two sockets," said Duran. "Going off the commonly accepted assumed maximum of a five virtual machines per core, a single system could have [as many as 60 virtual machines running concurrently]" (6 cores x 2 sockets x 5 virtual machines per core). Even with just 4 G-Bytes allocated to each machine, you'd need 240 G-Bytes of memory. When it comes to virtualization, the system memory is what turns out to be the bottleneck."

Enderle Group principal analyst Rob Enderle said HyperCloud looks promising but cautioned that short of certification from the software providers whose wares would be expected to run on such a system, IT managers should be prepared to conduct extensive tests before assuming the extra memory will make a difference.

"The machine should be thermally capable of filling all its slots," said Enderle. "The risk is more on the software side than the hardware side. Applications are often written and tuned with the idea that some limitation is in place. So, if you lift the limitation, it's possible that the application might act in some unanticipated manner." Enderle said that getting some certification from application providers would go a long way towards making IT managers feel comfortable running with such an unorthodox configuration.

Duran said that in terms of hardware certification, that Netlist was working with all the "usual suspects" but could only publicly mention Supermicro and Viglen as manufacturers that Netlist has worked with to certify its memory.

On the software side, HyperCloud has not been validated by any application or software providers. However, raising the memory bar from 192 G-bytes to 288 didn't seem to phase VMware product

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The retail price for a 16 G-Byte HyperCloud RDIMM is currently around $1200. But Duran warned that as with all other memory products on the market, HyperCloud's prices are subject to fluctuation.

Netlist will be exhibiting at booth 611 in Interop's Cloud Computing Zone.

David Berlind is the chief content officer of TechWeb and editor-in-chief of TechWeb.com. He can be reached at dberlind@techweb.com and you also can find him on Twitter and other social networks (see the list below).

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Comment by davidberlind Oct 12, 2010, 12:38 PM EDT

Thanks for the feedback UberGoober. Unfortunately, captcha is a necessary evil given the number of unscrupulous people who use bots to leave comment spam on our threads (eg: for Viagra, etc.). We are currently looking into alternative methods to keeping the comment spam at bay.

Regarding the erasure of your comment mid-thought, I'm looking into that as well. You should not be experiencing any "screen charges" though.

David Berlind

Chief Content Officer

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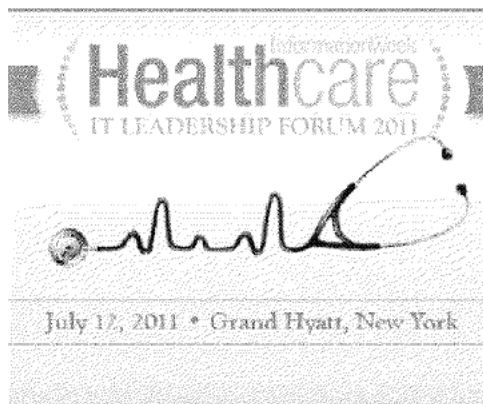
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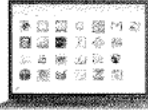
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Netlist's HyperCloud memory gets Wall Street's blessing
Raises $14.1m in stock sale

By Timothy Prickett Morgan

Posted in Financial News, 23rd March 2010 06:02 GMT

Right about now, server memory module maker Netlist is probably wishing that it hadn't already gone public. But if the enthusiasm in a new public offering by investors on Wall Street last Friday is any indication, Netlist may be onto something with its new HyperCloud DDR3 super-dense main memory for servers.

As *The Register* explained [1] last fall when Netlist announced the HyperCloud memory at the SC09 supercomputing trade show, the DDR3 memory from Netlist has an two special ASICs on the memory module that virtualize the memory. One ASIC virtualizes ranks of physical memory, allowing for the number of memory modules to be doubled up on each DDR3 memory channel coming out of the server. The other tricks the memory controllers on the processors into making four physical memory slots look like one, allowing for the extra memory slapped into the machines to run at the full 1.33 GHz speed for DDR3 modules today.

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Generally, as fatter DDR1, DDR2, and DDR3 memory modules are added to a machine or more memory slots are added to it, the clock speed for those modules has to be lowered. The important thing about the HyperCloud memory is that servers and their operating systems can use twice as much memory running at full speed, and the server iron is none the wiser that any of this is going on.

HyperCloud memory modules started sampling last December and were slated to be in production some time during the first quarter.

Netlist is not particularly large or profitable at this point in its history, but it has what sounds like a good idea, and so the company hired Needham & Company to put together a public offering of three million of its shares to raise some cash to put HyperCloud memory into production and market it.

Netlist said on Friday that it was actually able to offload just under four million shares at $3.85 a pop, fielding $15.4m in gross proceeds and about $14.1m for its own coffers. Needham & Company has 30 days to see if Wall Street might want another 599,250 shares, which could net Netlist another $2.2m if the shares sell, the company estimates.

Netlist has a market capitalization of $79.2m at time of writing. The real wonder is not why Netlist - which has a knack for choppy revenues and losses, as many startups do - was able to get money out of Wall Street. It is why one of the big server makers - Intel, or Advanced Micro Devices, all of which have a huge stake in server virtualization and will have to make up

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some revenue declines and margins if server virtualization eventually causes footprints to contract - hasn't snapped up Netlist already. ®

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First-Ever 16GB, 2 Virtual Rank Memory Module Developed by Netlist

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November 12th, 2009, 11:59 GMT| By Sebastian Pop

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"In HPC datacenters, servers are typically under-utilized due to memory bandwidth and memory capacity bottlenecks. Netlist is addressing these limitations with its new high-performing DDR3 RDIMM solution, called HyperCloud," Steve Conway, research vice president of technical computing at IDC, said. "HyperCloud is designed to improve server productivity and application performance, especially for memory-intensive applications and workloads."

The HyperCloud is the first ever invented 16GB, 2 virtual rank (vRank) memory module for servers. Utilizing Netlist's patented rank multiplication ASIC technology to fully populate three memory channels with 16GB vRank RDIMMs (double-data-rate three, registered dual in-line memory modules), the module allows 384 Gigabytes (GB) of dynamic random access memory (DRAM) to be populated in a single dual socket server. In doing so, this (DDR3 RDIMM) improved data center utilization above any levels previously attained.

Using the rank multiplication technology, four physical ranks are hidden from the memory controller hub and presented as 2 vRanks. This means that dual socket servers can then be fully populated with 24 16GB 2 vRank RDIMMs, for a maximum capacity of 384GB.

"HyperCloud marks an important step for Netlist as we look to fill the datacenter memory gap," C.K. Hong, president and CEO of Netlist, added. "Growth in key technologies like virtualization and cloud computing has been stymied by the limitations of existing memory solutions. By breaking memory barriers, HyperCloud successfully supports these applications and others like high-performance computing. Maximizing memory is the easiest way to improve performance and lower operating expenses for datacenters."

The Supercomputing tradeshow that will take place in Portland, Oregon, between November 17-19, 2009 will be the proving ground for this new breakthrough. The module will come in 4GB, 8GB, and 16GB 2 vRank module options and will enter production probably during the first quarter of 2010. Netlist plans to give samples of HyperCloud to major OEM customers in December.

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World's First Virtual Rank Memory for Data Centers

Posted on November 12, 2009 by Admin

Data Centers across the world would be advantaged by the latest memory module, HyperCloud that'd make possible 384 GB of DRAM in a dual socket server! Something that was never heard of before!

HyperCloud, the first virtual rank[2-vRank] memory module of 16 GB for servers was launched for the first time across the globe by Netlist Inc. *Netlist Inc*, is a California-based premier manufacturer of high performance modular memory subsystems that produces 1 million modules annually.

HyperCloud is a double-data-rate three, registered dual in-line memory module [DDR3 RDIMM] which maxes server utilization improving application performance in any data center. It harnesses Netlist Inc's proprietary rank multiplication ASIC technology to fully populate three memory channels with **16GB vRank RDIMMs**. 4 physical ranks are hidden from the memory controller hub and presented as 2 vRanks. **Dual socket servers can then be fully filled in with 24 16GB 2 vRank RDIMMs producing a total capacity of 384GB!**

Steve Conway, Research VP, Technical Computing at IDC pointed out, "In HPC datacenters, servers are typically under-utilized due to memory bandwidth and memory capacity bottlenecks. Netlist is addressing these limitations with its new high-performing DDR3 RDIMM solution, called HyperCloud," which is "is designed to improve server productivity and application performance, especially for memory-intensive applications and workloads."

The debut of HyperCloud is expected at the **Supercomputing Tradeshow**, taking place in Portland, Oregon from **17-19 November, 2009,** in booth number 2398. Sampling of HyperCloud to major OEM customers is planned by Netlist sometime in December with production slated for Q1 2010. HyperCloud modules would be retailed in 4GB, 8GB, & 16GB 2 vRank module options. HyperCloud is surely going to give a new lease of life to data centers across the world.

Share the news

This entry was posted in Dedicated Server, Virtual Server and tagged ASIC technology of Netlist, DDR3 RDIMM, HyperCloud, Netlist Inc, Portland, Supercomputing tradeshow, Virtual Rank Memory. Bookmark the permalink.

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Original URL: http://www.theregister.co.uk/2009/11/11/netlist_hypercloud_memory/

Netlist goes virtual and dense with server memory
So much for that Cisco UCS memory advantage

By Timothy Prickett Morgan

Posted in HPC, 11th November 2009 18:01 GMT

Netlist, a publicly traded company based in Irvine, California that was founded in 2000 and that you have probably never heard of, will probably make a big splash at the SC09 supercomputing trade show next week. Netlist, which makes memory modules on an OEM basis for various companies, said Wednesday that in December it will roll out a virtualized, dense memory DDR3 module that will be able to trick servers into having more main memory than they are supposed to.

The ability to offer more memory capacity on an x64 server than is allowed in standard boxes is, of course, one of the key selling points [1] of Cisco Systems' B250-M1 blade server in the "California" Unified Computing System and its rack-based sibling, the C250-M1. Both of these machines are equipped with a special memory ASIC that allows Cisco's two-socket Xeon 5500 servers to address up to 384GB of main memory, when a standard server tops out at 96GB in machines with 12 memory slots and at 144GB in machines with 18 slots using very pricey 8GB DIMMs. With the memory extender ASIC on the B250 and C250 servers, Cisco can use less capacious and cheaper 2GB and 4GB DIMMs to get a given capacity, and do so for a lot less money - between a quarter and a third of the price of other server platforms that have to resort to denser and more expensive memory.

Enter Netlist with its HyperCloud memory modules - which, by the way, will plug into any server and which will do essentially the same trick as Cisco is pulling, but do so inside the memory module rather than on the motherboard.

Netlist got its start in 2000 doing custom printed circuit board design, and a "netlist," according to Paul Duran, director of business development at the company, is akin to a bill of materials for all of the connectivity on a PCB. A few years back, when dense rack and blade servers started going volume, Netlist became a specialist in making very low profile memory on an OEM basis for blade server makers. (The company does not disclose who its customers are, but they're probably the usual suspects.) The company also developed a memory packaging technology called Planar-X, which allows for two PCBs loaded with memory chips to be packaged together relatively inexpensively to share a single memory slot. This technique is cheaper and more reliable, according to Duran, than some of the dual-die packaging techniques memory module makers use to make dense memory cards out of low density and cheaper memory chips.

With the HyperCloud memory, Netlist has created its own memory virtualization ASIC and is plunking it onto planar or Planar-X DDR3 memory modules, depending on what server makers want to deploy.

Using the Planar-X double-board designs, Netlist can take 1Gb memory chips and make an 8GB memory module that

costs only 20 to 30 per cent more than a standard 4GB module using 1Gb chips; using 2Gb chips, it can make a 16GB module, something no one else can do yet.

But this is not the neat bit.

In the current Nehalem Xeon designs, there is a limit to the number of ranks of memory that each memory channel can address. A standard DDR3 DIMM has four ranks of memory (two arrays of chips linked together on each side of the module) and each memory channel in the processor's integrated memory controllers can only address eight ranks per channel. With three channels per Nehalem processor, you top out at 96GB of main memory using four-rank 8GB DDR3 DIMMs, which aren't even available yet - and even then they are, they will be wicked expensive. And on the machines that have 18 memory slots, offering 144GB of memory capacity using 8GB DIMMs, you have to slow the memory down because there is a cap on the bandwidth the Xeon 5500s and their memory controllers will allow - 800 MT/sec, which means it has to run at 800MHz instead of 1.33GHz. This obviously has a big effect on performance.

The HyperCloud 2 vRank DDR3 DIMMs have two special ASICs. The first, a register device, presents four physical ranks of memory as two virtual ones to the memory controller on an x64 processor (it works with either Xeon or Opteron processors, and any DDR3 memory controller, for that matter). This allows the doubling-up of memory modules per channel. And, thanks to the Planar-X packaging, Netlist can put twice as much physical memory in a slot. The other ASIC is an isolation device that makes four memory slots look like one as far as the memory controllers and memory bandwidth are concerned, allowing for main memory to run at the full 1.33GHz speed, even on a system with 18 slots that is fully populated. The maximum of 384GB per two-socket server assumed 24 memory slots.

Duran says that Netlist will be making the first batches of HyperCloud memory using Hynix memory chips, and that the plan is to charge a slight premium (that's the 20 to 30 per cent mentioned above) for this memory compared to the prevailing spot prices for unvirtualized 4GB and 8GB DDR3 memory modules. The company can probably charge more for 16GB modules, since no one has these yet.

What's the net effect of using HyperCloud memory? Duran cooked up this comparison: take 60 Xeon-based servers, each with 48 virtual machines allocated with 4GB. By installing HyperCloud memory and doubling up memory capacity, the number of servers can be cut in half (assuming memory, not CPU capacity, is the main bottleneck for virtualization). If you assume that - and maybe that is rational and maybe not, but that is certainly Cisco's sales pitch - then using HyperCloud memory on those Xeon rack servers cuts the number of servers in half, power consumption by 36 per cent, and cuts hardware and software costs at the data center level by around 20 per cent. Memory is a big component of a server's price these days, and Netlist is charging a premium for its virtualized memory; hence, even when you cut the server count in half, the iron cost doesn't come down as much as you might expect.

The one cost that Duran did not calculate was savings in power and cooling, but the HyperCloud memory burns under 10 watts for a 16GB module, and in general, for a given capacity, a HyperCloud module will burn 2 to 3 watts less than a standard DDR3 module. And because HyperCloud memory can run at the full 1.33GHz speed, regardless of the capacity in the box, there should be a sizeable performance boost on applications that are sensitive to memory bandwidth - maybe as high as 50 per cent, says Duran.

Netlist plans to start sampling HyperCloud memory modules to OEM customers beginning in December, and expects volume production to begin in the first quarter of 2010. You can bet that more than one server maker will be lining up to give the product a spin as they try to push Cisco back into its networking space. ®

Links

1. http://www.theregister.co.uk/2009/10/09/cisco_c_racks/

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NLST -- Netlist Inc (NASDAQ) Last $1.93 $39M (MarketCap)

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Date: November 12, 2009 4:10 PM
Publisher: Editor's Desk
Tags: NLST, NASDAQ, Technology

HyperCloud is the new buzzword: Stock up 45%

Netlist Inc (NASDAQ/NLST) a designer and manufacturer of high-performance memory subsystems, today launches HyperCloud(TM), the world's first 16GB, 2 virtual rank (vRank) memory module for servers. A double-data-rate three, registered dual in-line memory module (DDR3 RDIMM), HyperCloud maximizes server utilization to improve datacenter application performance. HyperCloud allows 384 Gigabytes (GB) of dynamic random access memory (DRAM) to be populated in a single dual socket server, reaching unprecedented levels of server performance.

HyperCloud utilizes Netlist's patented rank multiplication ASIC technology to fully populate three memory channels with 16GB vRank RDIMMs. Four physical ranks are hidden from the memory controller hub and presented as 2 vRanks. Dual socket servers can then be fully populated with 24 16GB 2 vRank RDIMMs reaching a total capacity of 384GB.

"In HPC datacenters, servers are typically under-utilized due to memory bandwidth and memory capacity bottlenecks. Netlist is addressing these limitations with its new high-performing DDR3 RDIMM solution, called HyperCloud," said Steve Conway, Research Vice President of Technical Computing at IDC. "HyperCloud is designed to improve server productivity and application performance, especially for memory-intensive applications and workloads."

With load reduction, servers populated with four DIMMs per channel can operate at the highest transfer-rate of 1333MT/s providing maximum memory bandwidth, increased server performance and low latency.

"HyperCloud marks an important step for Netlist as we look to fill the datacenter memory gap," said C.K. Hong, President and CEO of Netlist. "Growth in key technologies like virtualization and cloud computing has been stymied by the limitations of existing memory solutions. By breaking memory barriers, HyperCloud successfully supports these applications and others like high-performance computing. Maximizing memory is the easiest way to improve performance and lower operating expenses for datacenters."

HyperCloud will debut at the Supercomputing tradeshow, taking place in Portland, Oregon November 17-19, 2009, in booth number 2398. Netlist plans to sample HyperCloud to major OEM customers in December with production slated for Q1 2010. HyperCloud will be available in 4GB, 8GB, and 16GB 2 vRank module options.

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L&L Energy, Inc. (NASDAQ: LLEN) Mining Coal and Profits in China

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Network Computing

David Skinner, VP of Information Services from Starhub, is opening up a universe of possibilities by moving into the cloud.   WATCH HIS STORY ●

Netlist Demonstrates New HyperCloud Memory Modules at Supercomputing 09

Posted by Mike Fratto, Editor on November 16, 2009

Portland, OR. - November 16, 2009 - At Supercomputing 09, Netlist, Inc. (NASDAQ: NLST), a designer and manufacturer of high-performance memory subsystems, is demonstrating the world's first 16GB 2 virtual rank (vRank) double-data-rate three, registered dual in-line memory module (DDR3 RDIMM), HyperCloud???. Netlist will also showcase the interoperability of HyperCloud memory with standard JEDEC server memory solutions on popular enterprise servers. This demonstration reinforces HyperCloud's ability to function as a standard RDIMM while increasing memory bandwidth and capacity for datacenter servers.

To showcase its 2-vRank HyperCloud modules, Netlist is using industry standard servers, such as the HP ProLiant DL380, demonstrated in the following configurations:

- 8GB and 16GB 2 vRank DDR3 RDIMM functionality
- Three 2 vRank modules per channel
- 1333 Mega Transfers per second (MT/s)
- Interoperability with standard JEDEC DDR3 modules
- Interoperability with different RDIMM capacities

"This technology maximizes server utilization with a simple plug-and-play memory module," said Paul Duran, director of business development at Netlist. "HyperCloud enables high-performance cloud computing while reducing datacenter costs and increasing application performance."

"Customers running memory intensive computing environments, such as virtualization, cloud computing, and HPC applications, are often limited by memory bottlenecks in their servers," said, Mike Gill, vice president, Industry Standard Servers Platform Engineering at HP. "The Netlist technology on HP industry-standard servers increases server memory capacity and bandwidth to enhance application performance in converged infrastructures."

HyperCloud will debut at the Supercomputing trade-show, taking place in Portland, Oregon during November 17-19, 2009, in booth number 2398. Netlist plans to sample HyperCloud to major OEM customers in December with production slated for Q1 2010. HyperCloud will be available in 4GB, 8GB, and 16GB 2 vRank module options.

About Netlist:
Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for the server and high-performance computing and communications markets. The Company's memory subsystems are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, and telecommunication equipment. Netlist was founded in 2000 and is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China.

Netlist is listed on the NASDAQ stock exchange under the ticker "NLST." More information can be found on the Company's web site: www.netlist.com.

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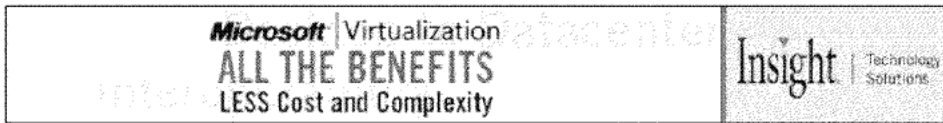
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Supermicro Qualifies Netlist's HyperCloud Memory on High-Density Servers

IRVINE, Calif., April 12 /PRNewswire-FirstCall/ -- Netlist, Inc. (Nasdaq: NLST), a designer and manufacturer of high performance memory subsystems, today announced qualification of HyperCloud(TM) memory on Super Micro Computer, Inc. (Supermicro) (Nasdaq: SMCI) high-density servers. Combining HyperCloud memory with select Supermicro servers enables optimal server utilization. This combination improves datacenter application performance and overcomes memory bottlenecks.

"With Netlist's HyperCloud memory, our servers empower customers to improve their productivity and to support memory-intensive applications such as cloud computing and virtualization," said Wally Liaw, vice president of sales at Supermicro. "HyperCloud helps us to uniquely position our high memory footprint servers with unprecedented levels of performance in these growth markets."

By optimizing server utilization, HyperCloud improves datacenter economics associated with memory intensive, high performance computing applications and workloads, including virtualization, cloud computing, online transaction processing, video services and storage. Servers in these datacenters are typically underutilized due to memory bandwidth and capacity bottlenecks. Improving performance while lowering operating and capital expenses in datacenters, increases utility out of new and existing servers.

"Qualification by Supermicro is a tremendous accomplishment for the HyperCloud team as we continue to expand our solution to a broader user base," said C.K. Hong, president and CEO of Netlist. "We look forward to working with Supermicro and providing the industry with a high performance memory solution that supports intensive workloads."

Pricing and Availability

HyperCloud memory is available with the OEM model SYS-6026TT-BTF-GS015 12-slot and the SYS-6026T-NTR+-GS015 18-slot Supermicro Servers. Contact Netlist for details on HyperCloud memory, pricing, part numbers, datasheets and application notes. For server information, please contact Gloria Sun, Senior Director of Sales at 408-503-8115 glorias@supermicro.com

About Netlist:

Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for the server and high-performance computing and communications markets. The Company's memory subsystems are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, and telecommunication equipment. Netlist was founded in 2000 and is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China.

Safe Harbor Statement

This news release contains forward-looking statements regarding future events and the future performance of Netlist. These forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those expected or projected. These risks and uncertainties include, but are not limited to, continuing development, qualification and volume production of NetVault(TM) and Hyper Cloud(TM); the rapidly-changing nature of technology; risks associated with intellectual property, including the costs and unpredictability of litigation over infringement of our intellectual property; volatility in the pricing of DRAM ICs and NAND; changes in and uncertainty of customer acceptance of, and demand for, our existing products and products under development, including uncertainty of and/or delays in product orders and product qualifications; delays in the Company's and its customers' product releases and development; introductions of new products by competitors; introductions of new products by competitors; changes in end-user demand for technology solutions; the Company's ability to attract and retain skilled personnel; the Company's reliance on suppliers of critical components; fluctuations in the market price of evolving industry standards; and the political and regulatory environment in the People's Republic of China. Other risks and uncertainties are described in the Company's annual report on Form 10-K, dated February 19, 2010, and subsequent filings with the U.S. Securities and Exchange Commission made by the Company from time to time. Except as required by law, Netlist undertakes no obligation to publicly update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

About Super Micro Computer, Inc. (NASDAQ: SMCI):

Supermicro, the leader in server technology innovation and green computing, provides customers around the world with application-optimized server, workstation, blade, storage and GPU systems. Based on its advanced Server Building Block Solutions, Supermicro offers the most optimized selection for IT, datacenter and HPC deployments. The company's system architecture innovations include the Twin server, double-sided storage and SuperBlade® product families. Offering the most comprehensive product lines in the industry, Supermicro provides businesses of all sizes with energy-efficient, earth-friendly solutions that deliver unmatched performance and value. Founded in 1993, Supermicro is headquartered in Silicon Valley with worldwide operations and manufacturing centers in Europe and Asia.

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[June 14, 2010]

Wall Street News Alert: Trade Alert: NLST, FRPT

Miramar, FLA., Jun 14, 2010 (M2 PRESSWIRE via COMTEX) -- Wall Street News Alert is issuing its "Daily Market Movers Report" for Monday morning. The list includes: Netlist, Inc. (NASDAQ: NLST) and Force Protection, Inc. (NASDAQ: FRPT).

Story continues below ↓

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For more information, please visit www.WallStreetNewsAlert.com.

Netlist, Inc. (NASDAQ: NLST) Netlist, Inc. (NASDAQ: NLST) closed Friday up 29.63% on over 2.1 million shares traded.

June 11, 2010 - Netlist, Inc. (NASDAQ: NLST), designer and manufacturer of high-performance memory subsystems, announced that its HyperCloud memory module has been selected to run on Viglen servers to support High Performance Computing (HPC) applications. Viglen is a leading British manufacturer and provider of IT solutions within the education and public sector.

"Netlist's HyperCloud memory uniquely increases aggregate memory bandwidth within our servers to support our customer's workload demands without memory bottlenecks," said Bordan Tkachuk, CEO of

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Viglen. "Viglen continues to empower our customer's IT estates with new HPC technologies. This differentiated capability improves simulation times with large data sets and increases overall server utilization in HPC applications." HyperCloud leverages the benefits of Netlist's patented load reduction and rank multiplication technology to improve overall server performance. Offering higher capacity to support memory intensive workloads, such as HPC simulations, HyperCloud serves as a cost-effective solution by lowering operating expenses for datacenters.

About the company: Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for the server and high-performance computing and communications markets. The Company's memory subsystems are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, and telecommunication equipment. Netlist was founded in 2000 and is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China.

Force Protection, Inc. (NASDAQ: FRPT) Force Protection, Inc. (NASDAQ: FRPT) closed Friday down 1.89% on 628,300 shares traded.

June 14, 2010 - Force Protection, Inc. (NASDAQ: FRPT), a leading designer, developer and manufacturer of survivability solutions and provider of total life cycle support for those products, today announced it has received a modification to contract M67854-07-D-5031 from the United States Marine Corps Systems Command for additional modernization of the U.S. military's Cougar fleet. The approximate $10.8 million firm, fixed price contract modification includes the design and purchase of 2,654 570-amp alternator kits and related materials. Work will be performed in Ladson, SC, with deliveries scheduled to begin in October 2010 and be completed by March 2011.

About the company: Force Protection, Inc. is a leading designer, developer and manufacturer of survivability solutions, including blast- and ballistic-protected wheeled vehicles currently deployed by the U.S. military and its allies to support armed forces and security personnel in conflict zones. The Company's specialty vehicles, including the Buffalo, Cougar and related variants, are designed specifically for reconnaissance and urban operations and to protect their occupants from landmines, hostile fire, and improvised explosive devices (IEDs, commonly referred to as roadside bombs). The Company also develops, manufactures, tests, delivers and supports products and services aimed at further enhancing the survivability of users against additional threats. In addition, the Company provides long-term life cycle support services of its vehicles that involve development of technical data packages, supply of spares, field and depot maintenance activities, assignment of highly-skilled field service representatives, and advanced on and off-road driver and maintenance training programs.

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Netlist Inc. (NASDAQ: NLST) $74M (MarketCap) Trading at +20%

20 tweets

Date: June 14, 2010 2:39 PM
Publisher: Ashley Montgomery
Categories: US Markets
Tags: Computer Networks, Computer Services, NASDAQ, NLST, World Market Media

NETLIST

Founded in 2000, Netlist, Inc. is a designer and manufacturer of high-performance, logic-based memory subsystems for the server and high-performance computing and communications markets. The company's memory subsystems are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. Netlist's product, HyperCloud, leverages the benefits of Netlist's patented load reduction and rank multiplication technology to improve overall server performance. It serves as a cost-effective solution by lowering operating expenses for datacenters, offering higher capacity to support memory intensive workloads such as HPC simulations. C.K. Hong, Netlist Chief Executive Officer comments, "Our HyperCloud technology is a key enabler of server efficiency and offers a unique value-add for companies deploying new IT infrastructures."

On June 11th, the company announced that its HyperCloud™ memory module has been selected to run on Viglen servers to support High Performance Computing (HPC) applications. Viglen is a leading British manufacturer and provider of IT solutions within the education and public sector. By incorporating HyperCloud DIMMs into their servers, Viglen has achieved several benefits, including improving aggregate memory bandwith and increasing data throughput by 57%. Following the announcement, its shares rallied nearly 30%. The company's shares continued to rally, jumping by 35 cents, or 14.3 %, to $2.80 in the Monday premarket session. Currently, Netlist's shares are trading at $2.96, up $.51 or 20.82%.

"Netlist's HyperCloud memory uniquely increases aggregate memory bandwidth within our servers to support our customer's workload demands without memory bottlenecks," said Bordan Tkachuk, CEO of Viglen. "Viglen continues to empower our customer's IT estates with new HPC technologies. This differentiated capability improves simulation times with large data sets and increases overall server utilization in HPC applications."

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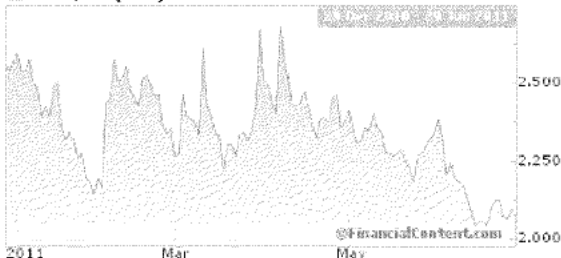
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Bio-Clean International, Inc. (OTC Pink: BCLE) Up Big as Stocks Dip

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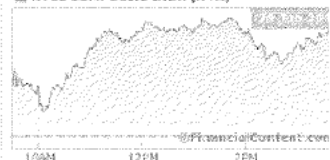
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Netlist Accelerates MSC Software Simulation Performance

Claims HyperCloud memory module boosts simulation speed by 21%.

by DE Editors | Published October 11, 2010

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Netlist, Inc. has announced that its HyperCloud memory module is accelerating the performance time of **MSC Software** finite element analysis (FEA) simulations. Overcoming memory constraints due to the large number of floating point calculations and large models in every analysis or simulation project, HyperCloud is reducing simulation times for MSC Software applications by 21%, according to the company.

"Using HyperCloud with our Nastran FEA simulations enables us to eliminate the high levels of input/output wait times and run complex simulations, with large models, greater than 15 million degrees of freedom, faster," says Joe Griffin, development engineer of MSC Software. "This has led to an overall increase in productivity and the ability to conduct more simulations at a given time per server. With HyperCloud, we also are able to conduct high-performance testing of critical parts and assemblies for products like automobiles and planes, and further design enhancements while decreasing design times."

Scientific modeling, financial analysis, and engineering design users can now launch multiple runs per day and run multiple jobs on a standard two-processor server, thereby increasing design productivity. Traditionally, these workloads require complex multi-node clusters which lead to increased datacenter costs.

"MSC Software's validation of the performance benefits that HyperCloud delivers to high-performance computing applications is helping engineers solve their most complex design problems," says Steve McClure, vice president of marketing at Netlist. "We are excited to work alongside MSC Software in removing the memory barriers our mutual customers encounter when modeling complex real world aerodynamic, mechanical impact, or heat transfer interactions."

Additionally, with HyperCloud, MSC Software is now able to more accurately analyze structural responses to design factors, such as stress, strain, vibration, displacement and temperature. HyperCloud allows memory to be populated at higher densities and speeds versus standard JEDEC RDIMMs, according to Netlist. The company says HyperCloud reduces cache misses that are common when simulating large models.

For more information, visit **Netlist**.

Sources: Press materials received from the company and additional information gleaned from the company's website.

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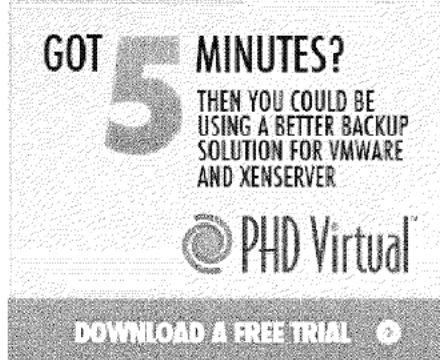
Netlist, Inc., a designer and manufacturer of high-performance memory subsystems, today announced that its HyperCloud memory module is now part of the MDS Micro Cloud Matrix. The MDS Micro Cloud Matrix provides modular server-based computing blocks that contain core datacenter hardware within a single enclosure including VMware-certified QUADv servers with mass local storage.

Cloud computing infrastructure is often based on elastic hardware platforms that allow on-demand access to virtual machines of varying sizes. This requires that memory, the central processing unit (CPU), and disks be maximized to full potential on each server. HyperCloud increases server utility by maximizing memory instead of adding more CPUs.

"Netlist's offering is unique in that it directly addresses the memory slowness that customers face on a server platform with a large amount of memory," said Tim Myers, senior architect of VMware. "Instead of the speed being reduced, they are able to maintain the faster speeds which provides a better opportunity for customer satisfaction."

With the incorporation of HyperCloud, MDS Micro is now able to provide increased server utility for virtualization applications in the Cloud.

"HyperCloud memory enables the Cloud Matrix to deliver efficient server compute blocks," said Karriem Adams, vice president of sales at MDS Micro. "We've seen significant interest in our Cloud Matrix solution for virtualization applications and we're in need of a technology that can effectively support demanding memory requirements. When evaluating memory solutions, Netlist was the clear winner for its ability to help increase server utility in our Cloud Matrix."

Certification of HyperCloud memory modules on MDS Micro's QUADv for the Cloud Matrix increases server performance to its full potential and enables up to 768GB of memory running at 1333 MT/s.

"Selection by MDS Micro is validation that HyperCloud enables more efficiency in virtualization environments," said Steve McClure, vice president of worldwide sales and marketing at Netlist. "We are excited to work with MDS Micro on delivering compelling server solutions to support the industry's growth in virtualization and cloud computing applications."

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Netlist will demonstrate HyperCloud memory in the MDS Micro QUADv server at the Supercomputing show, taking place November 15-18 at the Morial Convention Center in New Orleans, in booth number 4223.

Details on the Cloud Matrix can be found at: http://www.mdsmicro.com/sol_cloudmatrix.php

HyperCloud product information can be found at: www.netlist.com/hypercloud

Published Monday, November 15, 2010 5:32 AM by David Marshall
Filed under: Cloud

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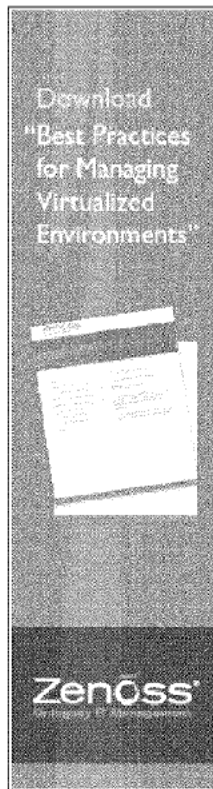
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BREITBART⊚COM

Red Bull Racing Revs Up Formula 1 Race Car Simulations with Netlist's HyperCloud Memory

Dec 15 07:00 AM US/Eastern

PR Newswire
United Business Media

IRVINE, Calif., Dec. 15, 2010 /PRNewswire/ -- Netlist, Inc. (Nasdaq: NLST), a designer and manufacturer of high-performance memory subsystems, today announced that its HyperCloud™ memory module is revving up the performance of Red Bull Racing's Formula 1 Racing Car simulations, which includes Computational Fluid Dynamics (CFD). HyperCloud overcomes the memory constraints associated with CFD simulations and large complex models.

"In Formula 1, we continually need to leverage technologies that can help us innovate," said Nathan Sykes, computational fluid dynamics manager at Red Bull Racing. "Using HyperCloud with our CFD simulations allows us to significantly increase our Formula 1 design productivity. With HyperCloud, we achieve 60 percent greater server utilization and are now running multiple jobs per machine. Launching multiple jobs on one machine increases the number of simulations which can be built on existing hardware, increasing the design throughput of the CFD department."

To enhance the accuracy of its simulation tests, Red Bull Racing leverages the benefits of CFD, which utilizes complex numerical methods and algorithms to analyze and solve problems that involve fluid flows. HyperCloud memory maximizes the performance and productivity of these aerodynamic modeling simulations which are memory intensive and require high-end servers to achieve sufficient performance to complete this level of analysis. Currently, Red Bull Racing uses ANSYS CFD simulation software running on HP DL380 servers configured with 16GB HyperCloud memory.

"Red Bull Racing is yet another example of how the high performance computing benefits of HyperCloud memory are significantly reducing the time spent on complex simulations," said Steve McClure, vice president of worldwide sales and marketing at Netlist. "We are excited to be a part of Red Bull Racing's compute platform and look forward to a longstanding relationship."

HyperCloud product information can be found at: www.netlist.com/hypercloud.

About Netlist:

Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for datacenter server and high-performance computing and communications markets. Netlist's flagship products include HyperCloud Memory, which breaks traditional memory barriers and NetVault, a flash memory-based subsystem that enables data retention weeks following a disaster. The memory technologies are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, and telecommunication equipment. Founded in 2000, Netlist is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China. For more information, visit the company's website at www.netlist.com.

Safe Harbor Statement:

This news release contains forward-looking statements regarding future events and the future performance of Netlist. These forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those expected or projected. These risks and uncertainties include, but are not limited to, continuing development, qualification and volume production of NetVault™ NV and HyperCloud™; the rapidly-changing nature of technology; risks associated with intellectual property, including the costs and unpredictability of litigation over infringement of our intellectual property; volatility in the pricing of DRAM ICs and NAND; changes in and uncertainty of customer acceptance of, and demand for, our existing products and products under development, including uncertainty of and/or delays in product orders and product qualifications; delays in the Company's and its customers' product releases and development; introductions of new products by competitors; changes in end-user demand for technology solutions; the Company's ability to attract and retain skilled personnel; the Company's reliance on suppliers of critical components; fluctuations in the market price of critical components; evolving industry standards; and the political and regulatory environment in the People's Republic of China. Other risks and uncertainties are described in the Company's annual report on Form 10-K, dated February 19, 2010, and subsequent filings with the U.S. Securities and Exchange Commission made by the Company from time to time. Except as required by law, Netlist undertakes no obligation to publicly update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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NETLIST

Cirrascale Qualifies HyperCloud™ Memory on Blade Server

HyperCloud memory improves EDA simulation runtime, speeding complex semiconductor development cycles and reducing design risk

IRVINE, Calif., April 28, 2011 – Netlist, Inc. (Nasdaq: NLST), a designer and manufacturer of high-performance memory subsystems, today announced that its 8GB and 16GB HyperCloud™ memory modules are qualified by Cirrascale, a premier developer of build-to-order, independent blade-based computing and storage data center infrastructures. Qualified specifically on Cirrascale's VB1325 blade server, HyperCloud supports memory intensive applications such as electronic design automation (EDA) and high performance computing (HPC) simulations. In addition, EDA and cloud computing thought leader Deopli Corporation benchmarked Cirrascale's HyperCloud configured server showing significant performance improvements.

"With HyperCloud memory, we are now able to improve simulation productivity for our customers while supporting the increased test demands of memory intensive EDA applications," said Dave Driggers, founder, CEO and CTO of Cirrascale. "HyperCloud ensures that we are maximizing server utilization, which in turn helps us to run more complex simulation models than ever before on a 2P server. The integration of HyperCloud positions us to support and develop new levels of HPC with increased performance gains for our customers on industry standard servers."

Higher memory capacities and speeds allow faster simulation times in HPC applications such as EDA. This performance benefit can increase productivity, improve design cycle times and reduce design risk.

"Cirrascale's VB1325 running 288GB at 1333MT/s allowed us to benchmark the performance gains EDA users can expect to see when using HyperCloud," said Scott Clark, president and CEO of Deopli Corporation. "With Cirrascale's HyperCloud configuration, simulation runtimes of memory intensive applications can be reduced on average by 15%. This has the potential to accelerate key portions of the design cycle, thereby reducing design risk and delivering more efficient use of the very expensive backend tools during System On Chip runs. Cirrascale's HyperCloud configuration will enable designs to successfully complete with fewer licenses. The cost of most of these licenses are in the hundreds of thousands of dollars. Therefore the avoidance of purchasing a single license will deliver an immediate ROI."

"Cirrascale's qualification and Deopli's EDA runtime benchmarks of HyperCloud highlight the significant end user benefits that HyperCloud delivers to HPC," said Steve McClure vice president of worldwide sales and marketing of Netlist. "HyperCloud breaks traditional memory speed and capacity limitations. Delivering 288GB at 1333MT/s in a dual Intel 5600 processor server provides Cirrascale's EDA customers a significant advantage in time to market and total project costs by reducing simulation runtimes."

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Cirrascale is currently in production with its VB1325 server blade, offering 8GB and 16GB HyperCloud memory. Additional information on Cirrascale's VB1325 can be found at http://cirrascale.com/serverblades.asp.

Additional information on Netlist's HyperCloud, and the Deopli whitepaper entitled "Mastering EDA Environments with High Performance Memory Technology" can be found at www.netlist.com\hypercloud.

About Cirrascale:
Cirrascale Corporation is a premier developer of independent blade-based cloud computing and cloud storage platforms for conventional and containerized data centers that are defining a new era in the green data center. Cirrascale provides the industry's most energy-efficient and reliable standards-based solutions with the lowest possible total cost of ownership in the absolute densest form factor due to its patented Vertical Cooling Technology. Cirrascale sells directly to large-scale infrastructure operators and managed services providers, and through resellers and distributors to HPC and Cloud segments. Cirrascale also licenses its award winning systems-level designs to technology partners globally. To learn more about Cirrascale and its unique data center infrastructure solutions, please visit http://www.cirrascale.com or call (888) 942-3800.

About Deopli:
Deopli is one of the foremost thought leaders in the EDA infrastructure and cloud computing space. Composed of highly-trained personnel, equipped with technology and experience, operating under principles of self-sufficiency, technical competence, speed, efficiency and close teamwork. Providing advisory and consulting services to EDA companies with respect to their HPC environments, they also conduct specialized operations including reconnaissance, strategy definition, tactical definition and resource training. In addition, Deopli executes non-operational, high-risk tasks to achieve significant strategic objectives. Deopli is headquartered in Irvine, California. For more information, visit www.deopli.com.

About Netlist:
Netlist, Inc. designs and manufactures high-performance, logic-based memory subsystems for datacenter server and high-performance computing and communications markets. Netlist's flagship products include HyperCloud Memory, which breaks traditional memory barriers and NetVault, a flash memory-based subsystem that enables data retention weeks following a disaster. The memory technologies are developed for applications in which high-speed, high-capacity memory, enhanced functionality, small form factor, and heat dissipation are key requirements. These applications include tower-servers, rack-mounted servers, blade servers, high-performance computing clusters, engineering workstations, telecommunication equipment, and other Industrial grade applications. Founded in 2000, Netlist is headquartered in Irvine, California with manufacturing facilities in Suzhou, People's Republic of China. For more information, visit the company's website at www.netlist.com.

Safe Harbor Statement:
This news release contains forward-looking statements regarding future events and the future performance of Netlist. These forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those expected or projected. These risks and uncertainties include, but are not limited to, continuing development, qualification and volume production of EXPRESSvault™, NVvault™ and HyperCloud™; the rapidly-changing nature of technology; risks associated with intellectual property, including the costs and unpredictability

of litigation over infringement of our intellectual property and the possibility of the Company's patents being re-examined by the United States Patent and Trademark office; volatility in the pricing of DRAM ICs and NAND; changes in and uncertainty of customer acceptance of, and demand for, our existing products and products under development, including uncertainty of and/or delays in product orders and product qualifications; delays in the Company's and its customers' product releases and development; introductions of new products by competitors; changes in end-user demand for technology solutions; the Company's ability to attract and retain skilled personnel; the Company's reliance on suppliers of critical components; fluctuations in the market price of critical components; evolving industry standards; and the political and regulatory environment in the People's Republic of China. Other risks and uncertainties are described in the Company's annual report on Form 10-K, dated March 3, 2011, and subsequent filings with the U.S. Securities and Exchange Commission made by the Company from time to time. Except as required by law, Netlist undertakes no obligation to publicly update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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# # #

Tab CL-O
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NETL.018RX1 / NETL.018RX6 / NETL.018RX7   PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee	: Bhakta et al.
Inter Partes Reexamination No.	: 95/000,578; 95/000,579; 95/001,339
Filing Date	: October 20, 2010; October 21, 2010; June 8, 2010
For	: MEMORY MODULE DECODER
Group Art Unit	: 3992
Confirmation No.	: 5035

DECLARATION OF DR. CARL SECHEN UNDER 37 C.F.R. § 1.132

Mail Stop Inter Partes Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

    I, Dr. Carl Sechen, declare as follows:

    1. I have been retained by Netlist, Inc., the owner of U.S. Patent No. 7,619,912 ("the '912 patent") to provide a technical opinion concerning the '912 patent, and certain prior art references cited in the above-captioned *inter partes* reexamination proceedings, which are discussed in further detail below.

    2. I have been a Professor of Electrical Engineering for approximately 25 years. Since August 15, 2005, I have been a Professor of Electrical Engineering at the University of Texas at Dallas. From July 1992 to August 2005, I was a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I was a Professor of Electrical Engineering at Yale University. Over these years my research has focused on the design and

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computer-aided design of digital integrated circuits, including the design of DRAM. I have
taught numerous students how to design DRAM memories as part of the design courses that I
have offered. I have authored or co-authored 158 papers, one book, and two patents. More
information about my academic work can be found in my curriculum vitae, which is attached as
Exhibit A.

3. I taught Verilog design to undergraduate students at the University of Washington
and at the University of Texas at Dallas since 2001. After taking this course, these undergraduate
students would easily comprehend the Verilog code presented in the '912 patent.

4. I earned a B.E.E. degree in Electrical Engineering from the University of Minnesota
in 1975. After that, I went on to the Massachusetts Institute of Technology, where I earned an
M.S. degree in Electrical Engineering. I was awarded a Ph.D. in electrical engineering from the
University of California at Berkeley in 1986. More details about my education are set forth in
my attached curriculum vitae. See Exhibit A.

5. In 2002, I was elected as a Fellow of the Institute of Electrical and Electronic
Engineers (IEEE). In 2002 I also received the Outstanding Research Advisor Award from the
Department of Electrical engineering and the University of Washington and the Best Project
Award from the NSF Center for the Design of Digital and Analog ICs. I also received a
Distinguished Teaching Award from the University of Texas in 2008. I also received the
Semiconductor Research Corporation's Inventor's Recognition Award in 2001 for the
development of output prediction logic. I received the 1994 SRC Technical Excellence Award,
and also received the Semiconductor Research Corporation's 1988 SRC Inventor's Award.
Additional honors and awards are set forth in my CV. See Exhibit A.

6. I am being compensated at a rate of $300 per hour by the patent owner for my
assistance in connection with the above-captioned *inter partes* reexamination proceedings, and
all activities in connection with the preparation of this declaration. I am being paid regardless of
the conclusions or opinions I reach. I have no personal or financial stake or interest in the
outcome of the present reexaminations.

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7.   I have reviewed and am familiar with the specification the '912 patent. I have reviewed and am familiar with the Office Action dated April 4, 2011 issued by the U.S. Patent and Trademark Office ("USPTO") in the reexamination proceedings against the '912 patent ("the '912 Office Action").

8.   I have also reviewed and am familiar with the prior art cited in the '912 Office Action and relied upon by the Examiner to reject one or more claims. This prior art includes:

- U.S. Patent No. 5,926,827 ("Dell 1");

- U.S. Patent No. 6,209,074 ("Dell 2");

- *Quad Band Memory (QBM^{TM}): DDR 200/266/333 devices producing DDR400/533/667*, QBM Alliance, Platform Conference, San Jose, California, January 23-24, 2002 ("QBMA");

- U.S. Patent No. 5,745,914 ("Connolly");

- U.S. Patent No. 6,414,868 ("Wong");

- U.S. Patent Application Publication No. 2006.0117152 ("Amidi");

- *Design Specification for PC2100 and PC1600 DDR SDRAM Registered DIMM*, JEDEC Standard No. 21-C, Revision 1.3, Release 11b, January 2002, ("JEDEC 21C");

- *Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications*, JEDEC Standard No. 82-4B, May 2003, ("JEDEC 82-4B");

- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79C, March 2003, ("JEDEC 79C");

- Micron, *DDR SDRAM RDIMM*, MT36VDDF12872 & MT36VDDF28672 Data Sheet © 2002, ("Micron");

I will refer to the three JEDEC references listed above collectively as "JEDEC" or "JEDEC Standards" herein.

9.   I have also reviewed and am familiar with the declaration of Christoforos Kozyrakis filed in connection with the '912 reexamination proceedings ("Kozyrakis '912 Decl."), and the declaration of Bruce Jacob filed in connection with the '912 reexamination proceedings ("Jacob '912 Decl.").

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10. I understand that U.S. patent law interprets patents and prior art from the point of view of a hypothetical person of ordinary skill in the art ("POSITA"). In his declarations Dr. Kozyrakis has proposed that, with regard to the '912 patent, such a POSITA would have "an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market," all as of the priority filing date of the '912 patent. Although I do not necessarily agree with Dr. Kozyrakis' definition of a POSITA in the technical field pertaining to the '912 patent, for purposes of my analysis and discussion herein, I have adopted Dr. Kozyrakis' definition of a POSITA.

11. Based on my educational background and work experience, I am and was familiar with the technology at issue as of the 2004-2005 timeframe in which the parent applications of the '912 patent were filed. My educational background and experience also allow me to evaluate what knowledge a POSITA, as defined above, would have because I have taught and worked with many people with similar qualifications. I believe I am familiar with what such a POSITA would understand from reading the '912 patent, or a particular reference. In this declaration, when discussing what a document discloses or suggests, I am describing what I believe a POSITA would have understood as being disclosed or suggested by the document.

12. Generally, the '912 patent discloses and claims a memory module that simulates a smaller number of larger memory devices using a larger number of smaller memory devices. In other words, the memory module uses a first number of ranks of memory devices ("actual physical memory devices") to simulate a second number of ranks of memory devices ("logical memory devices"), wherein the first number of ranks is larger (e.g., 2X larger) than the second number of ranks, and each actual physical memory device has a capacity that is smaller (e.g., 2X smaller) than the capacity of one logical memory devices. (See, e.g., '912 patent, col. 2, lines 61-66.) The '912 patent describes a variety of significant advantages provided by the new memory module technology: (i) They enable technological advances using "next-generation" high capacity memory modules that would otherwise be unachievable using available memory devices ('912-Col.22-lines 5-9 and Col 32 lines 44-51) (ii) They increase flexibility in system board design by allowing a memory module, as taught by '912 patent, to be used with computer

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systems that are designed for different or limited (small) number of ranks ('912-Col.32-lines31-36 and lines 39-44). (iii) They increase the memory capacity or memory density per memory slot or socket on the system board of the computer system ('912-Col.32-lines 26-29, and lines 39-44). (iv) They increase the total available memory capacity in systems with a limited number of memory slots ('912-Col.32-lines 29-31). (v) They advantageously reduce the total cost of the resultant memory module using a larger number of smaller memory devices to achieve the same memory capacity as a smaller number of larger memory devices. That's because the cost of recently developed devices with twice the capacity of previous devices are usually substantially more than double. (See, e.g., '912 patent, col. 4, line 42 to col. 5, line 5; col. 32, lines 20-26.)

I.   The '912 Patent

13. Claim 1 of the '912 patent presented below is directed to a representative embodiment of a memory module design and logical addressing scheme.

> 1.   (Original)   A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, *the logic element receiving a set of input control signals* from the computer system, the set of input control signals *comprising* at least one row/column address signal, *bank address signals,* and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, *the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,* the circuit generating

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a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a ***phase-lock loop device*** mounted to the printed circuit board, the phase-lock loop device ***operatively coupled to*** the plurality of DDR memory devices, ***the logic element***, and the register.

(Claim 1 of the '912 patent, emphasis added.)

14. As highlighted in claim 1 above, one feature required by the claimed invention is that the "logic element" of the memory module receives input control signals that include "bank address signals." Providing the bank address signals to the logic element, in combination with the other signals (e.g., CS, A_{n+1}) allows the logic element to identify the actual rank of memory devices that is desired to be accessed. By knowing which bank address is associated with a read or write command, the logic element can identify which of two or more actual physical ranks of memory devices should be accessed, wherein the two or more actual physical ranks of memory devices is viewed as a single rank from the perspective of the computer system. As one example of how bank address signals can be used in the present invention, the '912 patent discloses Verilog code specifying that bank address signals are provided to the logic element to determine which output control signals, including rank-selecting signals, to generate and transmit to the DDR memory devices (see, e.g., '912 patent at col. 17, l. 32 – col. 19, l. 52). As another example, based on the '912 patent specification, when performing back-to-back adjacent read operations, one of ordinary skill in the art would know that the computer system inserts one or

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more idle (dead) cycles when a change of CS (chip select) occurs during continuous read operations, indicating that the sequential memory access is taking place across the physical memory device boundaries. The '912 patent teaches how to design the logic element that supports back-to-back access by recognizing (based on the bank address) the memory device boundary that the computer system is not aware of. (See '912 patent specification, col. 24, lines 1-9.) Thus, after reviewing the '912 patent specification, a POSITA would clearly understand how bank address signals are used in the present invention. As discussed in further detail below, none of the cited prior art discloses or suggests supplying "bank address signals" to a logic device for performing address translation functions. Indeed, none of the cited prior art discloses or suggests using bank address signals at all to generate a new set of control signals.

15. Additionally, as highlighted in claim 1 above, another feature required by the claimed invention is that the logic element is "operatively coupled" to the phase lock loop device of the memory module. As shown in Figure 1 of the '912 patent, for example, the output of the PLL 50 is directly coupled to both the logic element 40 and the register 60. Based on the '912 patent specification, it is my opinion that a POSITA would understand that "operatively coupled" in the context of claim 1 of the '912 patent means that the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PLL 50. In other words, the output of the PLL 50 controls the operation of the logic element 40.

16. By providing a single, common clock from the PLL 50 to both the logic element 40 and the register 60, the memory module of claim 1 of the '912 patent is configured to provide reliable synchronous operation. Although prior art memory modules could also achieve synchronous operation, none of the cited references disclose providing a common clock output directly from the PLL to both the register and logic element of a memory module. Instead, Amidi, for example, couples only its register to the PLL clock output while its logic device is clocked by a system clock, which was due to applicable industry guidelines at the time. As explained in further detail below, a POSITA would not have been motivated or inclined to change the design of these prior art memory modules because doing so would have significantly affected the timing margins for synchronous operation of the memory modules, and likely would render the prior art memory modules inoperable or unreliable. Adding a load (e.g., a logic device) to the PLL output would have greatly impacted performance, and would have required

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significant redesign of the memory module layout in order to achieve accurate synchronous operation and reliability.

17. Amidi merely discloses using a PLL in a Zero-Delay Buffer. A Zero-Delay Buffer is a component with well-tuned multiple clock outputs for a given memory module reference design, where each clock output is well matched to the number of loads (e.g., memory devices) it drives as well as to the transmission line effects due to the variations in the placement of these loads on the printed circuit board of the memory module. The Zero-Delay Buffers employ PLL circuitry to match the phase of each of the output clock signals to the input clock signal and are extremely sensitive to changes in loading or layout. In general, the personal computer industry has recognized that while memory modules from different manufacturers may individually meet the technical requirements of JEDEC standard specifications, these memory modules either exhibited intermittent failures or failed to inter-operate with other memory modules. A consortium of industry leaders (e.g., Intel and other DRAM device, memory module and system manufacturers) adopted a more stringent set of standards for the 100 MHz SDRAM memory, and was released as the PC100 standard. The PLL performance was determined to be a major cause of these failures. Very stringent and detailed technical specifications were adopted and continue to be monitored and updated by JEDEC (e.g., see JEDEC 21-C page 4.20.4-24 and JEDEC JC-40). To guarantee robustly operating memory modules, system level manufacturers including Intel and JEDEC have released and continue to release memory module reference designs with strict layout, component placement and qualification guidelines to be adopted by memory module manufacturers. Adding a load (e.g., a logic device) to one PLL output clock and all the associated changes and modifications required would have greatly impacted the Zero-Delay Buffer's ability to transmit a tuned and balanced replica of the input clock signal to all the memory devices resulting in memory module failure or degraded performance causing intermittent or inter-operability failures. Very significant redesign and qualification efforts would be required before such an altered memory module could be qualified to achieve accurate and reliable operation.

A.   **None of the Cited Prior Art Discloses or Suggests Providing Bank Address Signals to the Logic Device**

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18. As shown in Figure 1 of the '912 patent, reproduced below, bank address signals "BA_0 - BA_m" are provided directly to an input of the logic element 40, which then utilizes the bank address signals to perform address translation functions and translate logical addresses, as viewed by the computer system, to actual physical memory addresses for activating a selected physical rank, and performing read/write operations onto the selected physical rank.

Figure 1A:
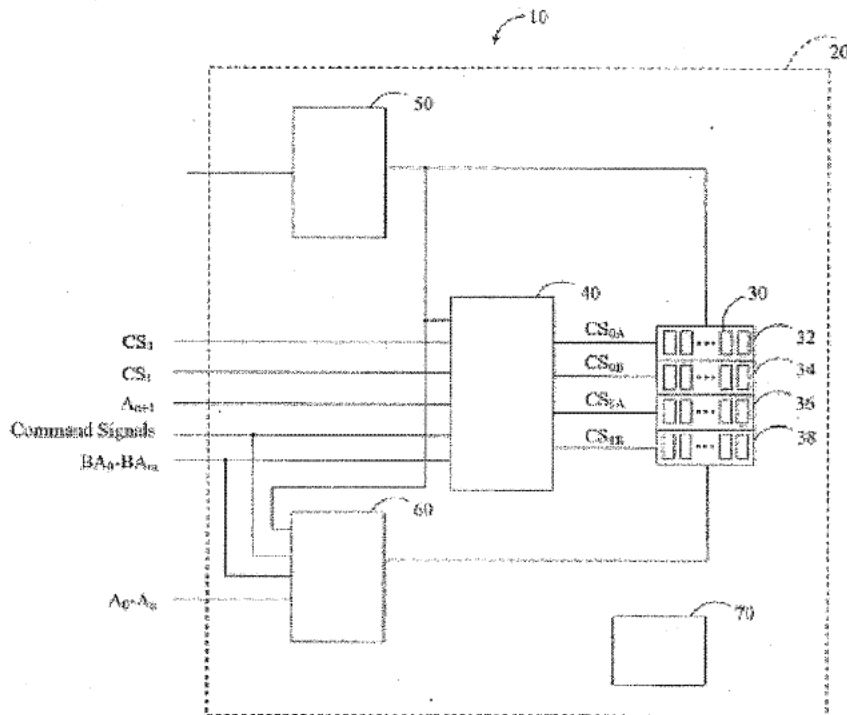
1.   Amidi

19. It is my understanding that one or more Requesters seek to interpret the term "logic element" to be the combination of a decoding or conversion logic device (e.g., the CPLD of Amidi) and a separate register that is operatively coupled to a PLL device (e.g., the register of Amidi). In my opinion, such an interpretation of "logic element" in the context of claim 1 of the '912 patent is incorrect. A person of ordinary skill in the art would understand that the term "logic element" implies something inherently different than the term "register". A logic element is understood to be combinational logic or a finite state machine (the latter may include one or

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more flip-flops). Meanwhile, a register is dominated by state-holding devices such as flip-flops, along with a small amount of control logic. The primary purpose of a register is to receive, store (for one or more clock cycles) and output signals. Also, the outputs of a register were previous inputs to it. In contrast, the outputs of a logic element are computationally derived from current and previous inputs. A logic element controls or computes (e.g., decodes or translates) data whereas a register stores data. It is therefore clear that these two terms of art describe very different types of circuitry that do very different things. Based on the '912 patent specification, and the language of claim 1, a POSITA would understand that the "logic element" performs the function of using incoming signals intended to access the logical memory locations targeted by the computer system to generate output control signals to instead access the actual physical memory devices. Neither registers disclosed by the '912 patent or Amidi, for example, are involved in such translating functions. Even making the incorrect assumption that Amidi's register was somehow considered to be part of the recited "logic element," Amidi still does not teach or suggest translating bank address signals to generate a new set of output control signals to access actual memory addresses.

20. The '912 patent describes "the logic element" and "the register" as being distinct entities with distinct functions (see, e.g., '912 patent at col. 5, ll. 31-36; col. 6, ll. 55-63; col. 7, ll. 43-46). While the '912 patent discloses that these distinct entities may be parts of a single component ('912 patent at col. 5, ll. 37-42), such packaging does not merge or otherwise affect the distinct functions performed by the logic element and the register. The '912 patent describes the functionality of the logic element and provides various implementation examples, including exemplary software (Verilog) code that can be synthesized to an actual physical hardware logic element, see col. 14 lines 17-25, col. 17-18, and Code Examples 1 and 2 col. 13 through 20. In contrast, the register as a component of a memory module possesses well-defined electrical and timing specifications as published by the JEDEC standard (e.g. JESD82-4B) and a POSITA would be well aware of the register functionality and application use in a memory module. A POSITA would still consider the logic element and the register to be distinct from one another, even if they were both contained in a single package. Thus, persons of ordinary skill in the art would not interpret the "logic element" of the claims as encompassing both the conversion logic device and the register that passes signals onto the DRAM devices.

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21. In Amidi, the conversion logic device and the register are also disclosed as being separate devices, each receiving sets of input signals having different functions to (i) operate on the sets of input signals and (ii) produce different output signals to the memory devices, while having their respective operations timed to different clock signals. (see, e.g., Amidi at ¶¶ 50, 58; Figs. 6A, 6B.) A person of ordinary skill would not interpret Amidi's register to be part of a "logic element" that translates a first set of chip select, row/column and bank address signals to generate a set of output control signals, as recited in claim 1 of the '912 patent. As discussed above, the register does not perform any translation functions. Also, one of ordinary skill in the art would not refer to a register as a logic element.

22. For the reasons discussed above, the register of Amidi is not part of a "logic element" for performing translation functions, as recited in claim 1 of the '912 patent. Thus, Amidi fails to disclose a "logic element" that receives and translates "bank address signals" as required by claim 1 of the '912 patent.

23. Furthermore, it would not be obvious to a POSITA to modify Amidi's system by providing the bank address signals to the CPLD device. Amidi does not discuss any rationale for making this modification, since the CPLD is disclosed by Amidi as being fully functional without having these bank address signals received by the CPLD. For example, Amidi at Fig. 8 and ¶¶ 64-70 discloses an internal circuitry of the CPLD that does not utilize the bank address signals at all. Amidi discloses that the register receives the bank address signals so that they can be passed through to the DDR memory devices for their normal function of specifying the bank from which data is to be read or written. In fact, Amidi consistently and unambiguously teaches that only the CS0, CS1 and an extra address bit are used to determine which rank is to be activated, which teaches away from the claimed invention of the '912 patent. Thus, a POSITA would not have been motivated to add bank address signals in addition to the row and column address signals to Amidi's system to generate control signals for accessing actual physical memory locations.

24. In contrast to Amidi, the claimed invention of the '912 patent provides the bank address signals to the logic element to be used in determining which output control signals, including rank-selecting signals, to generate and transmit to the DDR memory devices. The

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bank address signals are not simply clocked through the logic element, as would have been the case if the logic element provided the function of the register. These translation procedures and structures using bank address signals were not taught by Amidi or any of the other cited references, and would not have been known or foreseen by a POSITA until after reading the '912 patent specification. Thus, a POSITA would not have found it obvious to modify Amidi to produce the claimed invention.

2.   Amidi Combined with Dell 2

25. As discussed above, Amidi does not disclose or render obvious a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39. Dell 2 does not cure this deficiency of Amidi.

26. However, besides that, it is my opinion that a POSITA would not find it obvious to modify Amidi using the system disclosed by Dell 2. First, Amidi and Dell 2 are directed to opposing problems. Amidi is concerned with using more ranks of <u>cheaper, low-capacity</u> memory devices in place of fewer ranks of <u>more expensive, higher-capacity</u> memory devices to achieve cost savings (see, Amidi at ¶ 8, 11). In contrast, Dell 2 is concerned with using memory devices with more internal banks, which are generally <u>more expensive</u>, to replace cheaper memory devices with fewer internal banks (see, Dell 2 at col. 4, ll. 48-51). Using memory devices with more internal banks as disclosed by Dell 2 would be counterproductive to Amidi's goal of achieving cost savings, so a POSITA would not be motivated to modify Amidi using the disclosure of Dell 2.

27. Furthermore, Amidi and Dell 2 address their respective problems in different ways. Amidi addresses its problem by generating a larger number of chip-select signals for the larger number of ranks of memory devices using the smaller number of chip-select signals and an otherwise unused row/column address bit. In contrast, Dell 2 addresses its problem without generating any additional signals. Instead, Dell 2 merely teaches to connect a row/column address bit to become an additional bank address pin of DRAMs. In other words, the row/column address bit is used differently by Amidi (i.e., decoding the row/column address bit along with the received chip-select signals to generate a larger number of chip-select signals) than by Dell 2 (i.e., re-mapping the row/column address bit to become a bank address bit).

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Because these solutions are significantly different from one another, persons of ordinary skill in the art would not find it obvious to modify Amidi using the disclosure of Dell 2.

3.   Amidi Combined with JEDEC 21-C

28. For reasons similar to those discussed above with regard to Amidi, persons of ordinary skill would not interpret JEDEC 21-C's register as being a "logic element," so JEDEC 21-C does not include a logic element that receives a set of input control signals comprising bank address signals. Furthermore, since both the '912 patent and Amidi show a register that is equivalent to the JEDEC 21-C's register, it would be even less likely that a person of ordinary skill would interpret JEDEC21-C's register as being a logic element.

29. There is no disclosure in the cited references, including Amidi and JEDEC 21-C, that teaches or suggests that bank address signals can be used to generate actual physical address signals from logical address signals. Neither Amidi nor JEDEC 21-C discusses any rationale for modifying Amidi's system by providing the bank address signals to the logic element. JEDEC 21-C does not have any logic that uses the bank address signals except for passing them onto the DDR memory devices via the register. Therefore, a rationale for the proposed modification cannot come from the cited references.

30. Both Amidi and JEDEC 21-C disclose that the register receives the bank address signals so that they can be passed through to the DDR memory devices for their normal function of specifying the bank from which data is to be read or written. In contrast, by providing the bank address signals to the logic element as well, the claimed invention uses the bank address signals for a different function, namely, in determining which rank-selecting signal to generate and transmit to the DDR memory devices. This function was not taught by Amidi or by JEDEC 21-C and would not have been known or foreseen by persons of ordinary skill in the art to be useful.

31. Furthermore, the intended purpose of the JEDEC 21-C reference is to describe a DIMM that conforms to the JEDEC standard specification, and conformance to such industry standards is seen by persons of ordinary skill in the art to be a desirable goal to have success in the marketplace. To the extent that the system disclosed by Amidi is not JEDEC-compliant, a

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DIMM made by the proposed combination of Amidi and JEDEC 21-C would not work for JEDEC 21-C's intended purpose. Therefore, persons of ordinary skill in the art would not have found it obvious to modify Amidi in view of JEDEC 21-C to produce the claimed invention.

4.   Amidi combined with Micron

32. Micron defines the electrical and mechanical features for the 1GB and 2GB (x72, ECC, DR) 184-pin Double Data Rate Synchronous DRAM Registered Dual In-Line Memory Modules (DDR SDRAM RDIMMs). The DIMMs disclosed by Micron are conventional RDIMMs conforming to the relevant JEDEC standards, including "JEDEC Standard JESD82," "JEDEC Standard JESD82-1A," and "the JEDEC MO document" (Micron at Table 12, note 1; Table 14, note 1; Fig. 7, note 2).

33. For reasons similar to those discussed above with regard to Amidi, persons of ordinary skill would not interpret Micron's register as being part of a "logic element." Therefore, Micron does not disclose a logic element that receives a set of input control signals comprising bank address signals. While Micron's register does receive bank address signals, so does Amidi's register, so it is not clear what additional disclosure or suggestion Micron provides with regard to this claim feature that is not already disclosed or suggested by Amidi alone.

34. Furthermore, even if the distinct components of a logic element and a register were contained in a single package as proposed, such packaging does not merge or otherwise affect the distinct functions individually performed by each of the logic element and the register, so persons of ordinary skill in the art would still consider the logic element and the register to be distinct from one another.

35. There is no disclosure in the cited prior art, including Micron or Amidi, that teaches or suggests that bank address signals can be used for the type of translation of input signals as recited in the claims of the '912 patent. Therefore, the rationale for the modification cannot come from the cited prior art.

36. Contrary to the characterization provided by Kozyrakis's '912 Decl. at ¶ 15, the bank address field is <u>not</u> treated in DDR technology in the same way that the row address and column address fields are. For example, bank address signals are also used to supply certain

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initialization values to various control registers within the DDR DRAM devices (e.g., during a load mode register or extended mode registers commands). Because of this additional initialization information that is multiplexed onto the bank address signals during certain DDR commands, a person of ordinary skill in the art contemplating the use of the bank signals as inputs to Amidi's conversion logic would know that failure will occur. Therefore, persons of ordinary skill in the art would not expect that using a bank address bit in Amidi's conversion logic would work.

37. In contrast, even during row/column address translation, the claimed invention utilizes the bank address signals to determine which rank-selecting signals to generate and transmit to the DDR memory devices. This function of the bank address signals was not taught by Micron or by Amidi and would not have been known or foreseen by persons of ordinary skill in the art from either the individual or the combined teachings of Micron and Amidi.

5.   Dell 1 Combined with JEDEC 21-C

38. Neither Dell 1 nor JEDEC 21-C discloses or suggests a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39 of the '912 patent.

39. The only signals disclosed by Dell 1 as being received by its ASIC are RAS, CAS, and one row/column address bit (A11). The EDO memory devices used in Dell 1 do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so as discussed above, there is no need for Dell 1's memory module to receive such bank address signals. Therefore, persons skilled in the art would not be aware of a rationale to transmit bank address signals to the memory module of Dell 1, let alone having Dell 1's ASIC receive such bank address signals.

40. JEDEC 21-C does not provide any additional disclosure or suggestion such that persons of ordinary skill in the art would find it obvious to modify Dell 1 to have its ASIC receive bank address signals. Even though JEDEC 21-C discloses a register that passes through bank address signals to the DDR memory devices, as discussed above, persons of ordinary skill would not interpret JEDEC 21-C's register as being a "logic element," so JEDEC 21-C does not

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include a logic element that receives and translates a set of input control signals comprising bank address signals into a set of output control signals.

41. As discussed above, the claimed invention uses the bank address signals for a different function than does a register, namely, in determining which rank-selecting signal to generate and transmit to the DDR memory devices. This function is irrelevant to the EDO technology of Dell 1 since it does not use chip-select signals and doesn't have internal banks, so neither Dell 1 nor JEDEC 21-C provides a rationale for modifying Dell 1's system by sending bank address signals to the logic element.

6.   Wong Combined with JEDEC 21-C

42. Neither Wong nor JEDEC 21-C disclose or suggest a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39 of the '912 patent.

43. The only signals disclosed by Wong as being received by its bank control circuit are RAS0, CAS0, and one row/column address bit (A13). The EDO memory devices used in Wong do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so as discussed above, there is no need for Wong's memory module to receive such signals. Therefore, persons skilled in the art would not be aware of a rationale to transmit bank address signals to the memory module of Wong.

44. As discussed above, JEDEC 21-C does not provide any additional disclosure or suggestion such that persons of ordinary skill in the art would find it obvious to modify Wong to have its bank control circuit receive bank address signals, so neither Wong nor JEDEC 21-C provides a rationale for modifying Wong's system by sending bank address signals to the logic element.

7.   Micron Combined with Connolly

45. Neither Micron nor Connolly disclose or suggest a memory module having a logic element that receives bank address signals as recited by independent Claims 1, 15, 28, and 39. Micron was discussed above.

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46. Connolly also does not disclose that its ASIC receives bank address signals. The only signals disclosed by Connolly as being received by its ASIC are RAS, CAS, and two row/column address bits. The EDO memory devices used in Connolly do not have internal banks of memory locations that would be accessed using bank address signals (as do DDR memory devices), so there is no need for such signals for Connolly's EDO technology. For EDO technology, the ASIC of Connolly is disclosed as being fully functional without having these bank address signals received by the ASIC. Therefore, persons of ordinary skill in the art would not be aware of a rationale to transmit bank address signals to the memory module of Connolly, let alone having Connolly's ASIC receive such bank address signals.

47. Connolly describes a method and circuit implementation that is applicable to EDO Asynchronous DRAM memory devices. Connolly describes a conversion logic that receives additional bits (row or column address) that would be used to access larger size EDO memory devices, in conjunction with certain control signals, to control smaller size EDO memory devices. Connolly further describes that the portion of the row address or column address fields that are in common between the smaller size and larger size EDO devices are not processed by the logic, but are provided directly to the smaller size EDO memory devices (see Connolly Fig. 3, 4, 5, and 7). Because of the various differences between EDO command protocol and DDR command protocol, a person of ordinary skill in the art would not use the EDO-based technology of Connolly with DDR-based memory devices. Furthermore, the disclosure of Connolly only discusses the use of "extra" row and column address bits. Even though a person of ordinary skill in the art would be aware of DDR memory devices with multiple internal banks, because of the significant differences between how bank addresses and row or column addresses are used in DDR technology, such a person would not expect that a bank address bit could be used in the manner described by Connolly for row and column address bits. Even if such use would be attempted, they would still only be using a single bank address bit, not "bank address signals" as recited in the claims of the '912 patent.

48. In particular, contrary to the characterization provided by Kozyrakis's '912 Decl. at ¶ 15, the bank address field is *not* treated in DDR technology in the same way that the row address and column address fields are. For example, bank address signals are also used to supply certain initialization values to various control registers within the DDR DRAM devices (e.g.,

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during a load mode register or extended mode registers commands). Because of this additional initialization information that is multiplexed onto the bank address signals during certain DDR commands, a person of ordinary skill in the art contemplating the use of the bank signals as inputs to Connolly's conversion logic would know that failure will occur. Therefore, persons of ordinary skill in the art would not expect that using a bank address bit in Connolly's conversion logic would work.

B.   None of the Cited Prior Art Discloses or Suggests a PLL operatively coupled to a Logic Element

49. Each of Claims 1, 15, 28, and 39 recites that "the phase-lock loop device [is] operatively coupled to ... the logic element." As disclosed by the '912 patent, "the phase-lock loop device 50 transmits clock signals to ... the logic element 40" ('912 patent, col. 5, ll. 28-31; see also, Figs. 1A, 1B). It is my opinion that in the context of claim 1 of the '912 patent, a POSITA would understand "operatively coupled" to mean that the output of the recited "PLL device" controls the timing of operations performed by the recited "logic element." This is the interpretation of "operative coupling" between the PLL and logic element supported by the '912 patent specification.

1.   Amidi

50. It is clear from Fig. 6B of Amidi, for example, that its logic element (i.e., "CPLD") is not "operatively coupled" to a PLL, as required by the claims of the '912 patent. Instead, it is readily apparent that Amidi's CPLD is fully functional by being clocked off of the system side input differential clock signals Clk and Clk_n received from the computer system (see Amidi [0039]), and no alternatives are discussed.

51. It would <u>not</u> have been obvious to persons of ordinary skill in the art to modify Amidi's system by operatively coupling the PLL clock signals to the logic element. None of the cited references, including Amidi, discusses any rationale for making this modification. Amidi discloses that its PLL device is used "to generate a zero-delay buffer" off of the input clock signals from the computer system (Amidi, ¶ 39), and as shown in Figs. 6A, 6B, the output clock signals from the PLL device are transmitted to the register and to the memory devices, but not to the CPLD. Instead, Amidi's CPLD receives the input clock signals from the computer system

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(Amidi, Figs. 6A, 6B). Furthermore, a zero-delay buffer is a well-known term in the art that is ordinarily used to relay or buffer the input clock signal using many output clock drivers to transmit a tuned and balanced replica of the input clock signals to the DDR memory devices, by employing a PLL to match the phase of each of the output clock signals to the input clock signals. Various examples of a zero-delay buffer comprising PLL circuitry have been described, manufactured and sold at least by several companies (e.g., Altera, IDT, Cypress, and Pericom) dating back to at least 1998.

52. Additionally, Amidi discloses that its CPLD is fully functional by being clocked by input clock signals received from the computer system, and Amidi does not provide any reason for diverting from such a configuration. Furthermore, the knowledge of persons of ordinary skill in the art would not lead them to divert from Amidi's configuration. In fact, the knowledge of persons of ordinary skill in the art along with the ordinary industry design practices would lead to electrically connecting the CPLD of Amidi to the computer system input clock signals and not to the output of the zero-delay buffer, as discussed in paragraphs 16-18.

53. Furthermore, it is well known that the timing and waveform characteristics of signals propagating between the various components of the memory module are highly dependent on a complex set of variables, some of which are inter-related. These variables include the particular location and layout of the loads, circuit traces, and signal discontinuity points within the memory module. It is critically important that these variables are all properly controlled in order to avoid a catastrophic failure of the memory module. For example, due to transmission line effects, the variations in the signal trace design, the variations of memory device layouts on the board, and the variations in the number of loads per clock line, leads to a large variation in impedances, loading, signal path return currents, and terminations as seen by the output drivers. This results in signal edge aberrations, reflections, amplitude problems, crosstalk, jitter, and ground/supply voltage bounce, all of which can lead to failures of the memory module and thus in turn the failure of the computer system comprising the memory module. These effects are more severe as the speed of operation increases. For this reason, the design of any new memory module entails a large amount of time and effort to tune the various design parameters and variables to ensure sufficient signal timing and waveform characteristics for proper operation.

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54. Due to the large number of variables involved, exacerbated by the various interdependencies and other second order effects, it is not an easy task to design a memory module. Quite a number of fine-tuning iterations are required during the design process, encompassing a fair amount of trial and error, in order to obtain a working memory module design and then to optimize it. Even after the development of the JEDEC specification standards for memory modules, some manufactured and sold memory modules either failed to inter-operate or produced intermittent failures that plagued the personal computer industry. These failures were (i) recognized by industry leaders (e.g., Intel) that allocated resources to resolve these problems, and (ii) launched an effort to form a large consortium of industry leaders and research institutions to collaborate to resolve these system failures. For example, as early as 1998 the PC100 standard was born out of such a consortium and provided reference designs for memory modules complete with (i) bills of materials that specified prequalified parts, (ii) electrical schematics with every electrical connection point on a memory module, (iii) Gerber files that specify the complete layout of interconnecting traces within each Printed Circuit Board (PCB) layer of the memory module, and (iv) the values and placement of resistors and capacitors onto the PCB. To insure interoperability and system level performance, reference designs are continuously provided to DDR memory modules manufacturers. There are only a small number of memory module reference designs (e.g., raw cards) per type of memory module that are specified by JEDEC standards (see, JEDEC 21-C at pp. 10-16, 29-35), since developing a new memory module entails significant time and effort.

55. While expending such time and effort are commonplace in the design of a new memory module, persons of ordinary skill would not seek to do so unless absolutely necessary and they would try to keep such activities to a minimum. In particular, if a person of ordinary skill in the art sought to add a CPLD to a memory module as disclosed by Amidi, they would begin with Amidi's disclosed configuration of timing the CPLD using the computer system input clock signals, and would tune the design parameters to try to achieve proper operation. Persons of ordinary skill in the art would know that operationally coupling the CPLD to the PLL device (i) would change the load on the PLL, degrading its performance, in other words, degrading the relationship between the PLL output clock and the computer system input clock signal, and (ii) would result in the aberration of the waveform characteristics of these PLL output clock signals

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propagating to the DRAM devices, e.g., slew rate, jitter, and skew. These changes in clock

signal timing and waveform characteristics would be seen by a person of ordinary skill to likely

result in high risk of the memory module not working at all, or operating intermittently.

Therefore, such persons would not be tempted to make this change.

56. It is also the case that making such a modification as proposed by the Requests goes

against accepted practices in memory module design. Amidi's configuration in which (i) both

the CPLD and the PLL device are timed to clock signals from the computer system, and (ii) the

register and the DDR memory devices are timed to clock signals from the PLL device is in

accordance with what a person of ordinary skill would immediately recognize as seeking to

maintain the synchronous nature of the DDR memory module. To modify Amidi's configuration

by clocking the CPLD from the PLL device would run against accepted and conventional

industry practices.

57. Another reasons is that the signal propagation delays through the CPLD (see, e.g.,

Fig. 8) would be recognized to be different from the delays through the register in Amidi's

design, if for no other reason than that one is a logic device (the CPLD) and the other is not (the

register). In order to synchronize the arrival of the "Signals to Memory Devices" in Fig. 6A of

Amidi, one of ordinary skill in the art would immediately want to adjust the two clock arrival

times, namely, the arrival at the CPLD and the arrival at the register. Indeed, two separate clocks

are exactly what is depicted in Fig. 6A. Consequently, one of ordinary skill in the art would

routinely believe that Amidi teaches that the CPLD should not receive the output of the PLL.

58. Finally, modifying a JEDEC memory module reference design by clocking the CPLD

directly from the computer system input clock signals and not from the PLL output clock signals

provides the flexibility that persons of ordinary skill in the art would expect in order to design,

adjust, and tweak the memory module comprising the CPLD without having to change the

already well balanced and matched traces of the PLL output clock signals. Otherwise the

inevitable tuning of the PLL device would be significantly more difficult to perform, and would

results in a high risk of memory module or system failures.

59. For at least the foregoing reasons, providing the PLL clock signals to the CPLD

would be seen by persons of ordinary skill in the art as introducing unnecessary complexity that

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can lead to failure. In contrast, providing the computer system input clock signals to the CPLD would be seen by persons of ordinary skill in the art as the obvious choice along with a low risk of failure since no changes to the critical PLL output clock signal paths is incurred

2.   Amidi Combined with Dell 2

60. Dell 2 does not disclose or suggest using a PLL device, so Dell 2 does not cure the deficiency of Amidi.

3.   Amidi Combined with JEDEC 21-C

61. As discussed above, Amidi does not disclose or render obvious a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. While JEDEC 21-C discloses a DIMM having a PLL device operatively coupled to a register (as does Amidi), it does not disclose a logic element, let alone a logic element operatively coupled to the PLL device. Therefore, JEDEC 21-C cannot be relied upon for providing this claim feature missing from Amidi.

62. Furthermore, while JEDEC 21-C discloses that the DDR memory devices and the register each receive clock signals from the PLL device, JEDEC 21-C does not disclose or suggest using PLL clock signals for a logic element of the DIMM. JEDEC 21-C does provide the guidance that "[t]he most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM" (JEDEC 21-C, p. 74). To achieve this goal, accepted practices in DRAM DIMM design would lead persons of ordinary skill in the art to have Amidi's CPLD timed to the system clock signals, not to the PLL clock signals. In contrast, having the logic element operatively coupled to the PLL clock signals would be contrary to accepted practices in DRAM DIMM design.

4.   Amidi Combined with Micron

63. While Micron discloses an RDIMM having a PLL device operatively coupled to a register (as does Amidi), it does not disclose a logic element, let alone a logic element operatively coupled to the PLL device. Therefore, it does not cure the deficiencies Amidi discussed above.

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5.   Dell 1 Combined with JEDEC 21-C

64. Neither Dell 1 nor JEDEC 21-C discloses or suggests a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. JEDEC 21-C is discussed above. Similarly, Dell 1 does not disclose or suggest this claim feature, as acknowledged by the Office Action at p. 29.

65. Additionally, persons of ordinary skill in the art would not consider timing Dell 1's ASIC to the PLL clock signals for the various timing issues and complexities raised by such changes discussed above.

6.   Wong Combined with JEDEC 21-C

66. Neither Wong nor JEDEC 21-C disclose or suggest a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. JEDEC 21-C was discussed above. Similarly, Wong does not disclose or suggest this claim feature, as acknowledged by the Office Action at p. 36.

7.   Micron Combined with Connolly

67. Neither Micron nor Connolly disclose or suggest a memory module having a PLL device operatively coupled to the logic element as recited by independent Claims 1, 15, 28, and 39. Micron was discussed above. Connolly makes no mention of a PLL device.

68. While Micron discloses that the DDR memory devices and the register each receive clock signals from the PLL device, Micron does not disclose or suggest using PLL clock signals for a logic element of the DIMM. Contrary to the assertions made by Requesters, persons of ordinary skill in the art would not have considered timing Connolly's ASIC to the PLL clock signals for the reasons discussed above.

C.   None of the cited prior art discloses or suggests "stor[ing] an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure," as recited in claim 21

69. Claim 21 recites that the circuit "is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access

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procedure." Examples of such an input signal include the row address bit A_{n+1} and the bank address signals.

1.   Amidi

70.   Requesters and the '912 Office Action assert that Amidi discloses this feature. However, Amidi describes a memory module that responds to certain conventional DRAM access commands, including row access and column access commands, in which the address and control signals for column access commands are independently provided by the computer system from those of row access. Amidi's register does temporarily store and retransmit certain signals "to synchronize the incoming address and control signals with respect to differential clock signals" (Amidi, ¶ 38). However, a key difference is that the storage of these certain signals does not take place <u>during</u> a row access procedure with use of these certain signals occurring during a column access procedure. For example, Amidi's memory module receives the full bank address from the computer system during both RAS and CAS time, and Amidi merely provides the full bank address to the memory devices via the register (see, Amidi, ¶¶ 50, 58, Figs. 6A, 6B), without needing any address bits stored from a previous operation, in accordance with the conventional use of such a register. Persons of ordinary skill in the art would not interpret such conventional operations of Amidi's register as somehow storing a signal received during a row access procedure for subsequent use to the DDR memory devices during a column access procedure. Therefore, persons of ordinary skill in the art would not read Amidi as disclosing or rendering obvious such features.

71. The purpose of this feature in Claim 21 is to store an input signal (such as the bank address signals) received during a row access procedure that could be used several commands later, during a column access procedure. That is the key difference with Amidi, where a bank address signals (for example) received during a row access procedure in Amidi, could only be used on the very next command. Meanwhile, the '912 patent supports the use of that bank address signals possibly many commands, to properly respond to column access commands, later.

72. Furthermore, it would not be obvious to persons of ordinary skill in the art to modify Amidi to provide such claim features. Amidi does not provide a rationale for such a feature, and regarding the other cited references, either they do not disclose or suggest such a feature, or

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persons of ordinary skill in the art would not be aware of a rationale to modify Amidi to provide such a feature, for at least the reasons discussed above.

2.   Amidi Combined with Dell 2

73. As discussed above, Amidi does not disclose or suggest this claim feature. Furthermore, persons of ordinary skill in the art would not be aware of a rationale to modify Amidi to include this feature. Dell 2 also does not disclose this claim feature. Instead, Dell 2 merely connects a row/column address bit to an additional bank address pin. In contrast, Amidi's register receives the full bank address from the computer system during both RAS and CAS time, and Amidi provides it to the memory devices via the register (see, Amidi, ¶¶ 50, 58, Figs. 6A, 6B) without needing any bits stored from a previous operation. Therefore, as disclosed by Amidi, there is no reason to store the re-mapped bank address bit during RAS time or to re-send it during CAS time as disclosed by Dell 2. Accordingly, a POSITA would not have been inclined to modify Amidi with the teaching of Dell 2.

3.   Amidi Combined with JEDEC 21-C

74. Both Amidi and JEDEC 21-C disclose memory modules that respond to conventional row access commands and subsequent column access commands in which the address and control signals for column access commands are independently provided by the computer system from those for row access commands. Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure.

4.   Amidi Combined with Micron

75. Both Micron and Amidi disclose memory modules that respond to conventional row access commands and subsequent column access commands in which the address and control signals for column access commands are independently provided by the computer system from those for row access. Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure.

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76. In Amidi, bank address signals are (i) received by the memory module in conjunction with both row access commands and column access commands, and (ii) sent directly to the memory devices via the register. Therefore, not only is there no need to store the bank address signals from the row access procedure for use during the column access procedure, neither Amidi nor Micron individually or in combination teach this functionality.

5. Dell 1 Combined with JEDEC 21-C

77. Dell 1 does not disclose or suggest this claim feature, and as discussed above, neither does JEDEC 21-C. Dell 1 discloses a conversion of a row address bit into a RAS signal, but does not disclose or suggest storing a signal for use during a subsequent column access procedure. JEDEC 21-C discloses a memory module that responds to conventional row access commands and subsequent column access commands, which persons of ordinary skill in the art would not interpret as somehow storing a signal received during a row access procedure for subsequent use or transmission to the DDR memory devices during a column access procedure.

6. Wong Combined with JEDEC 21-C

78. Wong does not disclose or suggest this claim feature, and as discussed above, neither does JEDEC 21-C. Wong discloses a conversion of a row address bit into a RAS signal, but does not disclose or suggest storing a signal for use during a subsequent column access procedure. JEDEC 21-C discloses a memory module that responds to conventional row access commands and subsequent column access commands, which persons of ordinary skill in the art would not interpret as somehow storing a signal received during a row access procedure for subsequent use during a column access procedure.

6. Micron Combined with Connolly

79. Neither Micron nor Connolly discloses or suggests this claim feature. Micron discloses a memory module that responds to conventional row access commands and subsequent column access commands, in which the address and control signals for column access commands are independently provided by the computer system from those for row access commands. Persons of ordinary skill in the art would not interpret such conventional operations as somehow storing a signal received during a row access procedure for subsequent use during a column access procedure.

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80. This claim feature is also not disclosed or suggested by Connolly, or by the combination of Micron and Connolly. The '0579 Request cites Connolly's Fig. 7 as disclosing that the SYS RAS signal is stored during a row access procedure for subsequent use during a column access procedure. The Office Action at p. 47 appears to adopt this rationale by stating that "SYS RAS stored in 90 is used to generate CAS L and CAS R." However, as acknowledged by the '0579 Request at p. G-29, latching of SYS RAS only occurs by "SYS_CAS going active (which will cause SYS_RAS to be latched)." Thus, Connolly's ASIC latches the SYS RAS signal when SYS CAS becomes activated (see, Connolly at col. 11, ll. 5-6). In a read/write operation, upon SYS CAS going active, the row access procedure is ended, and the subsequent column access procedure has begun. Therefore, Connolly's ASIC does not store the SYS RAS during the row access procedure, so Connolly's treatment of the SYS RAS signal does not satisfy the claim feature of storing the input signal during a row access procedure for subsequent use during a column access procedure.

81. The '0579 Request also cites Connolly at col. 5, ll. 50-52 and Fig. 4 as disclosing that the address bit A11 is latched during a row access procedure so that "the address bit is A11 is freed and not required to stay in its state during the entire operation." However, while Connolly discloses latching and using the value of A11 to determine whether to make RAS A or RAS B active during a row access procedure, Connolly does not disclose or suggest that this latched address bit is used during a subsequent column access procedure. Therefore, Connolly's treatment of the address bit A11 also does not satisfy the claim feature of storing the input signal during a row access procedure for subsequent use during a column access procedure.

D.   None of the Cited Prior Art Disclose or Suggest a SPD device data characterizing the memory module as having different attributes

82. Each of new Claims 56, 60-63, 75, 80, 81, 85, 86, 90, 91, and 109-111 addresses the memory module storing data characterizing the plurality of DDR memory devices as having attributes that they do not actually have. None of the cited prior art discloses or suggests this feature. While Amidi discloses a memory module having an SPD device that is a "simple I2C interface EEPROM to hold information regarding memory module for BIOS during the power-up sequence" (see, e.g., Amidi, ¶ 40), nowhere does Amidi disclose or render obvious that the

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data stored by the SPD device characterizes the plurality of DDR memory devices as having attributes different from their actual attributes.

83. Wong does not disclose an SPD device, so it does not disclose or suggest this claim feature. Furthermore, as discussed above, JEDEC 21-C also does not disclose or suggest this feature, so these claims would not be obvious to persons of ordinary skill in the art.

84. Connolly does not disclose an SPD device, so it does not disclose or suggest this claim feature. While Micron discloses a serial presence detect (SPD) device, it does not disclose or suggest that the data stored by the SPD device is anything except a characterization of the actual attributes of the plurality of DDR memory devices of the DIMM. In fact, to have the data characterize the plurality of DDR memory devices as having any attributes different from its actual attributes would likely cause fatal errors when the computer's memory controller attempts to access the memory module, making the memory module disclosed by Micron inoperative for its intended purpose.

E.   None of the Cited Prior Art Enable Successive or Back-to-Back Adjacent Read Commands from Different DDR Devices

85. New Claims 64, 69, 102, and 103 are directed to memory modules capable of performing "successive read accesses from different ranks of DDR memory devices" and each of new Claims 65, 70, 78, 83, 88, 104, and 105 are directed to memory modules capable of performing "back-to-back adjacent read commands which cross DDR memory device boundaries."

86. Some of the issues with respect to performing successive read accesses will now be presented by means of an example. In the context of performing a read operation (which uses both an activate command and a subsequent read command) the '912 patent uses an extra row address bit for performing a read operation, and the same principles apply for a write operation.

87. In the DDR memory module of the '912 patent, the logic element 40 receives the bank address signals (e.g., BA_0-BA_m) from the computer system (see '912 patent, Figure 1A and col. 7, ll. 35-53) both during activate commands and during read/write commands. (Note that

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Amidi does <u>not</u> disclose that the CPLD ever receives the bank address bits BA[1:0].) For example, the '912 patent discloses that during the activate command, the logic element 40 receives the row address bit (A_{n+1}), the chip-select signals (CS_0, CS_1), and bank address signals (e.g., BA_0-BA_m) (*Id.*) For the activate command, the logic element 40 then generates the appropriate chip-select signals in response to the input chip-select signals (CS_0, CS_1), the row address bit (A_{n+1}), and the activate command (e.g., using the logic table of Table 1 of the '912 patent). The '912 patent also discloses that the logic element keeps track of the value of the row address bit received during the activate command for the selected bank identified by the received bank address signal (see, the '912 patent at col. 9, ll. 18-21, and the Verilog code at cols. 17-19). (Note again that Amidi's CPLD does not receive the bank address signals, so it is unable to keep track of this information.)

88. During the subsequent read command, the logic element 40 receives the bank address signals identifying the bank to be accessed and the chip-select signals from the computer system. The logic element uses the previous row address bit corresponding to the previous activate command that activated the bank identified to be accessed (see, the Verilog code of the '912 patent at cols. 17-19). In this way, the logic element of the '912 patent is able to generate the appropriate chip-select signals for the read command to correspond to the previously activated bank using the bank address signals from both the activate command and from the read access command. In particular, by utilizing the bank address signals in this way, the logic element disclosed by the '912 patent can handle command sequences that include successive or back-to-back adjacent read commands seeking to access data in two different physical ranks.

89. None of the cited references that I have reviewed disclose or suggest this solution to a person of ordinary skill in the art, and I am not aware of any prior work that discloses or suggests such a solution.

90. Amidi does not disclose or render obvious a memory module that is capable of performing such operations. In fact, as discussed in detail below, the disclosure of Amidi does not address the issue of adjacent read commands at all and it does not disclose a system that can correctly handle or respond to such command sequences.

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91. With regard to row address decoding, Amidi discloses that its CPLD receives some of the input control signals from the computer system, namely, chip-select signals (cs0, cs1), address bit Add(n), and command signal bits (CAS, RAS, WE). Amidi further discloses that its register receives some of the input control signals, namely, address bits Add[n-1:0], command signal bits (RAS, CAS, WE), and bank address bits BA[1:0] (Amidi at ¶ 50, Figs. 6A, 6B). Note that Amidi does not disclose that the CPLD 604 receives the bank address bits BA[1:0].

92. As a result, the memory module disclosed by Amidi and shown by Figure 6A will not be able to correctly control or activate the various ranks of DDR memory devices under circumstances that must be handled by an operational DDR memory module. Because the CPLD does not receive the bank address bits BA[1:0], the CPLD will not have enough information to know what chip-select signals to generate for successive or adjacent read accesses and/or write accesses. For example, to perform a read operation from the DDR memory devices of a memory module, an activate command signal is first issued to activate the bank and row identified by the bank address signals and the row address signals, respectively, along with the appropriate chip-select signal to enable the rank containing the bank and row to be activated. During a row address command as disclosed by Amidi at Fig. 6A and ¶¶ 49-52, to issue the activate command signal, the CPLD receives the row address bit Add(n) (e.g., A12) and the chip-select signals (cs0, cs1), and outputs the corresponding chip-select signals (rcs0, rcs1, rcs2, rcs3) according to the truth table of Fig. 5. The chip-select signals from the CPLD are sent to the DDR memory devices so that only the identified bank and row for the selected rank are activated.

93. To complete the read operation, a read command signal must also be issued separately to the DDR memory devices sometime after the activate command signal. For this read command signal, the column address signal is provided by the computer system to identify the column of the activated bank and row from which the data is to be read. However, the correct rank has to be enabled by the read command signal as well, since for DDR memory, the activate command signal does not have to immediately precede the subsequent corresponding read command signal. In addition, there can be multiple ranks enabled at any given time, each enabled by an activate command which activates one bank and one row for one enabled rank. As a result, there can be intervening activate command signals and/or other command signals

corresponding to other banks and rows of the DDR memory devices between a particular activate command signal and its corresponding read command signal.

94. There will be situations when multiple ranks are active concurrently and then two or more of the read access commands that complete the read operation from these active ranks will follow one another (e.g., successive read accesses from different physical ranks of DDR memory devices, also called back-to-back adjacent read commands which cross DDR memory device boundaries). An operational memory module comprising DDR memory devices is required to be able to handle such circumstances.

95. Each of these read command signals in DDR technology needs to identify which rank is to be read by including the appropriate chip-select signal in the read command signal. In conventional memory modules, it is a simple matter to do so since the appropriate chip-select signal is provided by the computer system. In this way, regardless of any intervening command signals, the read command signal is able to read data from the appropriate column of the previously activated bank and row.

96. However, in Amidi's memory module, the appropriate chip-select signals are to be generated by the CPLD. But the read command signal coming from the computer system does not include the row address bit needed for the CPLD to determine the correct rank to be enabled, since this row address bit is only available during the row access command and not during the column access command. In particular, while the needed address bit Add(n) is provided by the computer system with the row access command, it is not provided by the computer system with the column access command. The CPLD disclosed by Amidi cannot generate the chip-select signals for the read command signal to appropriately correspond to the previously activated bank and row. Therefore, the system disclosed by Amidi would not work for its intended purpose of providing an operable and reliable DDR memory module. In particular, the system disclosed by Amidi will not properly perform "successive read accesses from different ranks of DDR memory devices" or "back-to-back adjacent read commands which cross DDR memory device boundaries."

97. In contrast, these command sequences are described in the '912 patent, along with a DDR memory module that is able to correctly handle such command sequences. In the DDR

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memory module of the '912 patent, the logic element 40 receives the bank address signals (e.g.,
BA_0-BA_m) from the computer system (see, Figure 1A and col. 7, ll. 35-53), particularly both
during row access commands and during column access commands. As a result, the logic
element 40 has all the necessary information to generate the appropriate chip-select signals
(CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) for use with both the activate command signal and the read/write
command signal. For example, for row access commands, the '912 patent discloses that the
logic element 40 receives the row address bit (A_{n+1}), the chip-select signals (CS_0, CS_1), and bank
address signals (e.g., BA_0-BA_m) (see, the '912 patent at Figure 1A and col. 7, ll. 35-53). Thus,
the logic element 40 generates the appropriate chip-select signals in response to the input chip-
select signals (CS_0, CS_1), the row address bit (A_{n+1}), and the command signal (e.g., using the
logic table of Table 1 of the '912 patent). The logic element 40 latches the row address bit (A_{n+1})
during the activate command for the selected bank (see, the '912 patent at col. 9, ll. 18-21), for
subsequent use during a column access command. Thus, by using the "one-to-one-to-one"
correspondence between an activated bank, an activated row, and the enabled logical rank, the
logic element of the '912 patent is able to generate the appropriate chip-select signal for the read
command signal to correspond to the previously-activated bank and row using the bank address
signals from both the activate command and from the read access command. Thus, the memory
module disclosed and claimed by the '912 patent will not suffer from the missing information
problem of Amidi's memory module.

98. None of the cited references, including Amidi, discloses, suggests or attempts to solve
the underlying problem with Amidi's disclosed system. Furthermore, identification of the
problem, as well as identifying and implementing its solution, would be outside the knowledge,
experience, and capabilities of persons of ordinary skill in the art. Nowhere does the prior art
point to such a solution, and such a solution would be outside the knowledge and abilities of
persons of ordinary skill in the art. Therefore, Amidi's disclosure is not enabling for the subject
matter of the claims of the '912 patent, and the solution to this lack of enablement and its
implementation would not be obvious to persons of ordinary skill in the art. In particular, Amidi
does not disclose or render obvious a DDR memory module as recited in Claims 69, 70, 78, 83,
88, and 94-101.

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99. As discussed above, Amidi does not disclose or render obvious a memory module that is capable of performing successive or back-to-back adjacent read commands from ranks of different DDR devices. The DDR memory module of JEDEC is only capable of performing successive or back-to-back adjacent read commands from the same rank. However, it is far more difficult to implement such successive or back-to-back adjacent read commands across DDR device boundaries, and there has been no enabling guidance in the prior art and certainly not in the combined teachings of Amidi and JEDEC .

100.   Similarly, the DDR memory module of Micron is only capable of performing successive or back-to-back adjacent read commands from the same rank. However, it is far more difficult to implement such successive or back-to-back adjacent read commands across DDR device boundaries, and there has been no enabling guidance in the prior art and certainly not in the combined teachings of Micron and Amidi.

101.   Dell 1 does not disclose or render obvious a memory module that is capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands. The DDR memory module of JEDEC is only capable of performing successive or back-to-back adjacent read commands from the same rank. However, it is far more difficult to implement such successive or back-to-back adjacent read commands across DDR device boundaries, and there has been no enabling guidance in the prior art and certainly not in the combined teachings of Dell 1 and JEDEC 21-C.

102.   Wong does not disclose or render obvious a memory module that is capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands. The DDR memory module of JEDEC is only capable of performing successive or back-to-back adjacent read commands from the same rank. However, it is far more difficult to implement such successive or

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back-to-back adjacent read commands across DDR device boundaries, and there has been no enabling guidance in the prior art and certainly not in the combined teachings of Wong and JEDEC 21-C.

103.   Similarly, Connolly does not disclose or render obvious a memory module that is capable of performing such operations since reading or writing data in EDO memory technology requires a RAS command to be immediately prior to the corresponding CAS command, without intervening RAS or CAS commands, so it is not capable of executing back-to-back adjacent read commands across DDR memory device boundaries or successive read accesses from different ranks of DDR memory devices. The DDR memory module of Micron is only capable of performing successive or back-to-back adjacent read commands from the same rank. However, it is far more difficult to implement such successive or back-to-back adjacent read commands across DDR device boundaries, and there has been no enabling guidance in the prior art and certainly not in the combined teachings of Micron and Connolly. Therefore, claims reciting this feature are not rendered obvious by Micron in view of Connolly.

G.   A POSITA Would Not Have Combined DDR Teachings with EDO Teachings

104.   The DRAM devices of Dell 1 are not DDR memory devices, but extended data-out (EDO) memory devices. EDO memory technology is significantly different from the later-developed DDR memory technology that is recited in the claims of the'912 patent, as discussed more fully below. As acknowledged by the Office Action at p. 29, Dell 1 does not disclose a memory module using DDR memory devices. Due to the significant differences between DDR memory technology and Dell 1's EDO technology, persons of ordinary skill in the art would not find it obvious to make the modification proposed by the Office Action which results in the replacement of the EDO memory devices of Dell 1 with the DDR memory devices of JEDEC 21-C, as proposed by the Office Action (e.g., for Claims 1, 15, 28, and 39, and various dependent claims).

105.   While DDR memory is an advance in memory technology with capabilities beyond those of previously developed EDO memory technology, the significant differences between the two different protocols make substitution of DDR memory into Dell 1 impractical. These differences include but are not limited to: (i) memory organization (e.g., DDR memory

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devices have multiple selectable internal banks which are missing from EDO memory devices);
(ii) different address and control signals (e.g., DDR technology uses bank address signals and
chip-select signals that are not found in EDO technology); (iii) command signals/structure (e.g.,
DDR command protocol allows multiple chip-select signals to be asserted simultaneously, while
EDO command protocol allows only one RAS to be asserted at a time); and (iv) EDO uses
asynchronous operation, while DDR uses synchronous operation. Modifying a device designed
for one of these two protocols (e.g., Dell 1's EDO-compatible memory module) to incorporate
features of the other of these two protocols (e.g., JEDEC 21-C's DDR devices) would result in a
hybrid protocol, different from either EDO or DDR, that would require its own lengthy and
costly system development. Thus, these differences represent a huge technological hurdle that
would prevent persons of ordinary skill in the art from considering substituting JEDEC 21-C's
DDR memory devices for Dell 1's EDO memory devices.

106.   For example, properly accessing the multiple internal banks within DDR memory
devices, not found in EDO memory devices, introduces significant complications that would
require undue experimentation by persons of ordinary skill in the art if attempted without the
disclosure of the '912 patent. As another example, the differences between Dell 1's RAS signals
in EDO technology and the chip-select signals in DDR technology are such that persons of
ordinary skill in the art would not interpret Dell 1's RAS signals as chip-select signals.

107.   In addition, as discussed more fully below, EDO memory technology constrains
command sequences for reading or writing data such that the row activation (RAS) command is
immediately prior to the column access (CAS) command, without intervening RAS or CAS
commands. Therefore, EDO technology is not capable of providing the benefits of executing
back-to-back adjacent read commands across memory device boundaries or successive read
accesses from different ranks of memory devices, as can DDR memory technology.

108.   Requesters do not acknowledge these differences between DDR and EDO
memory technologies, either by not addressing the differences, or, in multiple places, by
incorrectly stating that Dell 1 explicitly references DDR technology or discloses the use of DDR
technology. The '0578 Request at p. 198 also states that "[t]he difference between the claimed
invention and [Dell 1] is that [Dell 1] does not explicitly disclose the use of certain signals."

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This statement trivializes the significant differences between DDR and EDO memory technologies in a manner in which persons of ordinary skill in the art would not agree. Therefore, persons of ordinary skill in the art would not find it obvious to replace the EDO memory of Dell 1 with the DDR memory of JEDEC 21-C as proposed by the Office Action.

       109.   In proposing a motivation for the combination, the Office Action at p. 29 states that "[i]t would have been obvious to one of ordinary skill in the art … to design the DIMM of Dell 1 in compliance with the JEDEC standard to make it compatible with computer systems that expect DIMMs installed in the system to be standard compliant." However, persons of ordinary skill in the art would not seek to design a DIMM using EDO technology to conform to a DDR standard, such as JEDEC 21-C. EDO technology has its own set of industry standards, and if persons of ordinary skill in the art wished to make the Dell 1 memory module "standard compliant" as suggested by the Office Action, they would look to the EDO standards, not DDR standards.

       110.   Similarly, the DRAM devices of Wong are not DDR memory devices, but EDO memory devices. As discussed above, EDO memory technology is significantly different from the later-developed DDR memory technology that is recited in the claims of the '912 patent. For the reasons discussed above, a POSITA would not have combined the DDR teachings of JEDEC 21-C with the EDO teachings of Wong.

       111.   Connolly includes substantially all of the disclosure of Dell 1, which as discussed above, discloses an EDO memory module. For the reasons discussed above, actual application of Connolly's EDO techniques to modify the DDR technology disclosure of Micron would have been beyond the skill of one of ordinary skill in the art and, thus, would not have been obvious to persons of ordinary skill in the art.

[Signature Page to Follow]

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112. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: July 5, 2011

Carl Sechen, Ph.D.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

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EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
10/04/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

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Date:

MAILED

OCT 04 2011

CENTRAL REEXAMINATION UNIT

Transmittal of Communication to Third Party Requester
Inter Partes Reexamination

REEXAMINATION CONTROL NO. : 95000578 + 95000579 + 95001839
PATENT NO. : 7619912
TECHNOLOGY CENTER : 3999
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified Reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the inter partes reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an ex parte reexamination has been merged with the inter partes reexamination, no responsive submission by any ex parte third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the Central Reexamination Unit at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

PTOL-2070(Rev.07-04)

OFFICE ACTION IN INTER PARTES *REEXAMINATION*	Control No. + 1339 95/000,578 + 579	Patent Under Reexamination 7619912
	Examiner WOO H. CHOI	Art Unit 3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on 7/5/2011
Third Party(ies) on 8/29/2011

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:
    2 MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.
For Third Party Requester's Comments on the Patent Owner Response:
    30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892
2. ☒ Information Disclosure Citation, PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims 1-118 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☒ Claims See Continuation Sheet are confirmed. [Unamended patent claims]
4. ☐ Claims _____ are patentable. [Amended or new claims]
5. ☒ Claims See Continuation Sheet are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____ ☐ are acceptable ☐ are not acceptable.
8. ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has:
    ☐ been received. ☐ not been received. ☐ been filed in Application/Control No 95000578.
10. ☐ Other _____

Continuation Sheet (PTOL-2064)   **Control No. 95/000,578**

Continuation of SUMMARY OF ACTION:3. Claims confirmed.[Unamended patent claims]are 9, 21, 53-56, 58-60, 66, 72-74, 92, 93, 95, 97, 99 and 101.

Continuation of SUMMARY OF ACTION: 5. Claims rejected are 1-8,10-20,22-52,57,61-65,67-71,75-91,94,96,98,100 and 102-118.

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Art Unit: 3992

INTER PARTES REEXAMINATION OFFICE ACTION

1.   This is an *inter partes* reexamination of U.S. Patent No. 7,619,912 ('912 patent). On

February 28, 2011 three *inter partes* proceedings, 95/000,578, 95/000,579, and 95/001,339

initiated based upon three different requests by Requester 2, Requester 3, and Requester 1,

respectively, have been merged. Clams 1-51 were subject to reexamination. In response to the

Office Action mailed April 4, 2011, Patent Owner added claims 52-118 without amending any of

the original claims. Claims 1-118 are currently pending in this proceeding. The references

discussed herein are as follows:

- U.S. Patent No. 5,926,827 ("Dell 1");

- U.S. Patent No. 6,209,074 ("Dell 2");

- *Quad Band Memory (QBM^{TM}): DDR 200/266/333 devices producing DDR400/533/667*, QBM Alliance, Platform Conference, San Jose, California, January 23-24, 2002 ("QBMA");

- U.S. Patent No. 5,745,914 ("Connolly");

- U.S. Patent No. 6,414,868 ("Wong");

- U.S. Patent Application Publication No. 2006.0117152 ("Amidi");

- *Design Specification for PC2100 and PC1600 DDR SDRAM Registered DIMM*, JEDEC Standard No. 21-C, Revision 1.3, Release 11b, January 2002, ("JEDEC 21C");

- *Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications*, JEDEC Standard No. 82-4B, May 2003, ("JEDEC 82-4B");

- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79C, March 2003, ("JEDEC 79C");

- Micron, *DDR SDRAM RDIMM*, MT36VDDF12872 & MT36VDDF28672 Data Sheet © 2002, ("Micron");

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Art Unit: 3992

- Murdocca, Miles, J., *Principles of Computer Architecture*, Prentice Hall, Inc., 2000 ("Murdocca").

- Vogt, Pete, "*Fully Buffered DIMM Server Memory Architecture: Capacity, Performance, Reliability, and Longevity,*" February 18, 2004 ("Vogt").

Statutory Bases for Rejections - 35 USC §§ 102 and 103

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Summary of Rejections

4.   The following list is the summary of rejections in this Office action.

Ground 1: Obviousness over QBMA and JEDEC 21C (Proposed by Requester 1)

Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

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Ground 2: Obviousness over QBMA and Dell 2 (Proposed by Requester 1)

Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 3: Anticipation by Amidi (Proposed by Requesters 1 and 2)

Rejection of claims 1-7, 9-11, 14-15, 18-21, 23-25, 28-34, 36-37, 40-43, 46, and

51, proposed by Requester 1, is **not adopted**.

Rejection of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, and 41-

45, and 50, proposed by Requester 2, is **not adopted**.

Ground 4: Obviousness over Amidi (Proposed by Requester 1)

Proposed rejection of claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, and 51 is **not

adopted**.

Proposed rejection of new claims 52-55, 57-59, 64-89, 92-108, and 112-118 is **not

adopted**.

Ground 5: Obviousness over Amidi and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-51 is **not adopted**.

Ground 6: Obviousness over Amidi and JEDEC (Proposed by Requesters 1 and 2)

Rejection of claims 1, 3-4, 6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34,

36-39, 41-43, 45, and 50, proposed by Requester 2 is **adopted**.

Rejection of claims 7, 9, 21, 33, and 44, proposed by Requester 2, is **not adopted**.

Rejection of new claims 61-63, 90-91, and 109-111, proposed by Requester 1 is

adopted.

Rejection of new claims 56 and 60, proposed by Requester 1, is **not adopted**.

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Rejection of new claims 52, 57, 61-71, 75, 77-91, 94, 96, 98, 100, and 102-118,

proposed by Requester 2, is **adopted**.

Rejection of new claims 53-56, 58-60, 66, 72-74, 92-93, 95, 97, 99, and 101,

proposed by Requester 2, is **not adopted**.

Ground 7: Obviousness over Murdocca and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42 is **not**

adopted.

Ground 8: Anticipation by Dell 1 (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39,

41-45, and 50 is **not adopted**.

Ground 9: Obviousness over Dell 1 and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-

39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 10: Anticipation by Wong (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39,

41-45, and 50 is **not adopted**.

Ground 11: Obviousness over Wong and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-

39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 12: Obviousness over Micron and Connelly (Proposed by Requester 3)

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Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-22, 24-25, 27-29, 31-33,

36-39, 41-45, and 50 is **adopted**.

Proposed rejection of claims 9 and 21 is **not adopted**.

Ground 13: Obviousness over Micron and Amidi (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-

34, 36-39, 41-45, and 50 is **adopted**.

Proposed rejection of claims 9 and 21 is **not adopted**.

Ground 14: Lack of written description support (Proposed by Requester 1)

Proposed rejection of claims 57-60, 68, 76, 79, 84, and 89-91 is **not adopted**.

Ground 15: Indefiniteness (Proposed by Requester 1)

Proposed rejection of claim 76 is **not adopted**.

Ground 16: Obviousness over Amidi, JEDEC, and Vogt (Proposed by Requester 2)

Proposed rejection of claim 76 is **adopted**.

Discussion of Rejections

Ground 1

5.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and

JEDEC 21C. The proposed rejection is **not adopted**.

6.   With respect to claims 1, 15, and 28, Requester alleges that QBMA discloses "a circuit

mounted to the printed board, the circuit comprising a logic element and a register" as claimed.

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Requester identified the QBM switch disclosed in QBMA on page 17 as the circuit or the logic

element (see Request 1 pp. 42-43). The QBM switch shown on page 17 is reproduced below.

As shown in the figure above, the QBM switch takes 8-bits (C[0,7]) + two strobe signals (DQS

C), and three control signals (Enable, SB, BE CLK) on the DIMM side of the interface as inputs.

In contrast, the claim requires "the logic element [to] receiv[e] a set of input control signals from

the computer system, the set of input control signal comprising at least one row/column address

signal, bank address signals, and at least one chip-select signal." Thus, the claim requires the

logic element to receive a set of at least four signals: one row/column address signal, two bank

signals, and one chip-select signal. It is clear from the figure that none of the signals received by

the QBM switch corresponds to any of the set of input signals required by the claim.

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7.   Requester 1 alleges that QBMA discloses RAS and CAS signals. However, these signals

are not address signals or a chip-select signal. Although Requester 1 also asserts, citing pages

17-20 and 23, that QBMA discloses a bank select signal which is supplied to the QBM switch,

Requester 1 has failed to identify the bank select signals allegedly taught by QBMA from any of

the figures on any of the cited pages. Requester 1 further alleges that the QBM controller shown

on page 24 provides address and control signals to the memory DIMM. While Requester 1 is

correct that address and control lines are shown on page 24, Requester 1 has failed to show how

page 24 of QBMA teaches the "logic element" limitation above.

8.   Requester 1 also alleges "that providing such input control signals to a logic element was

well known at the time of the invention" (see Request 1, p. 43). There is no evidence on the

record that it was well known to provide the recited set of input signals to a QBM switch at the

time of the invention.   Based on the above allegation without evidence, Requester 1 concludes

that "it would have been obvious to one of ordinary skill in the art to provide such input control

signals to the logic element particularly given that such was standard in the industry at the time

of the invention." Again, Requester 1 has provided no evidence that providing a row/column

address signal, bank address signals, and a chip-select signal to the QBM switch was standard in

the industry.

9.   With respect to claim 39, the claim recites an integrated circuit that comprises a logic

element, wherein the logic element receives bank address signals and at least one command

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signal. As with the other independent claims, Requester 1 identified the QBM switch as the

logic element. However, as shown above, the QBM switch does not receive bank address signals

or a command signal as input.

10.   Requester 1 also alleges that the limitation "the at least one integrated circuit element

generating a plurality of output signals in response to the plurality of input signals, the plurality

of output signals comprising row address signals, column address signals, bank address signals,

command signals, and the first number of chip-select signals" is taught by the QBM switch

which "contains circuitry that takes address bits [0,7] from "C:DIMM connector side" and maps

to "A or B: memory chip side" address A[0,7] or B[0,7]" (see Request, p. 64). This allegation is

based on Requester's interpretation of C[0,7] signals, shown on page 17 of QBMA, as address

signals. While QBMA does not explicitly state whether C[0,7] is a set of address signals or data

signals, the Figure above shows that the set of 8-bit signals (C[0,7] is the only set of 8-bit signals

shown in the Figure) is associated with the two data strobe signals for circuitries A and B (DQS

C_A and DQS C_B). Thus, it is more likely than not that C[0,7] is a set of signal that represents 8

data bits, rather than address bits as asserted by Requester 1.

Ground 2

11.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and Dell

2. The proposed rejection is **not adopted**.

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12.   The Examiner initially notes that Requester 1's proposed rejection maps alleged

teachings of the two references applied (QBMA and Dell 2) to limitations of individual claims in

a claim chart without clearly ascertaining the differences between the prior art and the claims at

issue (step 2 of the *Graham* v. *John Deere Co.* obviousness analysis framework). The proposed

rejection does not make it clear as to which features from which references are to be applied in a

combination to make a system that teaches all of the limitations of the claims. For example, the

claim chart for claim 1, at pages 71-74 of the Request, maps every element of claim 1 to some

teaching in Dell 2 appearing to allege that claim 1 is anticipated by Dell 2. Yet, the proposed

rejection uses QBMA as the primary reference and Dell 2 as a secondary reference.

13.   With respect to claims 1, 15, and 28, Requester 1 alleges that the limitation "the logic

element receiving a set of input control signals from the computer system, the set of input control

signals comprising at least one row/column address signal, bank address signal, and at least one

chip-select signal" is taught by the combination of the QBM switch and Dell 2's logic circuit that

receives "a number of address inputs an a number of bank address signals from a memory

controller with said address input and bank address input signals corresponding to N bank

memory devices" and that it would have been obvious to combine the teachings. As discussed

above, the QBM switch does not receive any of the recited input signals. Dell 2 does not cure

this deficiency because while the passage cited in Request 1 discloses a logic circuit receiving a

number of address input and a number of bank address signals, Dell 2 does not teach that the

logic circuit receives a chip-select signal.

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14.   Requester 1 alleges that it would have been obvious to combine the teachings of QBMA

and Dell 2 to produce a logic element which receives input control signals including at least one

row/column address signal, bank address signals, and a chip-select signal to facilitate memory

domain translation. However, Requester 1 has not explained how adding address signals and a

chip-select signal as inputs to the QBM switch facilitates memory domain translation. QBMA

does not disclose the use of the QBM switch for memory domain translation. Memory modules

disclosed in QBMA do not appear to handle row/column address and bank signals through the

QBM switch. Thus, it makes little sense to redesign the modules by rerouting the address/bank

signals through the QBM switch to use the QBM switch for memory domain translation

application when Dell's invention can be use for that purpose without any redesign.

15.   Requester 1 also alleges that the limitation "the circuit generating a set of output control

signals in response to the set of input control signals corresponding to the first number of DDR

memory device arrange in the first number of ranks" is taught by both QBMA and Dell 2,

without making it clear whether the combined system uses QBMA's teaching or Dell's teaching.

As discussed above, the QBM switch does not generate addresses. As to Dell 2's disclosure, the

passage cited by Requester 1 that allegedly teaches this limitation (c8:20-27) is a textual

description of Figure 1A. Figure 1A shows remapping of address signal A12 as BA1. The rest

of the address signals and the bank signal BA0 are used as they are. Therefore, Dell 2's circuit

does not "generate a set of output control signals in response to the set of input control signals."

To the extent that remapping of A12 as BA1 can be considered "generating an output signal,"

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Dell 2 teaches generating an output control signal BA1, not "output control signals" as required

by the claims.

16.   Claims also require the circuit to "generat[e] and transmit[] a second command signal and

the set of output control signals to the plurality of memory devices" in response to a first

command signal and the set of input control signal. Again, Requester 1 does not make it clear

whether the combined circuit is to use QBMA's teaching or Dell's teaching with respect to this

limitation. Requester asserts that QBMA's disclosure that a QBM uses standard DDR

commands teaches this limitation. However, the claim specifically requires the circuit to

respond to a first command by generating a second command. QBMA does not specifically

disclose that a QBM generates and transmits commands in response to standard DDR commands

or that it generates standard DDR commands in response to commands received by the circuit.

Likewise, the passage in Dell 2 cited by Requester 1 does not disclose a circuit that generates and

transmits a command in response to another command as required by the claims.

17.   Claim 39 recites limitations that are similar to those of claim 1 discussed above. See the

discussion of claim 1 above.

Ground 3

18.   Requester 1 asserts that claims 1-7, 9-11, 14-15, 18-21, 23-25, 28-34, 36-37, 40-43, 46,

and 51 are anticipated by Amidi. Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25,

27-29, 31-34, 36-39, and 41-45, and 50 are anticipated by Amidi. These rejections are **not**

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adopted. All claims require a circuit that comprises a logic element and a register. Amidi does

not disclose a circuit that comprises a logic element with all of its limitations **and** a register.

Prior rejections relied on the same register (408, 418, or 608, all depicting the same register) to

teach the limitations of the logic element limitation and the register. After consideration of all of

the arguments presented, the Examiner concludes that reasonable interpretation of the claim

language, in view of the specification, requires a logic element that is separate and distinct from

a register. Thus, Amidi teaches a logic element with all of its required limitations without a

register, or a logic element without all of the required limitations and a register, but not both as

required. See discussion below (Response to Arguments).

19.   Rejection of claims 21, proposed by Requesters 1 and 2, is **not adopted**. Requester 1

alleges that paragraphs 37, 38, and 57 of Amidi disclose the claim limitation. These paragraphs

and Figures 4 and 6 appear disclose a register that stores input signals and transmit output signals

during both column and row access procedures. However, there is no specific disclosure that an

input signal stored during a row access procedure is stored for subsequent use during a column

access procedure. Requester 2 explains that Amidi teaches that since standard DDR memory

modules have only one set of address lines, two sets of addresses must be provided to access

certain types of cells and that Amidi's memory module stores the input signals to provide

column address signals on a separate cycle from the row address signals citing paragraph 61.

However, Requester 2 fails to explain how paragraph 61 teaches the actual limitation "wherein

the configured to store an input signal of the set of input signal during a row access procedure for

subsequent use during a column access procedure." The cited paragraph does not disclose that

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an input address signal stored during a row access procedure is retained for subsequent use

during a column access procedure from the cited pages.

Ground 4

20.   Requester 1 asserts that claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, 51, and new claims

52-55, 57-59, 64-89, 92-108, and 112-118 are obvious over Amidi. Proposed rejection is **not**

adopted. See Ground 3 above.

21.   Requester 1 asserts that because the address signals supplied to the memory module via

the address bus includes Address[n:0] and BA[1:0], Amidi impliedly discloses that the set of

input control signals comprises "at least one row/column address signal, bank address signals,

and at least one chip-select signal" (Request 1, p. 128). Although the Examiner agrees that the

set of input control signals to the memory module comprises the recited signals, the claims

specifically require the "logic element" to receive those signals. Figure 6 clearly shows that only

the register 608 receives the bank address signals.

22.   Requester 1 further asserts that "[t]o the extent that [Amidi] does not explicitly disclose

that the set of input control signals comprises "at least one row/column address signal, bank

address signals, and at least one chip-select signal," it would have been obvious to one or

ordinary skill in the art at the time of the invention to provide such control signals to the logic

element to improve the active bank/rank determination" (Request 1, p. 128). This is merely an

allegation without any reasoned analysis as to how and why providing "such control signals" to

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CPLD would be obvious and improve the active bank/rank determination. These control signals
are received and handled by another element (register) in the module. Requester 1 does not
explain why one skilled in the art would move or duplicate the control signals so as to be
received by CPLD and how this improves the memory module. Conclusion of obviousness
requires an articulation of some reason with some rational underpinning to support the
conclusion.

23.   With respect to claims 16 and 17, Requester 1 asserts that "[o]ne of ordinary skill in the
art would have understood from the '152 publication that the command signal may be
transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned
explanation to support the assertion. Conclusion of obviousness requires more than a mere
conclusory statement.

24.   With respect to claim 21, the proposed rejection does not address the actual limitation of
the claim that requires storage of an input signal during a row access procedure for subsequent
use during a column access procedure.

Ground 5

25.   Requester 1 asserts that claims 1-51 are obvious over Amidi in view of Dell 2. Proposed
rejection is **not adopted**. See Grounds 3 and 4 above. Requester 1 asserts that "[t]o the extent
that [Amidi] does not explicitly show that the logic element receives a bank address signal,
Requester submits that [Dell 2] makes up for such deficiency" (Request 1, p. 162). Requester 1

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further explains that Dell 2 teaches a logic circuit that receives a number of bank signals at

c2:44-49 and concludes that it would have been obvious to combine the teachings of the

references to realize larger memory capacity at a lower cost. The proposed rejection is deficient

because it does not show how the combination results in a memory module that teaches all of the

limitations of the claims. Amidi also teaches a logic circuit (register) that receives a number of

bank signals. Thus, Dell 2's teaching as used in the proposed rejection does not add anything

that is not taught by Amidi. There is no explanation as to how Dell 2's teaching can be adopted

so that the combination teaches the logic element as well as the register.

26.   Proposed rejection of claims 16, 17, and 21 is **not adopted**. With respect to claims 16

and 17, see the discussion of these claims above.

27.   With respect to claim 21, Requester 1 points to c8:29-41 of Dell 2's specification that

teaches storing a re-mapped BA1 signal supplied at RAS time to re-send at CAS time. However,

Requester 1 does not make it clear how this teaching can be combined with Amidi to result in a

memory module of claim 21. Requester 1's proposed rejection provides mapping of teachings

from both Amidi and Dell 2 to different elements of claim 21, without providing any guidance as

to how the teachings from the two references are to be combined to result in a memory module

that discloses all of the limitations of claim 21. Amidi discloses a memory module that uses the

column address bit A11 to determine the active rank (see paragraph 57). Amidi does not appear

to use a signal supplied during a row access procedure. It is not clear how Dell 2's teaching of

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retaining the re-mapped BA1 signal can be applied in Amidi's memory module. Bank address

signals are not re-mapped in Amidi's memory module.

Ground 6

28.   Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45,

and 50 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34, 36-39, 41-43, 45, and 50, is **adopted**.

29.   Claims 1, 3-4, 6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34, 36-39, 41-43, 45, and

50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of

JEDEC 21-C.

30.   With respect to claim 1, Amidi discloses **a memory module** (Figure 4) **connectable to a**

computer system, the memory module comprising:

    a printed circuit board (see Figure 4, 400);

    a plurality of double data rate (DDR) memory devices (404) mounted to the printed

circuit board, the plurality of memory devices having a first number of memory devices

arranged in a first number of ranks (see Figure 4, the module has four ranks);

    a circuit mounted to the printed circuit board, the circuit comprising a logic element

(see Figure 6, CPLD 604 and register 608), **the logic element receiving a set of input control**

signals (see Figure 6, the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and

signals) **from the computer system, the set of input control signals comprising at least one**

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row/column address signal (Add[n:0]), bank address signals (BA[1:0]), and at least one chip

select signal (cs0), the set of input control signals corresponding to a second number of

memory devices arranged in a second number of ranks, the second number of memory

devices smaller than the first number of memory devices and the second number of ranks

less than the first number of ranks (see paragraphs 10-12, Amidi's invention is a transparent

four rank module fitting into a memory socket meant for a two rank module), the circuit

generating a set of output control signals in response to the set of input control signals, the

set of output control signals corresponding to the first number of memory devices arranged

in the first number of ranks, wherein the circuit further responds to a first command signal

and the set of input control signals from the computer system by generating and

transmitting a second command signal and the set of output control signals to the plurality

of memory devices, the first command signal and the set of input control signals

corresponding to the second number of ranks and the second command signal and the set

of output control signals corresponding to the first number of ranks (see Figure 6 and

paragraph 52, "CPLD also ensures that all commands for a two rank memory module conveyed

by the module connector 602 are also performed on the four rank memory modules. For

example, CPLD 604 generates rsc2 and rcs3 ..."); and

        a phase-lock loop device (412) mounted to the printed circuit board, the phase-lock

loop device operatively coupled to the plurality of memory devices, the logic element, and

the register.

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31.   However, Amid does not specifically disclose a register that is separate and distinct from

the logic element (604 and 608) above. On the other hand, JEDEC 21-C discloses a DDR

SDRAM Registered DIMM Design Specification that uses two registers (see JEDEC 21-C, p.

4.20.4-18). Adopting the JEDEC DIMM design would involve replacing Register 608 with two

registers, Register 1 and Register 2 as specified on p. 4.204.-18. In the resulting JEDEC

compliant design, the logic element limitation is taught by the combination of CPLD 604

(row/column address signal Add(n), chip select signals cs0 and cs1) and JEDEC Register 2 (bank

address signals BA0 and BA1). The register limitation is taught by Register1.

32.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Amidi and JEDEC 21-C before him at the time the invention was made, to design Amidi's

DIMM according to the JEDEC standard to have a marketable memory module that conforms to

the industry standard.

33.   With respect to claim 3, **the set of input control signals comprises a first number of

chip-select signals** (see Figure 4, cs0 and cs1) **and wherein the set of output control signals

comprises a second number of chip-select signals greater than the first number of chip-

select signals** (rcs0a-rcs3a).

34.   With respect to claim 4, **the first number of chip-select signals is two and the second

number of chip-select signals is four** (see the discussion of claim 3 above).

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35.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Figure 6, CPLD).

36.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

37.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board** (Figure 4A, ranks 0 and 2 are on the front side), **a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board** (Figure 4B, ranks 1 and 3 are on the back side), **the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set** (this is inherent as two physical devices cannot occupy the same space at the same time).

38.   With respect to claim 11, **the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side** (see paragraph 34, the devices are stacked on the front and the back side).

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39.   With respect to claims 15 and 28 see the discussion of claim 1 above.

40.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

41.   With respect to claim 18, **the command signal is transmitted to two ranks of the first
number of ranks at a time** (see Figure 6 and paragraph 52).

42.   With respect to claim 19, **the command signal comprises a refresh command signal**
(see paragraph 52).

43.   With respect to claim 20, **the command signal is transmitted to the two ranks of the
first number of ranks concurrently** (see claim 18 above).

44.   With respect to claim 22, **the command signal comprises a read command signal or a
write command signal** (read and write commands are inherent in any functioning DIMM), **the
set of input signals comprises a density bit which is a row address bit** (the specification
describes the density bit simply as a row address bit that is latched during the activate command
for the selected bank, with no other attribute), **and the circuit is configured to store the row
address bit during an activate command for a selected bank** (see Figure 6, register).

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45.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Figure 6, CPLD).

46.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see Figure 6).

47.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

48.   With respect to claims 31 and 32, see the discussion of claim 3 above.

49.   With respect to claim 34, **the first number of ranks is four and the second number of ranks is two** (paragraph 41).

50.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (paragraph 52).

51.   With respect to claim 37, **the input command signal is a precharge signal and the output command signal is a precharge signal** (paragraph 52).

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52.   With respect to claim 38, **the input command signal is a read signal or a write signal
and the output command signal is a read signal or a write signal**. See the discussion of claim
37 above.

53.   With respect to claim 39, see claims 1 and 3 above.

54.   With respect to claims 10 and 11, spacing of memory devices is also an obvious matter of
design choice subject to constraints imposed by various practical engineering, manufacturing,
marketing, cost, and other considerations.

55.   Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**. With respect to claims
7, 9, 33, and 44, the combination as applied discloses only one register that does not receive a
bank address. With respect to claim 21, see the discussion of this claim above.

56.   Requester 2 asserts that claims 52-75 and 77-118 are obvious over Amidi in view of
JEDEC standards. Proposed rejection of claims 52, 57, 61-71, 75, 77-91, 94, 96, 98, 100, and
102-118 is **adopted**.

57.   Claims 52, 57, 61-65, 67-71, 75, 77-91, 94, 96, 98, 100, and 102-118 are rejected under
35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of JEDEC 21-C.

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58.   With respect to claim 52, **the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip- select signals of the set Of output control signals** (see claim 1 above), **the first number of chip-select signals generated by the logic element equal to the first number of ranks** (see Amidi, Figure 6, CPLD 604, rcs0-4), **and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks** (cs0, cs1).

59.   With respect to claim 57, **operation of the register is responsive at least in part to clock signals received from the phase-lock loop device** (see Amidi, Figure 6) **and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device** (see claim 1 above, PLL supplies clock signals to the registers), **the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks** (see claim 52).

60.   With respect to claim 61, **the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data**

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width per DDR memory device, a memory density per DDR memory device, a number of

ranks of DDR memory devices, and a memory density per rank,

the memory module further comprising a read-only non-volatile memory device

storing data accessible to the computer system (Amidi, Figure 4A, SPD 414; JEDEC, p. 4.20-

4.68, Serial PD definition), wherein the data characterizes the plurality of DDR memory

devices as having at least one value of the at least one attribute (SPD Definition, bytes #5 and

#31, Number of Physical Banks on DIMM and Module Bank Density) that is different from an

actual value of the at least one attribute of the plurality of DDR memory devices (see

Bagherzadeh Declaration, ¶ 48, "One skilled in the art would understand that in order to appear

transparent to the computer system, which generally cannot use a four rank memory module, the

SPD device taught by Amidi must store data characterizing the module as a two rank module of

different memory density").

61.   With respect to claim 62, the at least one attribute comprises the number of ranks of

DDR memory devices and the memory density per rank (SPD Definition, byte #31).

62.   With respect to claim 63, the data characterizes the plurality of DDR memory devices

as having fewer ranks of DDR memory devices than the plurality of DDR memory devices

actually has, and as having a greater memory density per rank than the plurality of DDR

memory devices actually has (see claims 57 and 61).

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63.   With respect to claim 64, **the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices** (see Amidi, Figure 5 and paragraph 43).

.

64.   With respect to claim 65, **the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries** (see Amidi, Figure 5 and paragraph 43).

65.   With respect to claims 67 and 82, **the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals** (see claim 52).

66.   With respect to claim 68, **the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device** (see Amidi, Figure 6), **wherein the memory module is operable for use in a server system** (DIMM memory modules can be used in a server system or any other system that can accept DIMM modules).

67.   With respect to claims 69, 102, and 103, see claim 64.

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68.   With respect to claims 70, 78, 83, 88, 104, and 105, see claim 65.

69.   With respect to claim 71, **the bank address signals include bank address signals**

received during an activate command operation and bank address signals received during

a read or write command operation subsequent to the activate command operation, and the

rank-selecting signals are used for the read or write command operation (these limitations

are inherent in any functioning DIMM with multiple ranks).

70.   With respect to claims 75, 80, 85, and 90, see claim 61 above.

71.   With respect to claims 77 and 87, **the logic element is responsive at least in part to the**

bank address signals and the at least one chip-select signal of the set of input signals by

generating a number of rank-selecting signals of the set of output signals that is greater

than double or equal to double the number of chip-select signals of the set of input signals

(see claim 52 above).

72.   With respect to claims 79, 84, and 89, **the plurality of DDR memory devices and the**

logic element are timed to clock signals from the phase-lock loop device (see claim 57).

73.   With respect to claims 81, 86, and 91, **the one or more attributes comprise the number**

of ranks of DDR memory devices and the memory density per rank and the data

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characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory

devices than the plurality of DDR memory devices actually has, and as having a greater

memory density per rank than the plurality of DDR memory devices actually has (see claim

63).

74.   With respect to claims 94, 96, 98, and 100, **the logic element receives a bit of a non-**

bank address signal of the set of input control signals (Figure 6, cs0 and cs1) **in conjunction**

with an activate command (activate command is used to open a row in a particular bank for

read or write) **and uses the bit to generate rank-selecting signals** (see Figure 5, cs0 and cs1

bits are used to select an active bank) **for a subsequent read or write command.**

75.   With respect to claims 106, 107, and 108, **the logic element comprises means for using**

at least one address bit received by the memory module during an activate command

operation to generate chip-select signals for a read or write command operation, the read

or write command operation subsequent to the activate command operation (see claim 94).

76.   With respect to claims 109-111, **the memory module comprises means for**

characterizing the plurality of DDR memory devices as having one or more attributes that

are different from actual attributes of the plurality of DDR memory devices (see claim 61).

77   With respect to claims 112-114, **the logic element comprises means for performing**

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sequential and combinatorial logic procedures (see Amidi, Figure 8) **to generate rank-**

selecting signals of the set of output control signals (see claim 94).

78.   With respect to claims 115 and 117, **the first command signal is a row access**

command signal, and the logic element uses sequential and combinatorial logic procedures

with at least one address bit of the set of input control signals (see Amidi, Figure 8) **and the**

at least one chip-select signal to generate chip-select signals for the second command signal

(see claim 94).

79.   With respect to claims 116 and 118, **the logic element further uses the sequential and**

combinatorial logic procedures with the at least one address bit (see Figure 8) **to generate**

chip-select signals for a column access command signal subsequent to the row access

command signal, wherein the memory module receives a second column access command

signal between receiving the row access command signal and the subsequent column access

command signal (see claim 94).

80.   Proposed rejection of claims 53-56, 58-60, 66, 72-74, 92-93, 95, 97, 99, and 101, is **not**

adopted.

81.   With respect to claims 53-56 and 58-60, Amidi does not disclose that the register receive

and buffers the bank address signal. Although Amidi does disclose a register that receives bank

address signals, the rejection of the parent claim 1, relies on Register2 of JEDEC to teach the

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claimed "logic element" with Register 1 teaching the "register" limitation of the claims. Register

1 of JEDEC does not receive bank address signals.

82.   With respect to claims 66, Amidi does not disclose that CAS or chip-select signals are

generated in response to bank address signals.

83.   With respect to claims 72-74, the claims require generation of rank-selecting signal that

select none of the ranks and two ranks. Amidi and JEDEC combination does not disclose these

no-rank and two-rank selecting signals.

84.   With respect to claims 92 and 93, the claims require the logic element not to operate in

response to row/column address bits (A_0 - A_n). The logic element of the combination used to

reject the parent claims does operate in response to A_0, A_1, and A_{10}.

85.   With respect to claims 95, 99 and 101, the Amidi and JEDEC combination does not teach

that the bank address signals are used to generate rank-selecting signals. In the combination,

chip-select and A_n signals are used to generate rank-selecting signals.

86.   With respect to claim 97, in the proposed combination bank address signals are not used

to generate the rank-selecting signals for a subsequent read or write command.

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87.   Requester 1 asserts that claims 56, 60-63, 90-91, and 109-111 are obvious over Amidi in

view of JEDEC standards. Proposed rejection of claims 61-63, 90-91, and 109-111 is **adopted**.

See above. Proposed rejection of claims 56 and 60 is **not adopted**. See above.

Ground 7

88.   The Examiner notes that Requester has failed to properly raise a substantial new question

of patentability based on Murdocca and Dell 2 combination. Nevertheless, Requester's proposed

rejection based on Murdocca and Dell 2 has been considered on the merit as discussed below.

89.   Requester 1 asserts that claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42, and 51 are

obvious over Murdocca and Dell 2. The proposed rejection is **not adopted**.

90.   Requester 1 identified Murdocca's 1-to-2 decoder, shown on page 250, as the logic

element that receives a set input control signals from the computer system, the set of input

control signals comprising at least one row/column address signal, bank address signal, and at

least one chip select signal. Requester asserts that it would have been obvious to combine the

method for constructing larger RAMs from smaller RAMs disclosed in Murdocca with the logic

element disclose in Dell 2 that receives a number of address inputs and a number of bank address

signals. However, Requester fails to explain how the proposed combination would result in the

claimed logic element. For example, Requester does not explain how Murdocca's 1-to-2 decoder

that takes one address signal as input and a chip select signal as a control signal to produce two

output signals can accommodate bank address signals and how the output bank address signals

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are used to construct the claimed circuit. A combination proposed cannot be just a patchwork of different circuit elements that teach different limitations of the claim. In addition to containing all of the limitations of the claim, the proposed combined circuit must make sense in terms of its overall structure and function. It must work as a unit that comprises all of the claimed structural features and be functional as a unit in the manner claimed.

91.   Moreover, all claims require a circuit that "responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signal to the plurality of memory devices." Requester 1 asserts that Murdocca's teaching of a 1-to-2 decoder and Dell 2's disclosure at c2:44-49 and c8:32-41 disclose the circuit. The 1-to-2 decoder taught by Murdocca is an address decoder. It does not respond to a command. Nor does it generate any command. Dell 2's circuit that remaps addresses does not respond to a command by generating another command as required by the claims. Therefore, the proposed combination does not teach a circuit that responds to a first command by generating and transmitting a second command as required by the claims.

Ground 8

92.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are anticipated by Dell 1. Proposed rejection is **not adopted**. Claims are anticipated when a single reference teaches all of the limitations of the claims. Requester 2's proposed rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For

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example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C

"establishes that a DIMM has a PLL mounted to the printed circuit board" (Request 2, p. 63).

However, Requester 2 fails to explain where in Dell 1 a PLL is taught or how JEDEC 21-C's

teaching of a PLL is attributable to Dell 1.

Ground 9

93.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are obvious over Dell 1 in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6, 8, 15, 18-20, 22, 24-25, 27-29, 31-32, 36-39, 41-43, 45, and 50 is **adopted**.

94.   Claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31-32, 36-39, 41-43, 45, and 50 are

rejected under 35 U.S.C. 103(a) as being as being unpatentable over Dell 1 in view of JEDEC

21-C.

95.   With respect to claim 1, Dell 1 discloses **a memory module** (see Figure 3, DIMM with

two banks of memory chips) **connectable to a computer system, the memory module**

comprising:

    a printed circuit board (see c1:23-39, DIMMs for IBM PCs are implemented with

PCBs; see JEDE 21-C);

    a plurality of memory devices mounted to the printed circuit board (see Figure 3,

4Mx4 chips 40x), **the plurality of memory devices having a first number of memory devices**

arranged in a first number of ranks (see Figure 3; see also c1:60-67, 36 devices in two banks);

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       a circuit mounted to the printed circuit board, the circuit comprising a logic element and, the logic element receiving a set of input control signals (see Figure 3, the DIMM receives RAS, CAS, OE, WE, and A0-A11 signals) **from the computer system, the set of input control signals comprising at least** four address signals (A0-A11), **the set of input control signals corresponding to a second number of memory devices arranged in a second number of ranks** (see c1:46-53, 60-67, nine devices in one bank), **the second number of memory devices smaller than the first number of memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals** (see Figure 3, the circuit generates two CA0, two WE0, two OE0, RAS A, RAS B signals, and two sets of address signals A0-A10), **the set of output control signals corresponding to the first number of memory devices arranged in the first number of ranks** (the set of output control signals correspond to 36 4Mx4 devices arranged in two banks), **wherein the circuit further responds to a first command signal** (CBR refresh for one bank of 8Mx8 memory devices) **and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices** (see c6:22-29, Dell 1 disclose generating a CBR refresh command to both banks of 4Mx4 memory devices by activating two RAS signals), **the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks.**

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96.   However, Dell 1 does not specifically disclose that 1) the memory devices are **double-**

data-rate (DDR) devices, 2) the circuit comprises **a register**, 3) the address signals comprise at

least **one row/column address signal, bank address signals, and at least one chip-select**

signal, and 4) the memory module comprises **a phase-lock loop device mounted to the printed**

circuit board, the phase-lock loop device operatively coupled to the plurality of memory

devices, the logic element, and the register. On the other hand, JECED 21-C discloses 1) the

use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20.4-

18, Register 1), 3) address signals that comprise at least one row/column signal (p. 4.20.4-18,

Register 2, input signal A0), bank address signals (BA0-BA1), at least one chip-select signal

(S0), and 4) a phase-lock loop device mounted to the printed circuit board (p. 4.20.4-29) that is

operatively coupled to other elements of the module (see p. 4.20.4-17).

97.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Dell 1 and JEDEC 21-C before him at the time the invention was made, to design the DIMM of

Dell 1 in compliance with the JEDEC standard to make it compatible with computer systems that

expect DIMMs installed in the system to be standard compliant.

98.   With respect to claim 3, **the set of input control signals comprises a first number of**

chip-select signals (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip

select signal lines; a set of input signals with four chip select signals comprise two chip select

signals) **and wherein the set of output control signals comprises a second number of chip-**

select signals greater than the first number of chip-select signals (see JEDEC 21-C, p. 4.20.4-

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12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip

select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3,

would generate four output signal lines, RS0-RS3).

99.   With respect to claim 4, **the first number of chip-select signals is two and the second number of chip-select signals is four** (see the discussion of claim 3 above).

100.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Dell 1, c4:28-29).

101.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

102.   With respect to claims 15 and 28 see the discussion of claim 1 above.

103.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

104.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Dell 1, c6:28-30, CBR refresh command refreshes both banks concurrently).

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105.   With respect to claim 19, **the command signal comprises a refresh command signal**
(see the discussion of claim 18 above).

106.   With respect to claim 20, **the command signal is transmitted to the two ranks of the
first number of ranks concurrently** (see claim 18 above).

107.   With respect to claim 22, **the command signal comprises a read command signal or a
write command signal** (read and write commands are inherent in any functioning DIMM such
as the one disclosed by Dell 1 and JEDEC), **the set of input signals comprises a density bit
which is a row address bit** (the specification describes the density bit simply as a row address
bit that is latched during the activate command for the selected bank, with no other attribute),
**and the circuit is configured to store the row address bit during an activate command for a
selected bank** (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an
activate command to activate a row requires row address bits).

108.   With respect to claims 24, 29 and 41, **the logic element comprises an application-
specific integrated circuit** (see Dell 1, c4:28-29), **a field-programmable gate array, a custom-
designed semiconductor device, or a complex programmable-logic device.**

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109.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see JEDEC 21-C, p. 4.20.4-10).

110.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

111.   With respect to claims 31 and 32, see the discussion of claim 3 above.

112.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Dell 1, c6:28-30).

113.   With respect to claim 37, although Dell 1 and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal,** they do disclose receiving input commands and generating output commands as claimed. One of ordinary skill in the art would realize that Dell 1's high density DIMM with RAS address re-mapping must work for all commands, not just the ones specifically mentioned in the disclosure.

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113.   With respect to claim 38, Dell 1 and JEDEC 21-C discloses that **the input command
signal is a read signal or a write signal and the output command signal is a read signal or a
write signal**. See the discussion of claim 37 above.

114.   With respect to claim 39, see claims 1 and 3 above.

115.   Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**. With respect to claims
7, 9, 33, and 44, the combination as applied discloses only one register that does not receive a
bank address. With respect to claim 21, Requester asserts that JEDEC 21-C "teaches that all
input control signals to DIMM pass through the register, which stores them internally before re-
driving them, including during a column access procedure" citing pages 40.20.4-67 and 40.20.4-
11 (Request 2, pp. 242-243). However, Requester fails to explain how those pages teach the
actual limitation "wherein the configured to store an input signal of the set of input signal during
a row access procedure for subsequent use during a column access procedure." The Examiner
cannot ascertain which input signal stored during a row access procedure is retained for
subsequent use during a column access procedure from the cited pages.

Ground 10

116.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,
and 50 are anticipated by Wong. Proposed rejection is **not adopted**. Claims are anticipated
when a single reference teaches all of the limitations of the claims. Requester's proposed
rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For

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example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C "explains

that a DIMM has a PLL mounted to the printed circuit board" (Request, p. 674). However,

Requester fails to explain where in Wong a PLL is taught or how JEDEC 21-C's teaching of a

PLL is attributable to Wong.

Ground 11

117.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are obvious over Wong in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6, 8, 15, 18-20, 22, 24-25, 27-29, 31-30, 36-39, 41-43, 45, and 50, is **adopted**.

118.   Claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31-30, 36-39, 41-43, 45, and 50 are

rejected under 35 U.S.C. 103(a) as being as being unpatentable over Wong in view of JEDEC

21-C.

119.   With respect to claim 1, Wong discloses **a memory module** (see Figure 3, DIMM with

two banks of memory chips) **connectable to a computer system, the memory module

comprising:**

        a printed circuit board (see Figure 3, 1000);

        a plurality of memory devices mounted to the printed circuit board (Figure 3, 1002),

**the plurality of memory devices having a first number of memory devices arranged in a

first number of ranks** (1012 and 1012);

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       a circuit mounted to the printed circuit board, the circuit comprising a logic element and, the logic element receiving a set of input control signals (see Figures 4A and 4B) **from the computer system, the set of input control signals comprising at least** four address signals (A0-A13)**, the set of input control signals corresponding to a second number of memory devices arranged in a second number of ranks** (see c2:1-10, Wong discloses that a separate bank of memory typically requires at minimum either a unique RAS or unique CAS for each bank; see Figure 4, the input signal set contains one RAS and one CAS, i.e., a set for a single bank)**, the second number of memory devices smaller than the first number of memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals** (see Figure 4, the circuit generates two CAS, two WE, two RAS signals, and two sets of address signals A0-A12)**, the set of output control signals corresponding to the first number of memory devices arranged in the first number of ranks** (the set of output control signals correspond to 36 4Mx4 devices arranged in two banks)**, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices** (c2:30-34, CBR refresh for both banks)**, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks.**

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110.   However, Wong does not specifically disclose that 1) the memory devices are **double-data-rate (DDR)** devices, 2) the circuit comprises **a register**, 3) the address signals comprise at least **one row/column address signal, bank address signals, and at least one chip-select signal**, and 4) the memory module comprises **a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of memory devices, the logic element, and the register.** On the other hand, JECED 21-C discloses 1) the use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20.4-18, Register 1), 3) address signals that comprise at least one row/column signal (p. 4.20.4-18, input signal A0), bank address signals (BA0-BA1), at least one chip-select signal (S0), and 4) a phase-lock loop device mounted to the printed circuit board (p. 4.20.4-29) that is operatively coupled to other elements of the module (see p. 4.20.4-17).

111.   It would have been obvious to one of ordinary skill in the art, having the teachings of Wong and JEDEC 21-C before him at the time the invention was made, to design the DIMM of Wong in compliance with the JEDEC standard to make it compatible with computer systems that expect DIMMs installed in the system to be standard compliant.

112.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip select signal lines; a set of input signals with four chip select signals comprise two chip select signals) **and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-

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12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip

select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3,

would generate four output signal lines, RS0-RS3).

113.   With respect to claim 4, **the first number of chip-select signals is two and the second
number of chip-select signals is four** (see the discussion of claim 3 above).

114.   With respect to claim 6, **the logic element comprises an application-specific
integrated circuit, a field-programmable gate array, a custom-designed semiconductor
device, or a complex programmable-logic device** (see Wong, c2:41-44).

115.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and
the logic element are portions of a single component** (these are all portions of a single DIMM
which is a component of a personal computer).

116.   With respect to claims 15 and 28 see the discussion of claim 1 above.

117.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

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118.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Wong, c3:30-34).

119.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

120.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

121.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Wong and JEDEC), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an activate command to activate a row requires row address bits).

122.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Wong, c2:41-42).

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123.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see JEDEC 21-C, p. 4.20.4-10).

124.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

125.   With respect to claims 31 and 32, see the discussion of claim 3 above.

126.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Wong, c2:28-34).

127.   With respect to claim 37, although Wong and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal**, they do disclose receiving input commands and generating output commands as claimed. One of ordinary skill in the art would realize that Wong's memory expansion module including multiple memory banks and a bank control circuit must work for all commands, not just the ones specifically mentioned in the disclosure.

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128.   With respect to claim 38, Wong and JEDEC 21-C discloses that **the input command
signal is a read signal or a write signal and the output command signal is a read signal or a
write signal**. See the discussion of claim 37 above.

129.   With respect to claim 39, see claims 1 and 3 above.

130.   Proposed rejection of claims 21 is **not adopted**. Requester asserts that JEDEC 21-C
"teaches that all input control signals to DIMM pass through the register, which stores them
internally before re-driving them, including during a column access procedure" citing pages
40.20.4-67 and 40.20.4-14 (Request, pp. 856-857). However, Requester fails to explain how
those pages teach the actual limitation "wherein the configured to store an input signal of the set
of input signal during a row access procedure for subsequent use during a column access
procedure." The Examiner cannot ascertain which input signal stored during a row access
procedure is retained for subsequent use during a column access procedure from the cited pages.

Ground 12

131.   Requester 3 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,
and 50 are obvious over Micron in view of Connelly. Proposed rejection of claims 1, 3-4, 6-8,
10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

132.   Claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are
rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connolly.

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133.   With respect to claim 1, Micron discloses **a memory module** (Figures 1-3) **connectable
to a computer system, the memory module comprising:**

    a printed circuit board (see Figure 1);

    a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted
to the printed circuit board, the plurality of memory devices having a first number of
memory devices arranged in a first number of ranks** (see Figure 4, the module has two
ranks);

    **a circuit mounted to the printed circuit board, the circuit comprising a logic element
and** (p. 4, Figure 4, Register U37) **a register** (Register U38), **the logic element receiving a set
of input control signals** (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #)
**from the computer system, the set of input control signals comprising at least one
row/column address signal** (A0-A12), **bank address signals** (BA0, BA1), **and at least one
chip select signal** (S0); **and**

    a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,
the phase-lock loop device operatively coupled to the plurality of memory devices, the logic
element, and the register.**

134.   However, Micron does not specifically disclose that "the set of input control signals
corresponding to a second number of memory devices arranged in a second number of ranks, the
second number of memory devices smaller than the first number of memory devices and the
second number of ranks less than the first number of ranks, the circuit generating a set of output

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control signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of ranks,

wherein the circuit further responds to a first command signal and the set of input control signals

from the computer system by generating and transmitting a second command signal and the set

of output control signals to the plurality of memory devices, the first command signal and the set

of input control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks."

135.   On the other hand, Connolly discloses a DIMM that receives a set of input control signals

(Figure 3, RAS, CAS, OE, WE, A0-A11), **the set of input control signals corresponding to a**

second number of memory devices arranged in a second number of ranks (see Figure 2,

there are nine devices in one rank), **the second number of memory devices smaller than the**

first number of memory devices and the second number of ranks less than the first number

of ranks (see Figure 3, there are 36 devices in two ranks), **the circuit generating a set of output**

control signals in response to the set of input control signals (see Figure 3, the circuit

generates two CA0, two WE0, two OE0, RAS A, RAS B signals, and two sets of address signals

A0-A10), **the set of output control signals corresponding to the first number of memory**

devices arranged in the first number of ranks(the set of output control signals correspond to

36 4Mx4 devices arranged in two banks), **wherein the circuit further responds to a first**

command signal (CBR refresh for one bank of 8Mx8 memory devices) **and the set of input**

control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices

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(see c6:46-49, Connolly discloses generating a CBR refresh command to both banks of 4Mx4

memory devices by activating two RAS signals), **the first command signal and the set of input**

control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks.

136.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Micron and Connolly before him at the time the invention was made, to modify the design the

DIMM of Micron to incorporate Connolly's technique for converting system signals from one

address configuration to a different address configuration, to be able to use lower capacity

memory devices which can be much cheaper (see Connolly, c1:38-63).

137.   With respect to claim 3, **the set of input control signals comprises a first number of**

chip-select signals (see Micron, Figure 4, register input signal S0) **and wherein the set of**

output control signals comprises a second number of chip-select signals greater than the

first number of chip-select signals (register output signals S0 and S1).

138.   With respect to claim 4, Micron and Connolly do not specifically disclose that **the first**

number of chip-select signals is two and the second number of chip-select signals is four.

However, it would have been obvious to one of ordinary skill in the art to add two additional

chip select signals to design a module with more memory banks in order to increase the memory

capacity of the module.

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139.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Connolly, Figure 4, ASIC LOGIC 46).

140.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (see the rejection of claim 1).

141.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

142.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board** (Micron, Figure 7, U1-U10; see also Figure 8, U1-U6), **a second set of DDR memory devices on the first side of the printed circuit board** (Figure 7, U11-U18; Figure 8., U7-U12), **a third set of DDR memory devices on a second side of the printed circuit board** (Figure 7, U19-U28; Figure 8, U21-U26), **and a fourth set of DDR memory devices on the second side of the printed circuit board** (Figure 7, U29, U36; Figure 8, U28-U33), **the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set** (see Figure 7 and 8).

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143.   With respect to claim 11, **the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side** (see Figure 7 and 8).

144.   With respect to claims 15 and 28 see the discussion of claim 1 above.

145.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

146.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Connolly, c6:46-49, CBR refresh command refreshes both banks concurrently).

147.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

148.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

149.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Micron and Connolly; see also Micron Table 6), **the set of input signals**

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comprises a density bit which is a row address bit (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (Micron, Figure 4, row address bits are stored in a register and an activate command to activate a row requires row address bits).

150.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit** (Connolly, Figure 4), **a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.**

151.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (Micron, Figure 4).

152.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

153.   With respect to claims 31 and 32, see the discussion of claim 3 above.

154.   With respect to claims 33 and 44, **the register receives the bank address signals and the input command signal of the set of input control signals** (Micron, Figure 4).

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155.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Connolly, c6:46-49).

156.   With respect to claim 37, **the input command signal is a precharge signal and the output command signal is a precharge signal** (Micron, Table 6).

157.   With respect to claim 38, **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal** (Micron, Table 6).

158.   With respect to claim 39, see claims 1 and 3 above.

159.   Proposed rejection of claims 9 and 21 is **not adopted**. With respect to claim 9, the combination as applied discloses only one register. With respect to claim 21, see the discussion of this claim below.

Ground 13

160.   Requester 3 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are obvious over Micron in view of Amidi. Proposed rejection of claims 1, 3-4, 6-9, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

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161.   <u>Claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are</u>

<u>rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Amidi.</u>

162.   With respect to claim 1, Micron discloses **a memory module** (Figures 1-3) **connectable**

to a computer system, the memory module comprising:

    a printed circuit board (see Figure 1);

    a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted**

to the printed circuit board, the plurality of memory devices having a first number of

memory devices arranged in a first number of ranks (see Figure 4, the module has two

ranks);

    a circuit mounted to the printed circuit board, the circuit comprising a logic element

and (p.4, Figure 4, Register U37) **a register** (Register U38), **the logic element receiving a set of**

input control signals (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #)

from the computer system, the set of input control signals comprising at least one

row/column address signal (A0-A12), bank address signals (BA0, BA1), and at least one

chip select signal (S0); and

    a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,**

the phase-lock loop device operatively coupled to the plurality of memory devices, the logic

element, and the register.

163.   However, Micron does not specifically disclose that "the set of input control signals

corresponding to a second number of memory devices arranged in a second number of ranks, the

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second number of memory devices smaller than the first number of memory devices and the

second number of ranks less than the first number of ranks, the circuit generating a set of output

control signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of ranks,

wherein the circuit further responds to a first command signal and the set of input control signals

from the computer system by generating and transmitting a second command signal and the set

of output control signals to the plurality of memory devices, the first command signal and the set

of input control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks."

164.   On the other hand, Amidi discloses a DIMM that receives a set of input control signals

(see Figure 6, the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and signals),

the set of input control signals comprising at least one row/column address signal

(Add[n:0]), bank address signals (BA[1:0]), and at least one chip select signal (cs0), the set

of input control signals corresponding to a second number of memory devices arranged in

a second number of ranks, the second number of memory devices smaller than the first

number of memory devices and the second number of ranks less than the first number of

ranks (see paragraphs 10-12, Amidi's invention is a transparent four rank module fitting into a

memory socket meant for a two rank module), **the circuit generating a set of output control**

signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of

ranks, wherein the circuit further responds to a first command signal and the set of input

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control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices,

the first command signal and the set of input control signals corresponding to the second

number of ranks and the second command signal and the set of output control signals

corresponding to the first number of ranks (see Figure 6 and paragraph 52, "CPLD also

ensures that all commands for a two rank memory module conveyed by the module connector

602 are also performed on the four rank memory modules. For example, CPLD 604 generates

rsc2 and rcs3 ...").

165.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Micron and Amidi before him at the time the invention was made, to modify the design the

DIMM of Micron to adopt Amidi's transparent four rank memory module for standard two rank

sub-system teachings to be able to use lower capacity memory devices which can be much

cheaper (Amidi, p. 1, paragraph 8).

166.   With respect to claim 3, **the set of input control signals comprises a first number of**

chip-select signals (see Amidi, Figure 4, cs0 and cs1) **and wherein the set of output control**

signals comprises a second number of chip-select signals greater than the first number of

chip-select signals (rcs0a-rcs3a).

167.   With respect to claim 4, **the first number of chip-select signals is two and the second**

number of chip-select signals is four (see the discussion of claim 3 above).

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168.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Amidi, Figure 6, CPLD).

169.   With respect to claim 7, **the bank address signals of the set of input control signals are received by both the logic element and the register** (se claim 1).

170.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

171.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board** (Amidi, Figure 4A, ranks 0 and 2 are on the front side), **a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board** (Figure 4B, ranks 1 and 3 are on the back side), **the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set** (this is inherent as two physical devices cannot occupy the same space at the same time).   Micron discloses this limitation as well. See the discussion of claim 10 above.

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172.   With respect to claim 11, **the DDR memory devices of the second set are spaced from**

the DDR memory devices of the first set in a direction along the first side and the memory

devices of the fourth set are spaced from the memory devices of the third set in a direction

along the second side (see Amidi, paragraph 34, the devices are stacked on the front and the

back side; see also Micron, Figures 7 and 8).

173.   With respect to claims 15 and 28 see the discussion of claim 1 above.

174.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

175.   With respect to claim 18, **the command signal is transmitted to two ranks of the first**

number of ranks at a time (see Amidi, Figure 6 and paragraph 52).

176.   With respect to claim 19, **the command signal comprises a refresh command signal**

(see Amidi, paragraph 52).

177.   With respect to claim 20, **the command signal is transmitted to the two ranks of the**

first number of ranks concurrently (see claim 18 above).

178.   With respect to claim 22, **the command signal comprises a read command signal or a**

write command signal (read and write commands are inherent in any functioning DIMM), **the**

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set of input signals comprises a density bit which is a row address bit (the specification

describes the density bit simply as a row address bit that is latched during the activate command

for the selected bank, with no other attribute)**, and the circuit is configured to store the row

address bit during an activate command for a selected bank** (see Amidi, Figure 6, register).

179.   With respect to claims 24, 29 and 41, **the logic element comprises an application-

specific integrated circuit, a field-programmable gate array, a custom-designed

semiconductor device, or a complex programmable-logic device** (Amidi, Figure 6, CPLD).

180.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of

row/column address signals received and buffered by the register and sent from the

register to the plurality of DDR memory devices** (see Amidi, Figure 6).

181.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the

register, and the logic element are portions of a single component** (see the discussion of

claim 8 above).

182.   With respect to claims 31 and 32, see the discussion of claim 3 above.

183.   With respect to claims 33 and 44, **the register receives the bank address signals and

the input command signal of the set of input control signals** (see claim 1).

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184.   With respect to claim 36, **the input command signal is a refresh signal and the output
command signal is a refresh signal** (Amidi, paragraph 52).

185.   With respect to claim 37, **the input command signal is a precharge signal and the
output command signal is a precharge signal** (Amidi, paragraph 52).

186.   With respect to claim 38, **the input command signal is a read signal or a write signal
and the output command signal is a read signal or a write signal**. See the discussion of claim
37 above.

187.   With respect to claim 39, see claims 1 and 3 above.

188.   Proposed rejection of claims 9 and 21 is **not adopted**. With respect to claim 9, the
combination as applied discloses only one register. With respect to claim 21, Requester cites
Table 6 of Micron and paragraph 61 of Amidi, without any explanation as to how the cited
passages disclose the limitation "wherein the configured to store an input signal of the set of
input signal during a row access procedure for subsequent use during a column access
procedure." The cited passages do not disclose that an input address signal stored during a row
access procedure is retained for subsequent use during a column access procedure from the cited
pages. Requester asserts that one of ordinary skill in the art would have known how to select and
store needed inputs for later use. However, requester fails to explain which "input signal from a

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row access procedure that would be needed in - but would otherwise be unavailable during -

subsequent column access procedure" would be saved for later use.

Ground 14

189.   Requester 1 asserts that claims 57-60, 68, 76, 79, 84, and 89-91 should be rejected under

35 U.S.C §112, first paragraph. Proposed rejection is **not adopted**. Requester 1 asserts that

persons of ordinary skill in the art would not know how the signal from the phase locked loop

was used by the logic element of the '912 patent, because neither the claims nor the description

of the '912 patent explain how this signal is used (Comment 1, p. 17). The Examiner disagrees.

The '912 patent specifically discloses that "[i]n response to signals received from the computer

system, the phase-locked loop device 50 transmits clocks signals to the plurality of memory

devices 30, the logic element 40, and the register 60" (c5:27-31). Requester 1's assertion that

one skilled in the art would not know how clock signals are used to drive digital circuit elements

of a memory decoder is not credible. Clocks are used to synchronize timing of operations of

various circuit elements in a digital device. Because clocks control the timing of operations,

generation of output signals in a logic circuit that uses clock signals to operate properly is

necessarily responsive at least in part to clock signals received.

190.   Requester 1 further asserts that "[t]he '912 patent simply does not describe any

relationship between output control signals and clock signals received from a phase-locked loop

device or a logic element time to the clock signals from a phase locked loop device" (Comments

1, p. 17). Requester 1's implicit assertion that because there is no detailed description of exactly

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how the clock signals are used to operate the circuits to generate output signals the '912 does not

disclose the new claim limitations is undermined by Requester 1's allegation that Amidi teaches

the limitations of claim 57 and other claims involving the clock signals from the PLL. There is

no detailed disclosure in Amidi of how the clock signals are used to generate the claimed output

signals. Yet, Requester 1 asserted that Amidi teaches the same limitations when Amidi's

disclosure with respect to the clock signals is no more detailed than the '912 patent's.

191.   Requester 1 asserts that claim 76 should be rejected because the claim requires DDR

DRAM packages that are chip packages beyond DDR3 chip packages and that it fails to

particularly point out and distinctly define the metes and bounds of chip packages beyond DDR3

chip packages. This is argument is not persuasive because the specification of the '912 patent

specifically discloses that "the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip

packages, or chip packages beyond DDR3 chip packages" at c12:26-29. As to the allegation of

indefiniteness, 35 U.S.C §112, first paragraph is not the proper ground for an indefiniteness

rejection.

Ground 15

192.   Requester 1 asserts that claim 76 should be rejected under 35 U.S.C §112, second

paragraph. Proposed rejection is **not adopted**. Requester asserts that claim 76 requires DDR

DRAM chips packages that are chip packages beyond DDR3 chip packages and that the term

beyond has no outer boundary and nothing in the specification attaches special meaning to

"beyond DDR3 packages" (Comments 1, p. 19). The Examiner first notes that claim 76 does not

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require chip packages beyond DDR3 chip packages because it is claimed as an alternative

limitation. Also the term beyond is not unbounded as Requester 1 asserts. When read in the

context of the specification and the claim, "beyond DDR3 chip packages" refers to the DDR

family or series of chip packages.

Ground 16

193.   Requester 2 asserts that claim 76 should be rejected as being obvious over Amidi in view

of JEDEC and Vogt. The propose rejection is **adopted**.

194.   <u>Claim 76 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in

view of JEDEC 21-C and Vogt.</u>

195.   Amidi and JEDEC disclose all of the limitations of the parent claim 75 (see Ground 6).

However, Amidid and JEDEC do not specifically disclose the DDR DRAM chip packages are

DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages. On

the other hand, Vogt specifically discloses a DIMM with DDR2 chips. It would have been

obvious to one of ordinary skill in the art, having the teachings of Amidi, JEDEC and Vogt

before him at the time of the invention, to use DDR2 chips in the DIMM module of Amidi and

JEDEC, to be able to offer upgraded DIMMs with the latest available memory chips.

Examiner's Statement of Reasons for Patentability/Confirmation

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196.   Claims 9, 21, 53-56, 58-60, 66, 72-74, 92-93, 95, 97, 99, and 101 are deemed to be

patentable and/or confirmed over the prior art of record for the following reasons: Claim 9

recites the limitation "the register comprises a plurality of register devices". Prior art references

as applied in this Office Action only disclose one register. Claim 21 requires storage of an input

signal during a row access procedure for subsequent use during a column access procedure. As

discussed above, prior art references or combination of references applied in this Office Action

do not disclose this input signal storage feature of claim 21. As to claims 53-56, 58-60, 66, 72-

74, 92-93, 95, 97, 99, and 101, see Ground 6 above.

Response to Arguments

Secondary Considerations

197.   Patent Owner asserts that Lopez and Lee Declarations submitted provide evidence of

secondary considerations (industry acceptance and praise by others) to overcome any prima facie

case of obviousness that may be presented (Response p. 36). Requester 1 asserts that Patent

Owner has not established a nexus between the claimed invention and evidence of commercial

success (Comments 1, p. 14). Requester 2 also asserts that Patent Owner has not demonstrated

any nexus between the "praise" of its HyperCloud product and the claimed features at issue

(Comments 2, p. 12). The Examiner agrees with Requesters 1 and 2, that Patent Owner has not

demonstrated any nexus between the "praise" and "acceptance" and the claimed features that are

found to be obvious.

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198.   Although Patent Owner attempts to establish that the "rank multiplication" technology

disclosed in the '912 patent is responsible for the praise and acceptance with the Lee Declaration,

the inventors of the '912 patent are not the first inventors of this technology as evidenced by the

prior art of record (Amidi, Connelly, Dell 1 & 2, etc.). This "rank multiplication" technology

was well known in the art before the date of the invention. An anticipated feature cannot be non-

obvious. To overcome the prima facie case of obviousness, Patent Owner must provide

objective evidence of non-obviousness that establishes a nexus between the "praise" and

"acceptance" and features in the claims that are found to be obvious. Patent Owner has failed to

even link the claims to the evidence, much less the obvious features of the claims.

Ground 1

199.   Requester 1 argues that "[t]he Examiner should reconsider the confirmation of

allowability of claims 1-17, 19, 21, and 23-51 over the QBMA Reference and the JEDEC DIMM

Standard" because although page 17 of the QBMA Reference does not explicitly show all of the

signals recited in the claims, page 17 is one of many pages in the QBMA (see Requester 1's

Comments, p. 68). Requester 1 alleges that the control signals used for controlling the QBM

switch are described elsewhere in the QBMA Reference and JEDEC Standard in sufficient detail

that a person of ordinary skill in the art would have been motivated and able to combine the

references in a manner that yielded the inventions claimed by the '912 patent. The Examiner

notes that the claims have not been confirmed as being allowable as Requester 1 alleges. These

claims have been rejected on other grounds. The Examiner's decision was not to adopt the

rejection as proposed by Requester 1 because the rejection was deficient.

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200.   Requester 1's argument has been fully considered but is not persuasive. Requester 1

specifically identified the QBM switch shown on page 17 as the structure that teaches the

claimed logic element. The claimed logic element is required to receive a set of input control

signals specified in the claims. Although these input control signals are shown in the QBMA

and JEDEC, the references do not disclose that the control signals are received by the QBM

switch as required. Input and output signals of the QBM switch are clearly identified on page

17. They do not include the specific set of control signals claimed (at least one row/address

signals, bank address signals, and at least one chip-select signal). If the input control signals

used for controlling the QBM switch are described elsewhere in QBMA as Requester 1 asserts,

Requester 1 has failed to explain where in the QBMA reference such a disclosure can be found.

Nor has Requester 1 shown how the combination of references discloses the claimed logic

element with all of the required input control signals, and why one skilled in the art would

modify the QBM switch of page 17 to accept the claimed input control signals.

201.   A prima facie case of obviousness cannot be made by merely throwing all the recited

structural elements from different disclosures into a combination and alleging that it would have

been obvious to make the combination. The combination must teach all of the structural

limitations and there must be an articulation of some reason to support the conclusion of

obviousness. In this case, the proposed combination simply does not teach all of the structural

limitations of the logic element and no reason has been given to modify the QBM switch to

receive all of the required control input signals.

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Ground 2

202.   Requester 1 asserts that a person of ordinary skill in the art would have been familiar with

the features of DDR DRAMs as described in industry standards, including the presence of chip

select signal inputs on the devices and that one skilled in the art would have known how to

modify or generate a chip-select signal consistent with the Dell 2 address translation scheme

(Comments 1, p. 70). The Examiner agrees that one skilled in the art would have been familiar

with chip select signals. In fact, a chip select signal is well known in the art. However, issue is

not whether a chip select signal is known in the art. The real issue is whether Requester 1 has

made a prima facie case of obviousness of modifying Dell 2's memory module so that it teaches

all the limitations of the claims. The proposed rejection is devoid of any articulation of reasons

as to why one skilled in the art would include a chip select input to the address re-mapping logic

circuit of Dell 2 and why it would have been obvious to modify the address re-mapping device to

generate output control signals. Mere allegation that these features are known in the art and that

it would have been obvious to include them is not enough to meet the burden of establishing the

prima facie case of obviousness.

Ground 3

203.   Patent Owner argues that a person of ordinary skill in the art would not interpret the term

"logic element" as encompassing both the translation logic device and the register that passes

signal onto the DRAM devices (Patent Owner's Response, p. 38). To the extent that Patent

Owner's arguments are directed to the application of Amidi in the anticipation rejection of the

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last Office Action, the Examiner agrees that the "logic element" and the "register" are separate

elements in the claims. However, there is nothing in the claims or the specification that

precludes the logic element from comprising a storage device such as a register. The term "logic

element" is not a term of art. Nor is the term specifically defined in the specification. Therefore,

the term is construed using the ordinary definition of the words used in the term. Thus, the

Examiner interprets the term "logic element" as an element that performs some kind of logic

function or an element that comprises a logic circuit. This interpretation is consistent with the

specification of the '912 patent.

204.   Patent Owner's other arguments are moot because the rejection is not adopted.

Grounds 4 and 5

205.   Patent Owner's other arguments are moot because the rejections are not adopted.

Ground 6

206.   Patent Owner's other arguments are moot because the rejection no longer relies on

Ground 3 as applied in the last Office Action.

Ground 7

207.   Requester 1 asserts that a person of ordinary skill in the art would have been motivated to

combine Murdocca's address decoding method with Dell 2 system, which provides address

remapping logic in an ASIC to handle reconfiguration of banks of memory devices (Comments

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1, p. 70). As explained above, Requester 1 has failed to show how the combination results in a

device that teaches all of the limitation of the claims.

Ground 9

208.   Patent Owner's argument that the combination of Dell 1 and JEDEC 21-C does not

disclose or render obvious a memory module having a logic element that receives bank address

signals as required (Response, p. 50) is moot because the rejection in this Office Action relies on

JEDEC Register 2 to receive bank address signals.

209.   Patent Owner next argues that the EDO devices used in Dell 1 do not have bank address

of memory locations that would be accessed using bank address signals, thus, there is no need to

receive such address signals (Response, p. 51). This is not a persuasive argument because the

rejection is based on the combination of Dell 1 and JEDEC and JEDEC discloses DDR DRAM

devices. The rejection specifically proposes using DDR DRAM devices as taught by JEDEC.

210.   Patent Owner also argues that due to the significant differences between DDR memory

technology and Dell 1's EDO technology, persons of ordinary skill in the art would not find it

obvious to replace the EDO memory devices of Dell 1 with the DDR memory devices of JEDEC

21-C as proposed (Response, p. 51). This argument is not persuasive. Although Patent Owner

asserts that Dell 1 teaches EDO devices, there is nothing in Dell 1 that confines the invention to

DIMMs made with EDO devices. Dell 1 does not identify the DRAMs used in the DIMM as

EDO DRAMs. The devices are generically referred to as DRAMs as opposed to SRAMs. In

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fact, Dell 1 specifically states that "it is understood that this description is made only by way of

example, that the invention is not limited to particular embodiments described herein, and that

various rearrangements, modifications, and substitutions may be implemented without departing

from the true spirit of the invention as hereinafter claimed" (c6:63-68). As evidenced by

JEDEC, one skilled in the art would know how to make a DIMM with DDR DRAM devices at

the time of the invention.

Ground 11

211.   See Ground 9 above.

Ground 12

212.   Patent Owner asserts that Micron does not disclose a memory module having a logic

element that receives bank address signals to generate output signals (Response, p. 57). The

Examiner disagrees. Micron discloses two registers U37 and U38 that receive bank address

signals and other signals required by the claims. As discussed above, there is nothing in the

claims or the specification that precludes the "logic element" from comprising a register so long

as there is at least one other register that teaches the claimed register limitation.

213.   Patent Owner's argument that one skilled in the art would not combine the teachings of

Micron and Connelly because of the difference between EDO and DDR addressing and

command protocols is based on Patent Owner's misinterpretation of the proposed combination.

It is not the EDO addressing teachings of Connelly, if there are such teachings in Connelly as

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asserted by Patent Owner (as far as the Examiner can discern, Connelly does not specify the type

of DRAMs used in the DIMMs), that are being combined with Micron's teaching of DIMM

modules. Connelly's teaching to be adopted is the technique of generating two RAS and CAS

signals from a set of one RAS and one CAS signals, so that two banks of lower density DRAM

chips can be used in a DIMM in place of a single bank of higher density chips.

214.   With respect to claim 21, Patent Owner explains that latching of SYS RAS only occurs

by "SYS_CAS going active (which will cause SYS RAS to be latched)" and that the address bit

A11 latched during a row access procedure is used to determine whether to make RAS A or RAS

B active during a row access procedure. Upon closer inspective of the reference, the Examiner

agrees with Patent Owner. Accordingly, the rejection of claim 21 adopted in the last Office

Action is withdrawn.

Ground 13

215.   See Grounds 6 and 12 above.

Submissions

216.   In order to ensure full consideration of any amendments, affidavits or declarations, or

other documents as evidence of patentability, such documents must be submitted in response to

this Office action. Submissions after the next Office action, which is intended to be an Action

Closing Prosecution (ACP), will be governed by 37 CFR 1.116(b) and (d), which will be strictly

enforced.

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Extensions of Time

217.   Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes*

reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant"

and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c)

requires that *inter partes* reexamination proceedings "will be conducted with special dispatch"

(37 CFR 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are

provided for in 37 CFR 1.956. Extensions of time are not available for third party requester

comments, because a comment period of 30 days from service of patent owner's response is set

by statute. 35 U.S.C. 314(b)(3).

Service of Papers

218.   Any paper filed with the USPTO, i.e., any submission made, by either the Patent Owner

or the Third Party .Requester must be served on every other party in the reexamination

proceeding, including any other third party requester that is part of the proceeding due to merger

of the reexamination proceedings. As proof of service, the party submitting the paper to the

Office must attach a Certificate of Service to the paper, which sets forth the name and address of

the party served and the method of service. Papers filed without the required Certificate of

Service may be denied consideration. 37 CFR 1.903; MPEP 2666.06.

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Amendment in Reexamination Proceedings

219.   Any proposed amendment to the specification and/or claims in this reexamination

proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37

CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). Amendments in an

inter partes reexamination proceeding are made in the same manner that amendments in an *ex

parte* reexamination are made. MPEP 2666.01. See MPEP 2250 for guidance as to the manner of

making amendments in a reexamination proceeding.

Notification of Concurrent Proceedings

220.   The patent owner is reminded of the continuing responsibility under 37 CFR 1.985(a), to

apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the

patent undergoing reexamination or any related patent throughout the course of this

reexamination proceeding. The third party requester is also reminded of the ability to similarly

inform the Office of any such activity or proceeding throughout the course of this reexamination

proceeding. See MPEP § 2686 and 2686.04.

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All correspondence relating to this *inter partes* reexamination proceeding should be directed as follows:

By **U.S. Postal Service Mail** to:

    Mail Stop *Inter Partes* Reexam
    ATTN: Central Reexamination Unit
    Commissioner for Patents
    P.O. Box 1450
    Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
               Central Reexamination Unit

By hand to: Customer Service Window
              Randolph Building
              401 Dulany St.
              Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/Woo H. Choi/

Woo H. Choi
Primary Examiner
Central Reexamination Unit 3992

EBK
ESK

OFFICE ACTION IN INTER PARTES *REEXAMINATION*	Control No. *1339* 95/000,578 *t579t*	Patent Under Reexamination 7619912	
	Examiner WOO H. CHOI	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on 7/5/2011
Third Party(ies) on 8/29/2011

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:
     2 MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.
For Third Party Requester's Comments on the Patent Owner Response:
     30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892
2. ☐ Information Disclosure Citation, PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims 1-118 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☒ Claims See Continuation Sheet are confirmed. [Unamended patent claims]
4. ☐ Claims _____ are patentable. [Amended or new claims]
5. ☒ Claims See Continuation Sheet are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____   ☐ are acceptable   ☐ are not acceptable.
8. ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has:
     ☐ been received.   ☐ not been received.   ☐ been filed in Application/Control No 95000578.
10. ☐ Other _____

Continuation Sheet (PTOL-2064)   **Control No. 95/000,578**

Continuation of SUMMARY OF ACTION:3. Claims confirmed.[Unamended patent claims]are 2, 5, 9, 16, 17, 21, 23, 30, 51, 54-60, 66, and 72-74.

Continuation of SUMMARY OF ACTION: 5. Claims rejected are 1, 3, 4, 6-7,10-15, 18-20 ,22, 24-29, 31-49, 52, 53, 61-65,67-71, and 75-118.

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INTER PARTES REEXAMINATION OFFICE ACTION

1.   This is an *inter partes* reexamination of U.S. Patent No. 7,619,912 ('912 patent). On

February 28, 2011 three *inter partes* proceedings, 95/000,578, 95/000,579, and 95/001,339

initiated based upon three different requests by Requester 2, Requester 3, and Requester 1,

respectively, have been merged. Clams 1-51 were subject to reexamination. In response to the

Office Action mailed April 4, 2011, Patent Owner added claims 52-118 without amending any of

the original claims. In response, all three requesters proposed new rejections of newly added

claims. Claims 1-118 are currently pending in this proceeding. This Office Action supersedes

the Officer Action mailed on October 4, 2011[1]. The references discussed herein are as follows:

- U.S. Patent No. 5,926,827 ("Dell 1");

- U.S. Patent No. 6,209,074 ("Dell 2");

- *Quad Band Memory (QBM^{TM}): DDR 200/266/333 devices producing DDR400/533/667*, QBM Alliance, Platform Conference, San Jose, California, January 23-24, 2002 ("QBMA");

- U.S. Patent No. 5,745,914 ("Connolly");

- U.S. Patent No. 6,414,868 ("Wong");

- U.S. Patent Application Publication No. 2006.0117152 ("Amidi");

- *Design Specification for PC2100 and PC1600 DDR SDRAM Registered DIMM*, JEDEC Standard No. 21-C, Revision 1.3, Release 11b, January 2002, ("JEDEC 21C");

- *Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications*, JEDEC Standard No. 82-4B, May 2003, ("JEDEC 82-4B");

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[1] Requester 3's Comments were not available in the official Image File Wrapper until after the prior Office Action was mailed. The Examiner recommends that parties use electronic filing to ensure that submissions are placed in the correct file wrapper. The Examiner also recommends that parties verify, through PAIR, that submitted papers are properly entered into the official record of the case.

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- *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79C, March 2003, ("JEDEC 79C");

- Micron, *DDR SDRAM RDIMM*, MT36VDDF12872 & MT36VDDF28672 Data Sheet © 2002, ("Micron");

- Murdocca, Miles, J., *Principles of Computer Architecture*, Prentice Hall, Inc., 2000 ("Murdocca").

- Vogt, Pete, "*Fully Buffered DIMM Server Memory Architecture: Capacity, Performance, Reliability, and Longevity,*" February 18, 2004 ("Vogt").

Statutory Bases for Rejections - 35 USC §§ 102 and 103

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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Summary of Rejections

4.   The following list is the summary of rejections in this Office action.

Ground 1: Obviousness over QBMA and JEDEC 21C (Proposed by Requester 1)

      Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 2: Obviousness over QBMA and Dell 2 (Proposed by Requester 1)

      Proposed rejection of claim 1-17, 19, 21, and 23-51 is **not adopted**.

Ground 3: Anticipation by Amidi (Proposed by Requesters 1 and 2)

      Rejection of claims 1-7, 9-11, 14-15, 18-21, 23-25, 28-34, 36-37, 40-43, 46, and

51, proposed by Requester 1, is **not adopted**.

      Rejection of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, and 41-

45, and 50, proposed by Requester 2, is **not adopted**.

Ground 4: Obviousness over Amidi (Proposed by Requester 1)

      Proposed rejection of claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, and 51 is **not
adopted**.

      Proposed rejection of new claims 52-55, 57-59, 64-89, 92-108, and 112-118 is **not
adopted**.

Ground 5: Obviousness over Amidi and Dell 2 (Proposed by Requester 1)

      Proposed rejection of claims 1-51 is **not adopted**.

Ground 6: Obviousness over Amidi and JEDEC (Proposed by Requesters 1 and 2)

      Rejection of claims 1, 3-4, 6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34,

36-39, 41-43, 45, and 50, proposed by Requester 2 is **adopted**.

      Rejection of claims 7, 9, 21, 33, and 44, proposed by Requester 2, is **not adopted**.

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The Examiner rejects claims 12-14, 40, and 46-49.

Rejection of new claims 61-63, 90-91, and 109-111, proposed by Requester 1 is **adopted**.

Rejection of new claims 56 and 60, proposed by Requester 1, is **not adopted**.

Rejection of new claims 52, 61-65, 67-71, 75, 77-91, 94, 96, 98, 100, and 102-118, proposed by Requester 2, is **adopted**.

Rejection of new claims 53-60, 66, 72-74, 92-93, 95, 97, 99, and 101, proposed by Requester 2, is **not adopted**.

Ground 7: Obviousness over Murdocca and Dell 2 (Proposed by Requester 1)

Proposed rejection of claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42 is **not adopted**.

Ground 8: Anticipation by Dell 1 (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **not adopted**.

Ground 9: Obviousness over Dell 1 and JEDEC standards (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 10: Anticipation by Wong (Proposed by Requester 2)

Proposed rejection of claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **not adopted**.

Ground 11: Obviousness over Wong and JEDEC standards (Proposed by Requester 2)

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Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31, 32, 36-39, 41-43, 45, and 50 is **adopted**.

Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**.

Ground 12: Obviousness over Micron and Connelly (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 is **adopted**.

Proposed rejection of claims 9 and 21 is **not adopted**.

The Examiner rejects claims 26 and 35.

Proposed rejection of new claims 64-65, 94, 96, 98, 102, 107, and 112-113 is **adopted**.

Proposed rejection of new claims 52-63, 66-93, 95, 97, 99-101, 103-106, 108-111, and 114-118 is **not adopted**.

Ground 13: Obviousness over Micron and Amidi (Proposed by Requester 3)

Proposed rejection of claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 is **adopted**.

Proposed rejection of claims 9 and 21 is **not adopted**.

The Examiner rejects claim 26.

Proposed rejection of new claims 52, 53, 61-65, 67-71, 75-91, 94, 96, 98, 100, and 102-118 is **adopted**.

Proposed rejection of new claims 54-60, 66, 72-74, 92-93, 95, 97, 99, and 101 is **not adopted**.

Ground 14: Lack of written description support (Proposed by Requesters 1 and 3)

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    Rejection of claims 57-60, 68, 76, 79, 84, and 89-91, proposed by Requester 1 is

not adopted.

    Rejection of claims 92-101 and 115-118, proposed by Requester 3, is **adopted**.

Ground 15: Lack of enablement (Proposed by Requester 3)

    Proposed rejection of claims 115-118 is **adopted**.

    Proposed rejection of claims 68-70, 76, 78, 82, 88, 94, 96, 98, 100, is **not**

adopted.

Ground 16: Indefiniteness (Proposed by Requesters 1 and 3)

    Rejection of claim 76, proposed by Requester 1, is **not adopted**.

    Rejection of claims 116-118, proposed by Requester 3, is **adopted**.

    Rejection of claims 64, 65, 68, 76, 87, 94, 95, 97, 99, 101, 102-108, 112-115,

proposed by Requester 3, is **not adopted**.

Ground 17: Obviousness over Amidi, JEDEC, and Vogt (Proposed by Requester 2)

    Proposed rejection of claim 76 is **adopted**.

Ground 18: Obviousness over Micron, Connelly and Dell 2 (Proposed by Requester 3)

    Proposed rejection of claims 1, 15, 28, and 39 is **adopted**.

Ground 19: Obviousness over Micron, Amidi, and Dell 2 (Proposed by Requester 3)

    Proposed rejection of claim 21 is **not adopted**.

Discussion of Rejections

Ground 1

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5.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and

JEDEC 21C. The proposed rejection is **not adopted**.

6.   With respect to claims 1, 15, and 28, Requester alleges that QBMA discloses "a circuit

mounted to the printed board, the circuit comprising a logic element and a register" as claimed.

Requester identified the QBM switch disclosed in QBMA on page 17 as the circuit or the logic

element (see Request 1 pp. 42-43). The QBM switch shown on page 17 is reproduced below.

As shown in the figure above, the QBM switch takes 8-bits (C[0,7]) + two strobe signals (DQS

C), and three control signals (Enable, SB, BE CLK) on the DIMM side of the interface as inputs.

In contrast, the claim requires "the logic element [to] receiv[e] a set of input control signals from

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the computer system, the set of input control signal comprising at least one row/column address

signal, bank address signals, and at least one chip-select signal." Thus, the claim requires the

logic element to receive a set of at least four signals: one row/column address signal, two bank

signals, and one chip-select signal. It is clear from the figure that none of the signals received by

the QBM switch corresponds to any of the set of input signals required by the claim.

7.   Requester 1 alleges that QBMA discloses RAS and CAS signals. However, these signals

are not address signals or a chip-select signal. Although Requester 1 also asserts, citing pages

17-20 and 23, that QBMA discloses a bank select signal which is supplied to the QBM switch,

Requester 1 has failed to identify the bank select signals allegedly taught by QBMA from any of

the figures on any of the cited pages. Requester 1 further alleges that the QBM controller shown

on page 24 provides address and control signals to the memory DIMM. While Requester 1 is

correct that address and control lines are shown on page 24, Requester 1 has failed to show how

page 24 of QBMA teaches the "logic element" limitation above.

8.   Requester 1 also alleges "that providing such input control signals to a logic element was

well known at the time of the invention" (see Request 1, p. 43). There is no evidence on the

record that it was well known to provide the recited set of input signals to a QBM switch at the

time of the invention. Based on the above allegation without evidence, Requester 1 concludes

that "it would have been obvious to one of ordinary skill in the art to provide such input control

signals to the logic element particularly given that such was standard in the industry at the time

of the invention." Again, Requester 1 has provided no evidence that providing a row/column

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address signal, bank address signals, and a chip-select signal to the QBM switch was standard in

the industry.

9.   With respect to claim 39, the claim recites an integrated circuit that comprises a logic

element, wherein the logic element receives bank address signals and at least one command

signal. As with the other independent claims, Requester 1 identified the QBM switch as the

logic element. However, as shown above, the QBM switch does not receive bank address signals

or a command signal as input.

10.   Requester 1 also alleges that the limitation "the at least one integrated circuit element

generating a plurality of output signals in response to the plurality of input signals, the plurality

of output signals comprising row address signals, column address signals, bank address signals,

command signals, and the first number of chip-select signals" is taught by the QBM switch

which "contains circuitry that takes address bits [0,7] from "C:DIMM connector side" and maps

to "A or B: memory chip side" address A[0,7] or B[0,7]" (see Request, p. 64). This allegation is

based on Requester's interpretation of C[0,7] signals, shown on page 17 of QBMA, as address

signals. While QBMA does not explicitly state whether C[0,7] is a set of address signals or data

signals, the Figure above shows that the set of 8-bit signals (C[0,7] is the only set of 8-bit signals

shown in the Figure) is associated with the two data strobe signals for circuitries A and B (DQS

C_A and DQS C_B). Thus, it is more likely than not that C[0,7] is a set of signal that represents 8

data bits, rather than address bits as asserted by Requester 1.

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Ground 2

11.   Requester 1 asserts that claims 1-17, 19, 21, and 23-51 are obvious over QBMA and Dell

2. The proposed rejection is **not adopted**.

12.   The Examiner initially notes that Requester 1's proposed rejection maps alleged

teachings of the two references applied (QBMA and Dell 2) to limitations of individual claims in

a claim chart without clearly ascertaining the differences between the prior art and the claims at

issue (step 2 of the *Graham* v. *John Deere Co.* obviousness analysis framework). The proposed

rejection does not make it clear as to which features from which references are to be applied in a

combination to make a system that teaches all of the limitations of the claims. For example, the

claim chart for claim 1, at pages 71-74 of the Request, maps every element of claim 1 to some

teaching in Dell 2 appearing to allege that claim 1 is anticipated by Dell 2. Yet, the proposed

rejection uses QBMA as the primary reference and Dell 2 as a secondary reference.

13.   With respect to claims 1, 15, and 28, Requester 1 alleges that the limitation "the logic

element receiving a set of input control signals from the computer system, the set of input control

signals comprising at least one row/column address signal, bank address signal, and at least one

chip-select signal" is taught by the combination of the QBM switch and Dell 2's logic circuit that

receives "a number of address inputs an a number of bank address signals from a memory

controller with said address input and bank address input signals corresponding to N bank

memory devices" and that it would have been obvious to combine the teachings. As discussed

above, the QBM switch does not receive any of the recited input signals. Dell 2 does not cure

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this deficiency because while the passage cited in Request 1 discloses a logic circuit receiving a

number of address input and a number of bank address signals, Dell 2 does not teach that the

logic circuit receives a chip-select signal.

14.   Requester 1 alleges that it would have been obvious to combine the teachings of QBMA

and Dell 2 to produce a logic element which receives input control signals including at least one

row/column address signal, bank address signals, and a chip-select signal to facilitate memory

domain translation. However, Requester 1 has not explained how adding address signals and a

chip-select signal as inputs to the QBM switch facilitates memory domain translation. QBMA

does not disclose the use of the QBM switch for memory domain translation. Memory modules

disclosed in QBMA do not appear to handle row/column address and bank signals through the

QBM switch. Thus, it makes little sense to redesign the modules by rerouting the address/bank

signals through the QBM switch to use the QBM switch for memory domain translation

application when Dell's invention can be use for that purpose without any redesign.

15.   Requester 1 also alleges that the limitation "the circuit generating a set of output control

signals in response to the set of input control signals corresponding to the first number of DDR

memory device arrange in the first number of ranks" is taught by both QBMA and Dell 2,

without making it clear whether the combined system uses QBMA's teaching or Dell's teaching.

As discussed above, the QBM switch does not generate addresses. As to Dell 2's disclosure, the

passage cited by Requester 1 that allegedly teaches this limitation (c8:20-27) is a textual

description of Figure 1A. Figure 1A shows remapping of address signal A12 as BA1. The rest

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of the address signals and the bank signal BA0 are used as they are. Therefore, Dell 2's circuit

does not "generate a set of output control signals in response to the set of input control signals."

To the extent that remapping of A12 as BA1 can be considered "generating an output signal,"

Dell 2 teaches generating an output control signal BA1, not "output control signals" as required

by the claims.

16.   Claims also require the circuit to "generat[e] and transmit[] a second command signal and

the set of output control signals to the plurality of memory devices" in response to a first

command signal and the set of input control signal. Again, Requester 1 does not make it clear

whether the combined circuit is to use QBMA's teaching or Dell's teaching with respect to this

limitation. Requester asserts that QBMA's disclosure that a QBM uses standard DDR

commands teaches this limitation. However, the claim specifically requires the circuit to

respond to a first command by generating a second command. QBMA does not specifically

disclose that a QBM generates and transmits commands in response to standard DDR commands

or that it generates standard DDR commands in response to commands received by the circuit.

Likewise, the passage in Dell 2 cited by Requester 1 does not disclose a circuit that generates and

transmits a command in response to another command as required by the claims.

17.   Claim 39 recites limitations that are similar to those of claim 1 discussed above. See the

discussion of claim 1 above.

Ground 3

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18.   Requester 1 asserts that claims 1-7, 9-11, 14-15, 18-21, 23-25, 28-34, 36-37, 40-43, 46,

and 51 are anticipated by Amidi. Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25,

27-29, 31-34, 36-39, and 41-45, and 50 are anticipated by Amidi. These rejections are **not**

adopted. All claims require a circuit that comprises a logic element and a register. Amidi does

not disclose a circuit that comprises a logic element with all of its limitations **and** a register.

Prior rejections relied on the same register (408, 418, or 608, all depicting the same register) to

teach the limitations of the logic element limitation and the register. After consideration of all of

the arguments presented, the Examiner concludes that reasonable interpretation of the claim

language, in view of the specification, requires a logic element that is separate and distinct from

a register. Thus, Amidi teaches a logic element with all of its required limitations without a

register, or a logic element without all of the required limitations and a register, but not both as

required. See discussion below (Response to Arguments).

19.   Rejection of claims 21, proposed by Requesters 1 and 2, is **not adopted**. Requester 1

alleges that paragraphs 37, 38, and 57 of Amidi disclose the claim limitation. These paragraphs

and Figures 4 and 6 appear disclose a register that stores input signals and transmit output signals

during both column and row access procedures. However, there is no specific disclosure that an

input signal stored during a row access procedure is stored for subsequent use during a column

access procedure. Requester 2 explains that Amidi teaches that since standard DDR memory

modules have only one set of address lines, two sets of addresses must be provided to access

certain types of cells and that Amidi's memory module stores the input signals to provide

column address signals on a separate cycle from the row address signals citing paragraph 61.

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However, Requester 2 fails to explain how paragraph 61 teaches the actual limitation "wherein

the configured to store an input signal of the set of input signal during a row access procedure for

subsequent use during a column access procedure." The cited paragraph does not disclose that

an input address signal stored during a row access procedure is retained for subsequent use

during a column access procedure from the cited pages.

Ground 4

20.   Requester 1 asserts that claims 1-21, 23-25, 27-34, 36-43, 45-48, 50, 51, and new claims

52-55, 57-59, 64-89, 92-108, and 112-118 are obvious over Amidi. Proposed rejection is **not**

adopted. See Ground 3 above.

21.   Requester 1 asserts that because the address signals supplied to the memory module via

the address bus includes Address[n:0] and BA[1:0], Amidi impliedly discloses that the set of

input control signals comprises "at least one row/column address signal, bank address signals,

and at least one chip-select signal" (Request 1, p. 128). Although the Examiner agrees that the

set of input control signals to the memory module comprises the recited signals, the claims

specifically require the "logic element" to receive those signals. Figure 6 clearly shows that only

the register 608 receives the bank address signals.

22.   Requester 1 further asserts that "[t]o the extent that [Amidi] does not explicitly disclose

that the set of input control signals comprises "at least one row/column address signal, bank

address signals, and at least one chip-select signal," it would have been obvious to one or

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ordinary skill in the art at the time of the invention to provide such control signals to the logic

element to improve the active bank/rank determination" (Request 1, p. 128). This is merely an

allegation without any reasoned analysis as to how and why providing "such control signals" to

CPLD would be obvious and improve the active bank/rank determination. These control signals

are received and handled by another element (register) in the module. Requester 1 does not

explain why one skilled in the art would move or duplicate the control signals so as to be

received by CPLD and how this improves the memory module. Conclusion of obviousness

requires an articulation of some reason with some rational underpinning to support the

conclusion.

23.   With respect to claims 16 and 17, Requester 1 asserts that "[o]ne of ordinary skill in the

art would have understood from the '152 publication that the command signal may be

transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned

explanation to support the assertion. Conclusion of obviousness requires more than a mere

conclusory statement.

24.   With respect to claim 21, the proposed rejection does not address the actual limitation of

the claim that requires storage of an input signal during a row access procedure for subsequent

use during a column access procedure.

Ground 5

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25.   Requester 1 asserts that claims 1-51 are obvious over Amidi in view of Dell 2. Proposed

rejection is **not adopted**. See Grounds 3 and 4 above. Requester 1 asserts that "[t]o the extent

that [Amidi] does not explicitly show that the logic element receives a bank address signal,

Requester submits that [Dell 2] makes up for such deficiency" (Request 1, p. 162). Requester 1

further explains that Dell 2 teaches a logic circuit that receives a number of bank signals at

c2:44-49 and concludes that it would have been obvious to combine the teachings of the

references to realize larger memory capacity at a lower cost. The proposed rejection is deficient

because it does not show how the combination results in a memory module that teaches all of the

limitations of the claims. Amidi also teaches a logic circuit (register) that receives a number of

bank signals. Thus, Dell 2's teaching as used in the proposed rejection does not add anything

that is not taught by Amidi. There is no explanation as to how Dell 2's teaching can be adopted

so that the combination teaches the logic element as well as the register.

26.   Proposed rejection of claims 16, 17, and 21 is **not adopted**. With respect to claims 16

and 17, see the discussion of these claims above.

27.   With respect to claim 21, Requester 1 points to c8:29-41 of Dell 2's specification that

teaches storing a re-mapped BA1 signal supplied at RAS time to re-send at CAS time. However,

Requester 1 does not make it clear how this teaching can be combined with Amidi to result in a

memory module of claim 21. Requester 1's proposed rejection provides mapping of teachings

from both Amidi and Dell 2 to different elements of claim 21, without providing any guidance as

to how the teachings from the two references are to be combined to result in a memory module

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that discloses all of the limitations of claim 21. Amidi discloses a memory module that uses the

column address bit A11 to determine the active rank (see paragraph 57). Amidi does not appear

to use a signal supplied during a row access procedure. It is not clear how Dell 2's teaching of

retaining the re-mapped BA1 signal can be applied in Amidi's memory module. Bank address

signals are not re-mapped in Amidi's memory module.

Ground 6

28.   Requester 2 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45,

and 50 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34, 36-39, 41-43, 45, and 50, is **adopted**.

29.   <u>Claims 1, 3-4, 6, 8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31, 32, 34, 36-39, 41-43, 45, and</u>

<u>50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of</u>

<u>JEDEC 21-C.</u>

30.   With respect to claim 1, Amidi discloses **a memory module (Figure 4) connectable to a**

computer system, the memory module comprising:

    a printed circuit board (see Figure 4, 400);

    a plurality of double data rate (DDR) memory devices (404) mounted to the printed

circuit board, the plurality of memory devices having a first number of memory devices

arranged in a first number of ranks (see Figure 4, the module has four ranks);

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a circuit mounted to the printed circuit board, the circuit comprising a logic element (see Figure 6, CPLD 604 and register 608), **the logic element receiving a set of input control signals** (see Figure 6, the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and signals) **from the computer system, the set of input control signals comprising at least one row/column address signal (Add[n:0]), bank address signals (BA[1:0]), and at least one chip select signal (cs0), the set of input control signals corresponding to a second number of memory devices arranged in a second number of ranks, the second number of memory devices smaller than the first number of memory devices and the second number of ranks less than the first number of ranks** (see paragraphs 10-12, Amidi's invention is a transparent four rank module fitting into a memory socket meant for a two rank module), **the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks** (see Figure 6 and paragraph 52, "CPLD also ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules. For example, CPLD 604 generates rsc2 and rcs3 ..."); **and**

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> **a phase-lock loop device (412) mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of memory devices, the logic element, and the register.**

31.   However, Amid does not specifically disclose a register that is separate and distinct from the logic element (604 and 608) above. On the other hand, JEDEC 21-C discloses a DDR SDRAM Registered DIMM Design Specification that uses two registers (see JEDEC 21-C, p. 4.20.4-18). Adopting the JEDEC DIMM design would involve replacing Register 608 with two registers, Register 1 and Register 2 as specified on p. 4.204.-18. In the resulting JEDEC compliant design, the logic element limitation is taught by the combination of CPLD 604 (row/column address signal Add(n), chip select signals cs0 and cs1) and JEDEC Register 2 (bank address signals BA0 and BA1). The register limitation is taught by Register1.

32.   It would have been obvious to one of ordinary skill in the art, having the teachings of Amidi and JEDEC 21-C before him at the time the invention was made, to design Amidi's DIMM according to the JEDEC standard to have a marketable memory module that conforms to the industry standard.

33.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals (see Figure 4, cs0 and cs1) and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals (rcs0a-rcs3a).**

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34.   With respect to claim 4, **the first number of chip-select signals is two and the second
number of chip-select signals is four** (see the discussion of claim 3 above).

35.   With respect to claim 6, **the logic element comprises an application-specific
integrated circuit, a field-programmable gate array, a custom-designed semiconductor
device, or a complex programmable-logic device** (Figure 6, CPLD).

36.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and
the logic element are portions of a single component** (these are all portions of a single DIMM
which is a component of a personal computer).

37.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first
set of DDR memory devices on a first side of the printed circuit board, a second set of DDR
memory devices on the first side of the printed circuit board** (Figure 4A, ranks 0 and 2 are on
the front side), **a third set of DDR memory devices on a second side of the printed circuit
board, and a fourth set of DDR memory devices on the second side of the printed circuit
board** (Figure 4B, ranks 1 and 3 are on the back side), **the DDR memory devices of the second
set spaced from the DDR memory devices of the first set, the DDR memory devices of the
fourth set spaced from the DDR memory devices of the third set** (this is inherent as two
physical devices cannot occupy the same space at the same time).

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38.   With respect to claim 11, **the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side** (see paragraph 34, the devices are stacked on the front and the back side).

39.   With respect to claims 15 and 28 see the discussion of claim 1 above.

40.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

41.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Figure 6 and paragraph 52).

42.   With respect to claim 19, **the command signal comprises a refresh command signal** (see paragraph 52).

43.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

44.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command

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for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see Figure 6, register).

45.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (Figure 6, CPLD).

46.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see Figure 6).

47.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

48.   With respect to claims 31 and 32, see the discussion of claim 3 above.

49.   With respect to claim 34, **the first number of ranks is four and the second number of ranks is two** (paragraph 41).

50.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (paragraph 52).

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51.   With respect to claim 37, **the input command signal is a precharge signal and the
output command signal is a precharge signal** (paragraph 52).

52.   With respect to claim 38, **the input command signal is a read signal or a write signal
and the output command signal is a read signal or a write signal**. See the discussion of claim
37 above.

53.   With respect to claim 39, see claims 1 and 3 above.

54.   With respect to claims 10 and 11, spacing of memory devices is also an obvious matter of
design choice subject to constraints imposed by various practical engineering, manufacturing,
marketing, cost, and other considerations.

55.   Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**. With respect to claims
7, 9, 33, and 44, the combination as applied discloses only one register that does not receive a
bank address. With respect to claim 21, see the discussion of this claim above.

56.   The Examiner rejects claims 12-14, 40, and 46-49 as being obvious over Amidi in view
of JEDEC standards.

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57.   <u>Claims 12-14, 40, and 46-49 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of JEDEC 21-C.</u>

58.   With respect to claims 12, 13, and 46-48, see claim 10 above.

59.   With respect to claims 14 and 49, see Amidi, paragraph 41.

60.   With respect to claim 40, see Amidi, paragraph 41. See also, Figures 6A and 6B, CLPD input and output signals.

61.   Requester 2 asserts that claims 52-75 and 77-118 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 52, 61-71, 75, 77-91, 94, 96, 98, 100, and 102-118 is **adopted**.

62.   <u>Claims 52, 61-65, 67-71, 75, 77-91, 94, 96, 98, 100, and 102-118 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of JEDEC 21-C.</u>

63.   With respect to claim 52, **the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip- select signals of the set Of output control signals (see claim 1 above), the first number of chip-select signals generated by the logic element equal to the first number of ranks (see Amidi, Figure 6,**

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CPLD 604, rcs0-4), **and the at least one chip-select signal of the set of input control signals**

comprises a second number of chip-select signals equal to the second number of ranks (cs0,

cs1).

64.   With respect to claim 61, **the plurality of DDR memory devices has at least one**

attribute selected from a group consisting of: a number of row address bits per DDR

memory device, a number of column address bits per DDR memory device, a number of

bank address bits per DDR memory device, a number of DDR memory devices, a data

width per DDR memory device, a memory density per DDR memory device, a number of

ranks of DDR memory devices, and a memory density per rank,

the memory module further comprising a read-only non-volatile memory device

storing data accessible to the computer system (Amidi, Figure 4A, SPD 414; JEDEC, p. 4.20-

4.68, Serial PD definition), **wherein the data characterizes the plurality of DDR memory**

devices as having at least one value of the at least one attribute (SPD Definition, bytes #5 and

#31, Number of Physical Banks on DIMM and Module Bank Density) **that is different from an**

actual value of the at least one attribute of the plurality of DDR memory devices (see

Bagherzadeh Declaration, ¶ 48, "One skilled in the art would understand that in order to appear

transparent to the computer system, which generally cannot use a four rank memory module, the

SPD device taught by Amidi must store data characterizing the module as a two rank module of

different memory density").

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65.   With respect to claim 62, **the at least one attribute comprises the number of ranks of**

DDR memory devices and the memory density per rank (SPD Definition, byte #31).

66.   With respect to claim 63, **the data characterizes the plurality of DDR memory devices**

as having fewer ranks of DDR memory devices than the plurality of DDR memory devices

actually has, and as having a greater memory density per rank than the plurality of DDR

memory devices actually has (see claims 57 and 61).

67.   With respect to claim 64, **the logic element comprises means for generating rank-**

selecting signals of the set of output control signals for performing successive read accesses

from different ranks of DDR memory devices of the plurality of DDR memory devices (see

Amidi, Figure 5 and paragraph 43).

68.   With respect to claim 65, **the logic element comprises means for generating rank-**

selecting signals of the set of output control signals for performing back-to-back adjacent

read commands which cross DDR memory device boundaries (see Amidi, Figure 5 and

paragraph 43).

69.   With respect to claims 67 and 82, **the logic element is responsive at least in part to the**

bank address signals and the at least one chip-select signal of the set of input control signals

by generating a number of rank-selecting signals of the set of output control signals that is

greater than double or equal to double the number of chip-select signals of the set of input

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control signals (see claim 52).

70.   With respect to claim 68, **the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device** (see Amidi, Figure 6), **wherein the memory module is operable for use in a server system** (DIMM memory modules can be used in a server system or any other system that can accept DIMM modules).

71.   With respect to claims 69, 102, and 103, see claim 64.

72.   With respect to claims 70, 78, 83, 88, 104, and 105, see claim 65.

73.   With respect to claim 71, **the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation** (these limitations are inherent in any functioning DIMM with multiple ranks).

74.   With respect to claims 75, 80, 85, and 90, see claim 61 above.

75.   With respect to claims 77 and 87, **the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input signals by generating a number of rank-selecting signals of the set of output signals that is greater**

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than double or equal to double the number of chip-select signals of the set of input signals

(see claim 52 above).

76.   With respect to claims 79, 84, and 89, **the plurality of DDR memory devices and the**

logic element are timed to clock signals from the phase-lock loop device (see claim 57).

77.   With respect to claims 81, 86, and 91, **the one or more attributes comprise the number**

of ranks of DDR memory devices and the memory density per rank and the data

characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory

devices than the plurality of DDR memory devices actually has, and as having a greater

memory density per rank than the plurality of DDR memory devices actually has (see claim

63).

78.   With respect to claims 94, 96, 98, and 100, **the logic element receives a bit of a non-**

bank address signal of the set of input control signals (Figure 6, cs0 and cs1) **in conjunction**

with an activate command (activate command is used to open a row in a particular bank for

read or write) **and uses the bit to generate rank-selecting signals** (see Figure 5, cs0 and cs1

bits are used to select an active bank) **for a subsequent read or write command.**

79.   With respect to claims 106, 107, and 108, **the logic element comprises means for using**

at least one address bit received by the memory module during an activate command

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operation to generate chip-select signals for a read or write command operation, the read

or write command operation subsequent to the activate command operation (see claim 94).

80.   With respect to claims 109-111, **the memory module comprises means for**

characterizing the plurality of DDR memory devices as having one or more attributes that

are different from actual attributes of the plurality of DDR memory devices (see claim 61).

81.   With respect to claims 112-114, **the logic element comprises means for performing**

sequential and combinatorial logic procedures (see Amidi, Figure 8) **to generate rank-**

selecting signals of the set of output control signals (see claim 94).

82.   With respect to claims 115 and 117, **the first command signal is a row access**

command signal, and the logic element uses sequential and combinatorial logic procedures

with at least one address bit of the set of input control signals (see Amidi, Figure 8) **and the**

at least one chip-select signal to generate chip-select signals for the second command signal

(see claim 94).

83.   With respect to claims 116 and 118, **the logic element further uses the sequential and**

combinatorial logic procedures with the at least one address bit (see Figure 8) **to generate**

chip-select signals for a column access command signal subsequent to the row access

command signal, wherein the memory module receives a second column access command

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signal between receiving the row access command signal and the subsequent column access command signal (see claim 94).

84.   Proposed rejection of claims 53-60, 66, 72-74, 92-93, 95, 97, 99, and 101, is **not adopted**.

85.   With respect to claims 53-56 and 58-60, Amidi does not disclose that the register receive and buffers the bank address signal. Although Amidi does disclose a register that receives bank address signals, the rejection of the parent claim 1, relies on Register2 of JEDEC to teach the claimed "logic element" with Register 1 teaching the "register" limitation of the claims. Register 1 of JEDEC does not receive bank address signals.

86.   With respect to claims 57-60, Amidi does not disclose that the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device. In the combination, the generation of chip-select signals (CPLD output signals) is in response to the clock signals that are supplied to the PLL, not received from the PLL device.

87.   With respect to claims 66, Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals.

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88.   With respect to claims 72-74, the claims require generation of rank-selecting signal that select none of the ranks and two ranks. Amidi and JEDEC combination does not disclose these no-rank and two-rank selecting signals.

89.   With respect to claims 92 and 93, the claims require the logic element not to operate in response to row/column address bits (A_0 - A_n). The logic element of the combination used to reject the parent claims does operate in response to A_0, A_1, and A_{10}.

90.   With respect to claims 95, 99 and 101, the Amidi and JEDEC combination does not teach that the bank address signals are used to generate rank-selecting signals. In the combination, chip-select and A_n signals are used to generate rank-selecting signals.

91.   With respect to claim 97, in the proposed combination bank address signals are not used to generate the rank-selecting signals for a subsequent read or write command.

92.   Requester 1 asserts that claims 56, 60-63, 90-91, and 109-111 are obvious over Amidi in view of JEDEC standards. Proposed rejection of claims 61-63, 90-91, and 109-111 is **adopted**. See above. Proposed rejection of claims 56 and 60 is **not adopted**. See above.

Ground 7

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93.   The Examiner notes that Requester has failed to properly raise a substantial new question of patentability based on Murdocca and Dell 2 combination. Nevertheless, Requester's proposed rejection based on Murdocca and Dell 2 has been considered on the merit as discussed below.

94.   Requester 1 asserts that claims 1-11, 14, 15, 19, 21, 23-25, 28-34, 36, 39-42, and 51 are obvious over Murdocca and Dell 2. The proposed rejection is **not adopted**.

95.   Requester 1 identified Murdocca's 1-to-2 decoder, shown on page 250, as the logic element that receives a set input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signal, and at least one chip select signal. Requester asserts that it would have been obvious to combine the method for constructing larger RAMs from smaller RAMs disclosed in Murdocca with the logic element disclose in Dell 2 that receives a number of address inputs and a number of bank address signals. However, Requester fails to explain how the proposed combination would result in the claimed logic element. For example, Requester does not explain how Murdocca's 1-to-2 decoder that takes one address signal as input and a chip select signal as a control signal to produce two output signals can accommodate bank address signals and how the output bank address signals are used to construct the claimed circuit. A combination proposed cannot be just a patchwork of different circuit elements that teach different limitations of the claim. In addition to containing all of the limitations of the claim, the proposed combined circuit must make sense in terms of its overall structure and function. It must work as a unit that comprises all of the claimed structural features and be functional as a unit in the manner claimed.

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96.   Moreover, all claims require a circuit that "responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signal to the plurality of memory devices." Requester 1 asserts that Murdocca's teaching of a 1-to-2 decoder and Dell 2's disclosure at c2:44-49 and c8:32-41 disclose the circuit. The 1-to-2 decoder taught by Murdocca is an address decoder. It does not respond to a command. Nor does it generate any command. Dell 2's circuit that remaps addresses does not respond to a command by generating another command as required by the claims. Therefore, the proposed combination does not teach a circuit that responds to a first command by generating and transmitting a second command as required by the claims.

Ground 8

97.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are anticipated by Dell 1. Proposed rejection is **not adopted**. Claims are anticipated when a single reference teaches all of the limitations of the claims. Requester 2's proposed rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C "establishes that a DIMM has a PLL mounted to the printed circuit board" (Request 2, p. 63). However, Requester 2 fails to explain where in Dell 1 a PLL is taught or how JEDEC 21-C's teaching of a PLL is attributable to Dell 1.

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Ground 9

98.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are obvious over Dell 1 in view of JEDEC standards. Proposed rejection of claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31-32, 36-39, 41-43, 45, and 50 is **adopted**.

99.   Claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31-32, 36-39, 41-43, 45, and 50 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Dell 1 in view of JEDEC 21-C.

100.   With respect to claim 1, Dell 1 discloses **a memory module** (see Figure 3, DIMM with two banks of memory chips) **connectable to a computer system, the memory module comprising:**

    a printed circuit board (see c1:23-39, DIMMs for IBM PCs are implemented with PCBs; see JEDE 21-C);

    a plurality of memory devices mounted to the printed circuit board (see Figure 3, 4Mx4 chips 40x), **the plurality of memory devices having a first number of memory devices arranged in a first number of ranks** (see Figure 3; see also c1:60-67, 36 devices in two banks);

    a circuit mounted to the printed circuit board, the circuit comprising a logic element and, the logic element receiving a set of input control signals (see Figure 3, the DIMM receives RAS, CAS, OE, WE, and A0-A11 signals) **from the computer system, the set of input control signals comprising at least** four address signals (A0-A11), **the set of input control signals corresponding to a second number of memory devices arranged in a second number**

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of ranks (see c1:46-53, 60-67, nine devices in one bank), **the second number of memory**

devices smaller than the first number of memory devices and the second number of ranks

less than the first number of ranks, the circuit generating a set of output control signals in

response to the set of input control signals (see Figure 3, the circuit generates two CA0, two

WE0, two OE0, RAS A, RAS B signals, and two sets of address signals A0-A10), **the set of**

output control signals corresponding to the first number of memory devices arranged in

the first number of ranks (the set of output control signals correspond to 36 4Mx4 devices

arranged in two banks), **wherein the circuit further responds to a first command signal** (CBR

refresh for one bank of 8Mx8 memory devices) **and the set of input control signals from the**

computer system by generating and transmitting a second command signal and the set of

output control signals to the plurality of memory devices (see c6:22-29, Dell 1 disclose

generating a CBR refresh command to both banks of 4Mx4 memory devices by activating two

RAS signals), **the first command signal and the set of input control signals corresponding to**

the second number of ranks and the second command signal and the set of output control

signals corresponding to the first number of ranks.

101.   However, Dell 1 does not specifically disclose that 1) the memory devices are **double-**

data-rate (DDR) devices, 2) the circuit comprises **a register,** 3) the address signals comprise at

least **one row/column address signal, bank address signals, and at least one chip-select**

signal, and 4) the memory module comprises **a phase-lock loop device mounted to the printed**

circuit board, the phase-lock loop device operatively coupled to the plurality of memory

devices, the logic element, and the register. On the other hand, JECED 21-C discloses 1) the

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use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20.4-
18, Register 1), 3) address signals that comprise at least one row/column signal (p. 4.20.4-18,
Register 2, input signal A0), bank address signals (BA0-BA1), at least one chip-select signal
(S0), and 4) a phase-lock loop device mounted to the printed circuit board (p. 4.20.4-29) that is
operatively coupled to other elements of the module (see p. 4.20.4-17).

102.   It would have been obvious to one of ordinary skill in the art, having the teachings of
Dell 1 and JEDEC 21-C before him at the time the invention was made, to design the DIMM of
Dell 1 in compliance with the JEDEC standard to make it compatible with computer systems that
expect DIMMs installed in the system to be standard compliant.

103.   With respect to claim 3, **the set of input control signals comprises a first number of
chip-select signals** (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip
select signal lines; a set of input signals with four chip select signals comprise two chip select
signals) **and wherein the set of output control signals comprises a second number of chip-
select signals greater than the first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-
12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip
select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3,
would generate four output signal lines, RS0-RS3).

104.   With respect to claim 4, **the first number of chip-select signals is two and the second
number of chip-select signals is four** (see the discussion of claim 3 above).

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105.   With respect to claim 6, **the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device** (see Dell 1, c4:28-29).

106.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

107.   With respect to claims 15 and 28 see the discussion of claim 1 above.

108.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

109.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Dell 1, c6:28-30, CBR refresh command refreshes both banks concurrently).

110.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

111.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

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112.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Dell 1 and JEDEC), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address bit that is latched during the activate command for the selected bank, with no other attribute), **and the circuit is configured to store the row address bit during an activate command for a selected bank** (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an activate command to activate a row requires row address bits).

113.   With respect to claims 24, 29 and 41, **the logic element comprises an application-specific integrated circuit** (see Dell 1, c4:28-29), **a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.**

114.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices** (see JEDEC 21-C, p. 4.20.4-10).

115.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (see the discussion of claim 8 above).

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116.   With respect to claims 31 and 32, see the discussion of claim 3 above.

117.   With respect to claim 36, **the input command signal is a refresh signal and the output command signal is a refresh signal** (Dell 1, c6:28-30).

118.   With respect to claim 37, although Dell 1 and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal**, they do disclose receiving input commands and generating output commands as claimed. One of ordinary skill in the art would realize that Dell 1's high density DIMM with RAS address re-mapping must work for all commands, not just the ones specifically mentioned in the disclosure.

119.   With respect to claim 38, Dell 1 and JEDEC 21-C discloses that **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal**. See the discussion of claim 37 above.

120.   With respect to claim 39, see claims 1 and 3 above.

121.   Proposed rejection of claims 7, 9, 21, 33, and 44 is **not adopted**. With respect to claims 7, 9, 33, and 44, the combination as applied discloses only one register that does not receive a bank address. With respect to claim 21, Requester asserts that JEDEC 21-C "teaches that all input control signals to DIMM pass through the register, which stores them internally before re-

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driving them, including during a column access procedure" citing pages 40.20.4-67 and 40.20.4-

11 (Request 2, pp. 242-243). However, Requester fails to explain how those pages teach the

actual limitation "wherein the configured to store an input signal of the set of input signal during

a row access procedure for subsequent use during a column access procedure." The Examiner

cannot ascertain which input signal stored during a row access procedure is retained for

subsequent use during a column access procedure from the cited pages.

Ground 10

122.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are anticipated by Wong. Proposed rejection is **not adopted**. Claims are anticipated

when a single reference teaches all of the limitations of the claims. Requester's proposed

rejection relies extensively on JEDEC 21-C to teach many of the limitations of the claims. For

example, all claims require a phase locked loop. Requester alleges that JEDEC 21-C "explains

that a DIMM has a PLL mounted to the printed circuit board" (Request, p. 674). However,

Requester fails to explain where in Wong a PLL is taught or how JEDEC 21-C's teaching of a

PLL is attributable to Wong.

Ground 11

123.   Requester 2 asserts that claims 1, 3-4, 6-9, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are obvious over Wong in view of JEDEC standards. Proposed rejection of claims 1, 3-4,

6, 8, 15, 18-20, 22, 24-25, 27-29, 31-30, 36-39, 41-43, 45, and 50, is **adopted**.

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124.   Claims 1, 3-4, 6, 8, 15, 18-20, 22, 24-25, 27-29, 31-30, 36-39, 41-43, 45, and 50 are

rejected under 35 U.S.C. 103(a) as being as being unpatentable over Wong in view of JEDEC

21-C.

125.   With respect to claim 1, Wong discloses **a memory module** (see Figure 3, DIMM with

two banks of memory chips) **connectable to a computer system, the memory module**

comprising:

  a printed circuit board (see Figure 3, 1000);

  a plurality of memory devices mounted to the printed circuit board (Figure 3, 1002),

the plurality of memory devices having a first number of memory devices arranged in a

first number of ranks (1012 and 1012);

  a circuit mounted to the printed circuit board, the circuit comprising a logic element

and, the logic element receiving a set of input control signals (see Figures 4A and 4B) **from**

the computer system, the set of input control signals comprising at least four address signals

(A0-A13), **the set of input control signals corresponding to a second number of memory**

devices arranged in a second number of ranks (see c2:1-10, Wong discloses that a separate

bank of memory typically requires at minimum either a unique RAS or unique CAS for each

bank; see Figure 4, the input signal set contains one RAS and one CAS, i.e., a set for a single

bank), **the second number of memory devices smaller than the first number of memory**

devices and the second number of ranks less than the first number of ranks, the circuit

generating a set of output control signals in response to the set of input control signals (see

Figure 4, the circuit generates two CAS, two WE, two RAS signals, and two sets of address ·

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signals A0-A12), **the set of output control signals corresponding to the first number of
memory devices arranged in the first number of ranks** (the set of output control signals
correspond to 36 4Mx4 devices arranged in two banks), **wherein the circuit further responds
to a first command signal and the set of input control signals from the computer system by
generating and transmitting a second command signal and the set of output control signals
to the plurality of memory devices** (c2:30-34, CBR refresh for both banks), **the first command
signal and the set of input control signals corresponding to the second number of ranks and
the second command signal and the set of output control signals corresponding to the first
number of ranks.**

126.   However, Wong does not specifically disclose that 1) the memory devices are **double-
data-rate (DDR)** devices, 2) the circuit comprises **a register,** 3) the address signals comprise at
least **one row/column address signal, bank address signals, and at least one chip-select
signal,** and 4) the memory module comprises **a phase-lock loop device mounted to the printed
circuit board, the phase-lock loop device operatively coupled to the plurality of memory
devices, the logic element, and the register.** On the other hand, JECED 21-C discloses 1) the
use of DDR SDRAM devices in a DIMM (see Title page), 2) a register for a DIMM (p. 4.20.4-
18, Register 1), 3) address signals that comprise at least one row/column signal (p. 4.20.4-18,
input signal A0), bank address signals (BA0-BA1), at least one chip-select signal (S0), and 4) a
phase-lock loop device mounted to the printed circuit board (p. 4.20.4-29) that is operatively
coupled to other elements of the module (see p. 4.20.4-17).

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127.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Wong and JEDEC 21-C before him at the time the invention was made, to design the DIMM of

Wong in compliance with the JEDEC standard to make it compatible with computer systems that

expect DIMMs installed in the system to be standard compliant.

128.   With respect to claim 3, **the set of input control signals comprises a first number of

chip-select signals** (see JEDEC 21-C, p. 4.20.4-6, JEDEC discloses four pins, S0-S3, for chip

select signal lines; a set of input signals with four chip select signals comprise two chip select

signals) **and wherein the set of output control signals comprises a second number of chip-

select signals greater than the first number of chip-select signals** (see JEDEC 21-C, p. 4.20.4-

12, a JEDEC DIMM with two input chip select lines, S0 and S1, generate RS0 and RS1 chip

select output lines, indicating that a JEDEC DIMM with four input chip select lines, S0-S3,

would generate four output signal lines, RS0-RS3).

129.   With respect to claim 4, **the first number of chip-select signals is two and the second

number of chip-select signals is four** (see the discussion of claim 3 above).

130.   With respect to claim 6, **the logic element comprises an application-specific

integrated circuit, a field-programmable gate array, a custom-designed semiconductor

device, or a complex programmable-logic device** (see Wong, c2:41-44).

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131.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and the logic element are portions of a single component** (these are all portions of a single DIMM which is a component of a personal computer).

132.   With respect to claims 15 and 28 see the discussion of claim 1 above.

133.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

134.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Wong, c3:30-34).

135.   With respect to claim 19, **the command signal comprises a refresh command signal** (see the discussion of claim 18 above).

136.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

137.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM such as the one disclosed by Wong and JEDEC), **the set of input signals comprises a density bit which is a row address bit** (the specification describes the density bit simply as a row address

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bit that is latched during the activate command for the selected bank, with no other attribute),

and the circuit is configured to store the row address bit during an activate command for a

selected bank (see JEDEC 21-C, p. 4.20.4-11, row address bits are stored in a register and an

activate command to activate a row requires row address bits).

138.   With respect to claims 24, 29 and 41, **the logic element comprises an application-**

specific integrated circuit, a field-programmable gate array, a custom-designed

semiconductor device, or a complex programmable-logic device (see Wong, c2:41-42).

139.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of**

row/column address signals received and buffered by the register and sent from the

register to the plurality of DDR memory devices (see JEDEC 21-C, p. 4.20.4-10).

140.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the**

register, and the logic element are portions of a single component (see the discussion of

claim 8 above).

141.   With respect to claims 31 and 32, see the discussion of claim 3 above.

142.   With respect to claim 36, **the input command signal is a refresh signal and the output**

command signal is a refresh signal (Wong, c2:28-34).

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143.   With respect to claim 37, although Wong and JEDEC 21-C do not specifically mention that **the input command signal is a precharge signal and the output command signal is a precharge signal**, they do disclose receiving input commands and generating output commands as claimed. One of ordinary skill in the art would realize that Wong's memory expansion module including multiple memory banks and a bank control circuit must work for all commands, not just the ones specifically mentioned in the disclosure.

144.   With respect to claim 38, Wong and JEDEC 21-C discloses that **the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal**. See the discussion of claim 37 above.

145.   With respect to claim 39, see claims 1 and 3 above.

146.   Proposed rejection of claims 21 is **<u>not adopted</u>**. Requester asserts that JEDEC 21-C "teaches that all input control signals to DIMM pass through the register, which stores them internally before re-driving them, including during a column access procedure" citing pages 40.20.4-67 and 40.20.4-14 (Request, pp. 856-857). However, Requester fails to explain how those pages teach the actual limitation "wherein the configured to store an input signal of the set of input signal during a row access procedure for subsequent use during a column access procedure." The Examiner cannot ascertain which input signal stored during a row access procedure is retained for subsequent use during a column access procedure from the cited pages.

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Ground 12

147.   Requester 3 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are obvious over Micron in view of Connelly. Proposed rejection of claims 1, 3-4, 6-8,

10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

148.   Claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are

rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connelly.

149.   With respect to claim 1, Micron discloses **a memory module** (Figures 1-3) **connectable
to a computer system, the memory module comprising:**

   a printed circuit board (see Figure 1);

   a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted
to the printed circuit board, the plurality of memory devices having a first number of
memory devices arranged in a first number of ranks** (see Figure 4, the module has two
ranks);

   **a circuit mounted to the printed circuit board, the circuit comprising a logic element
and** (p. 4, Figure 4, Register U37) **a register** (Register U38), **the logic element receiving a set
of input control signals** (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #)
**from the computer system, the set of input control signals comprising at least one
row/column address signal (A0-A12), bank address signals (BA0, BA1), and at least one
chip select signal (S0); and**

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a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,
the phase-lock loop device operatively coupled to the plurality of memory devices, the logic
element, and the register.**

150.   However, Micron does not specifically disclose that "the set of input control signals
corresponding to a second number of memory devices arranged in a second number of ranks, the
second number of memory devices smaller than the first number of memory devices and the
second number of ranks less than the first number of ranks, the circuit generating a set of output
control signals in response to the set of input control signals, the set of output control signals
corresponding to the first number of memory devices arranged in the first number of ranks,
wherein the circuit further responds to a first command signal and the set of input control signals
from the computer system by generating and transmitting a second command signal and the set
of output control signals to the plurality of memory devices, the first command signal and the set
of input control signals corresponding to the second number of ranks and the second command
signal and the set of output control signals corresponding to the first number of ranks."

151.   On the other hand, Connolly discloses a DIMM that receives a set of input control signals
(Figure 3, RAS, CAS, OE, WE, A0-A11), **the set of input control signals corresponding to a
second number of memory devices arranged in a second number of ranks** (see Figure 2,
there are nine devices in one rank), **the second number of memory devices smaller than the
first number of memory devices and the second number of ranks less than the first number
of ranks** (see Figure 3, there are 36 devices in two ranks), **the circuit generating a set of output**

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control signals in response to the set of input control signals (see Figure 3, the circuit generates two CA0, two WE0, two OE0, RAS A, RAS B signals, and two sets of address signals A0-A10), **the set of output control signals corresponding to the first number of memory devices arranged in the first number of ranks**(the set of output control signals correspond to 36 4Mx4 devices arranged in two banks), **wherein the circuit further responds to a first command signal** (CBR refresh for one bank of 8Mx8 memory devices) **and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices** (see c6:46-49, Connolly discloses generating a CBR refresh command to both banks of 4Mx4 memory devices by activating two RAS signals), **the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks.**

152.   It would have been obvious to one of ordinary skill in the art, having the teachings of Micron and Connolly before him at the time the invention was made, to modify the design the DIMM of Micron to incorporate Connolly's technique for converting system signals from one address configuration to a different address configuration, to be able to use lower capacity memory devices which can be much cheaper (see Connolly, c1:38-63).

153.   With respect to claim 3, **the set of input control signals comprises a first number of chip-select signals** (see Micron, Figure 4, register input signal S0) **and wherein the set of**

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output control signals comprises a second number of chip-select signals greater than the

first number of chip-select signals (register output signals S0 and S1).

154.   With respect to claim 4, Micron and Connolly do not specifically disclose that **the first**

number of chip-select signals is two and the second number of chip-select signals is four.

However, it would have been obvious to one of ordinary skill in the art to add two additional

chip select signals to design a module with more memory banks in order to increase the memory

capacity of the module.

155.   With respect to claim 6, **the logic element comprises an application-specific**

integrated circuit, a field-programmable gate array, a custom-designed semiconductor

device, or a complex programmable-logic device (see Connolly, Figure 4, ASIC LOGIC 46).

156.   With respect to claim 7, **the bank address signals of the set of input control signals**

are received by both the logic element and the register (see the rejection of claim 1).

157.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and**

the logic element are portions of a single component (these are all portions of a single DIMM

which is a component of a personal computer).

158.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first**

set of DDR memory devices on a first side of the printed circuit board (Micron, Figure 7,

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U1-U10; see also Figure 8, U1-U6), **a second set of DDR memory devices on the first side of**

the printed circuit board (Figure 7, U11-U18; Figure 8., U7-U12), **a third set of DDR**

memory devices on a second side of the printed circuit board (Figure 7, U19-U28; Figure 8,

U21-U26), **and a fourth set of DDR memory devices on the second side of the printed**

circuit board (Figure 7, U29, U36; Figure 8, U28-U33), **the DDR memory devices of the**

second set spaced from the DDR memory devices of the first set, the DDR memory devices

of the fourth set spaced from the DDR memory devices of the third set (see Figure 7 and 8).

159.   With respect to claim 11, **the DDR memory devices of the second set are spaced from**

the DDR memory devices of the first set in a direction along the first side and the memory

devices of the fourth set are spaced from the memory devices of the third set in a direction

along the second side (see Figure 7 and 8).

160.   With respect to claims 15 and 28 see the discussion of claim 1 above.

161.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

162.   With respect to claim 18, **the command signal is transmitted to two ranks of the first**

number of ranks at a time (see Connolly, c6:46-49, CBR refresh command refreshes both

banks concurrently).

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163.   With respect to claim 19, **the command signal comprises a refresh command signal**
(see the discussion of claim 18 above).

164.   With respect to claim 20, **the command signal is transmitted to the two ranks of the
first number of ranks concurrently** (see claim 18 above).

165.   With respect to claim 22, **the command signal comprises a read command signal or a
write command signal** (read and write commands are inherent in any functioning DIMM such
as the one disclosed by Micron and Connolly; see also Micron Table 6), **the set of input signals
comprises a density bit which is a row address bit** (the specification describes the density bit
simply as a row address bit that is latched during the activate command for the selected bank,
with no other attribute), **and the circuit is configured to store the row address bit during an
activate command for a selected bank** (Micron, Figure 4, row address bits are stored in a
register and an activate command to activate a row requires row address bits).

166.   With respect to claims 24, 29 and 41, **the logic element comprises an application-
specific integrated circuit** (Connolly, Figure 4), **a field-programmable gate array, a custom-
designed semiconductor device, or a complex programmable-logic device.**

167.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of
row/column address signals received and buffered by the register and sent from the
register to the plurality of DDR memory devices** (Micron, Figure 4).

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168.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the**

register, and the logic element are portions of a single component (see the discussion of

claim 8 above).

169.   With respect to claims 31 and 32, see the discussion of claim 3 above.

170.   With respect to claims 33 and 44, **the register receives the bank address signals and**

the input command signal of the set of input control signals (Micron, Figure 4).

171.   With respect to claim 36, **the input command signal is a refresh signal and the output**

command signal is a refresh signal (Connolly, c6:46-49).

172.   With respect to claim 37, **the input command signal is a precharge signal and the**

output command signal is a precharge signal (Micron, Table 6).

173.   With respect to claim 38, **the input command signal is a read signal or a write signal**

and the output command signal is a read signal or a write signal (Micron, Table 6).

174.   With respect to claim 39, see claims 1 and 3 above.

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175.   Proposed rejection of claims 9 and 21 is **not adopted**. With respect to claim 9, the combination as applied discloses only one register. With respect to claim 21, see the discussion of this claim below.

176.   The Examiner rejects claims 26 and 35 as being obvious over Micron in view of Connelly.

177.   <u>Claims 26 and 35 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connelly.</u>

178.   With respect to claim 26, Connelly discloses **that the logic element** (see Micron, Figure 8, one of the two registers) **receives the bank address signals and the command signal from the computer system and the register** (the other register) **receives the bank address signals and the command signal from the computer system.**

179.   With respect to claim 35, Connelly discloses a memory module where **the first number of ranks is two and the second number of ranks is one** (see Connelly, c4:9-32).

180.   Requester 3 asserts that claims 52-118 are obvious over Micron in view of Connelly. Proposed rejection of claims 52, 64-65, 94, 96, 98, 102, 107, and 112-113, is **adopted**.

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181.   <u>Claims 64-65, 94, 96, 98, 102, 107, and 112-113 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connelly.</u>

182.   With respect to claim 64, **the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices** (see Connelly, Figure 3, 16).

183.   With respect to claim 65, **the logic element comprises means for generating rank-selecting signals of the set of output control signals for performing back-to-back adjacent read commands which cross DDR memory device boundaries** (see claim 64). Capability to perform back-to-back adjacent read commands (consecutive read across banks) is a basic capability of a memory module that is expected of any commercial quality memory module with multiple banks, regardless of whether there may be some potential issues like delays associated with switching banks. The Examiner notes that the passage cites as support for this limitation merely states that "the codes of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX."" The specification does not disclose the nature of the potential problems that the logic of the exemplary code supposedly reduces.

184.   The Examiner also notes that Sechen Declaration, paragraph 88, which supposedly explains how the '912 patent facilitates handling of command sequences that include successive

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or back-to-back adjacent read commands seeking to access data in two different physical ranks,

is problematic because the Vericode segment (cols. 17-19) that supposedly describes how the

logic element generates appropriate chip-select signals for the read command does not actually

generate any chip-select signal. The cited code corresponds to a logic element 40 which receives

one gated CAS signal from the computer system and which generates two gated CAS signals

(the '912 patent, c17:32-c18:30). The declarant also states at paragraph 89 that none of the cited

references discloses or suggests "this solution" to a person of ordinary skill in the art. The

Examiner agrees because prior art references cannot possibly disclose "a solution" to an

undisclosed problem with back-to-back adjacent read commands across ranks.

185.   With respect to claims 94, 96, and 98, **the logic element receives a bit of a non-bank
address signal of the set of input control signals** (Connelly, Figure 4, A11) **in conjunction
with an activate command** (activate command is used to open a row in a particular bank for
read or write) **and uses the bit to generate rank-selecting signals** (RAS A & RAS B) **for a
subsequent read or write command.**

186.   With respect to claim 102, **the logic element comprises means for generating rank-
selecting signals** (Connelly, Figure 4, RAS signals) **of the set of output control signals for
performing successive read accesses from different ranks of DDR DRAM devices of the
plurality of DDR DRAM devices** (Micron teaches DDR DRAM devices).

187.   With respect to claim 107, **the logic element comprises means for using at least one**

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address bit received by the memory module during an activate command operation to

generate chip-select signals for a read or write command operation, the read or write

command operation subsequent to the activate command operation (see claim 94).

188.   With respect to claims 112-113, **the logic element comprises means for performing**

sequential and combinatorial logic procedures (see Connelly, Figure 4) **to generate rank-**

selecting signals of the set of output control signals (see claim 94).

189.   Proposed rejection of claims 52-63, 66-93, 95, 97, 99-101, 103-106, 108-111, and 114-

118 is **not adopted**.

190.   With respect to claims 52-60, Connelly does not disclose that chip select signals are

generated as output control signals.

191.   With respect to claims 61-63, 75-76, 80-81, 90-91, 109-110, neither Connelly nor Micron

discloses that the ROM SPD stores data that characterizes the plurality of devices as having one

or more attributes that are different from the one or more attributes of the plurality of DDR

memory devices.

192.   With respect to claims 66-71 and 82-89, the proposed combination does not disclose that

the rank-selecting signals are generated at least in part to a bank address signal.

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193.   With respect to claims 72-74, the claims require generation of rank-selecting signal that

select none of the ranks and two ranks. Micron and Connelly combination does not disclose

these no-rank and two-rank selecting signals.

194.   With respect to claims 92 and 93, the claims require the logic element not to operate in

response to row/column address bits (A_0 - A_n). The logic element of the combination used to

reject the parent claims does operate in response to A_0-A_{12}.

195.   With respect to claims 95, 97, 99 and 101, the Micron and Connelly combination does

not teach that the bank address signals are used to generate rank-selecting signals. In the

combination, RAS, CAS and A_{11} signals are used to generate rank-selecting signals (RAS A and

RAS B).

196.   With respect to claims 100, 103-106, 108, and 114-118, the combination does not

generate chip-select signals.

Ground 13

197.   Requester 3 asserts that claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-33, 36-39, 41-45,

and 50 are obvious over Micron in view of Amidi. Proposed rejection of claims 1, 3-4, 6-8, 10,

11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50, is **adopted**.

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198.   Claims 1, 3-4, 6-8, 10, 11, 15, 18-20, 22, 24-25, 27-29, 31-33, 36-39, 41-45, and 50 are

rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Amidi.

199.   With respect to claim 1, Micron discloses **a memory module** (Figures 1-3) **connectable
to a computer system, the memory module comprising:**

    a printed circuit board (see Figure 1);

    a plurality of double data rate (DDR) memory devices (Figure 4, U1-U36) **mounted
to the printed circuit board, the plurality of memory devices having a first number of
memory devices arranged in a first number of ranks** (see Figure 4, the module has two
ranks);

    **a circuit mounted to the printed circuit board, the circuit comprising a logic element
and** (p.4, Figure 4, Register U37) **a register** (Register U38), **the logic element receiving a set of
input control signals** (see Figure 4, RAS #, CAS #, WE #, A0-A12, BA0, BA1, S0 #, S1 #)
**from the computer system, the set of input control signals comprising at least one
row/column address signal** (A0-A12), **bank address signals** (BA0, BA1), **and at least one
chip select signal** (S0); **and**

    a phase-lock loop device (Figure 4, PLL U40) **mounted to the printed circuit board,
the phase-lock loop device operatively coupled to the plurality of memory devices, the logic
element, and the register.**

200.   However, Micron does not specifically disclose that "the set of input control signals

corresponding to a second number of memory devices arranged in a second number of ranks, the

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second number of memory devices smaller than the first number of memory devices and the

second number of ranks less than the first number of ranks, the circuit generating a set of output

control signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of ranks,

wherein the circuit further responds to a first command signal and the set of input control signals

from the computer system by generating and transmitting a second command signal and the set

of output control signals to the plurality of memory devices, the first command signal and the set

of input control signals corresponding to the second number of ranks and the second command

signal and the set of output control signals corresponding to the first number of ranks."

201.   On the other hand, Amidi discloses a DIMM that receives a set of input control signals

(see Figure 6, the DIMM receives cs0, cs1, Add[n:0], BA[1:0], RAS, CAS, WE, and signals),

the set of input control signals comprising at least one row/column address signal

(Add[n:0]), bank address signals (BA[1:0]), and at least one chip select signal (cs0), the set

of input control signals corresponding to a second number of memory devices arranged in

a second number of ranks, the second number of memory devices smaller than the first

number of memory devices and the second number of ranks less than the first number of

ranks (see paragraphs 10-12, Amidi's invention is a transparent four rank module fitting into a

memory socket meant for a two rank module), **the circuit generating a set of output control**

signals in response to the set of input control signals, the set of output control signals

corresponding to the first number of memory devices arranged in the first number of

ranks, wherein the circuit further responds to a first command signal and the set of input

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control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices,

the first command signal and the set of input control signals corresponding to the second

number of ranks and the second command signal and the set of output control signals

corresponding to the first number of ranks (see Figure 6 and paragraph 52, "CPLD also

ensures that all commands for a two rank memory module conveyed by the module connector

602 are also performed on the four rank memory modules. For example, CPLD 604 generates

rsc2 and rcs3 ...").

202.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Micron and Amidi before him at the time the invention was made, to modify the design the

DIMM of Micron to adopt Amidi's transparent four rank memory module for standard two rank

sub-system teachings to be able to use lower capacity memory devices which can be much

cheaper (Amidi, p. 1, paragraph 8).

203.   With respect to claim 3, **the set of input control signals comprises a first number of**

chip-select signals (see Amidi, Figure 4, cs0 and cs1) **and wherein the set of output control**

signals comprises a second number of chip-select signals greater than the first number of

chip-select signals (rcs0a-rcs3a).

204.   With respect to claim 4, **the first number of chip-select signals is two and the second**

number of chip-select signals is four (see the discussion of claim 3 above).

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205.   With respect to claim 6, **the logic element comprises an application-specific
integrated circuit, a field-programmable gate array, a custom-designed semiconductor
device, or a complex programmable-logic device** (Amidi, Figure 6, CPLD).

206.   With respect to claim 7, **the bank address signals of the set of input control signals
are received by both the logic element and the register** (se claim 1).

207.   With respect to claim 8, **two or more of the phase-lock loop device, the register, and
the logic element are portions of a single component** (these are all portions of a single DIMM
which is a component of a personal computer).

208.   With respect to claim 10, **the plurality of DDR memory devices is arranged as a first
set of DDR memory devices on a first side of the printed circuit board, a second set of DDR
memory devices on the first side of the printed circuit board** (Amidi, Figure 4A, ranks 0 and
2 are on the front side), **a third set of DDR memory devices on a second side of the printed
circuit board, and a fourth set of DDR memory devices on the second side of the printed
circuit board** (Figure 4B, ranks 1 and 3 are on the back side), **the DDR memory devices of the
second set spaced from the DDR memory devices of the first set, the DDR memory devices
of the fourth set spaced from the DDR memory devices of the third set** (this is inherent as
two physical devices cannot occupy the same space at the same time).   Micron discloses this
limitation as well. See the discussion of claim 10 above.

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209.   With respect to claim 11, **the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side** (see Amidi, paragraph 34, the devices are stacked on the front and the back side; see also Micron, Figures 7 and 8).

210.   With respect to claims 15 and 28 see the discussion of claim 1 above.

211.   With respect to claims 39 and 50, see the discussion of claims 1 and 3 above.

212.   With respect to claim 18, **the command signal is transmitted to two ranks of the first number of ranks at a time** (see Amidi, Figure 6 and paragraph 52).

213.   With respect to claim 19, **the command signal comprises a refresh command signal** (see Amidi, paragraph 52).

214.   With respect to claim 20, **the command signal is transmitted to the two ranks of the first number of ranks concurrently** (see claim 18 above).

215.   With respect to claim 22, **the command signal comprises a read command signal or a write command signal** (read and write commands are inherent in any functioning DIMM), **the**

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set of input signals comprises a density bit which is a row address bit (the specification

describes the density bit simply as a row address bit that is latched during the activate command

for the selected bank, with no other attribute), **and the circuit is configured to store the row**

address bit during an activate command for a selected bank (see Amidi, Figure 6, register).

216.   With respect to claims 24, 29 and 41, **the logic element comprises an application-**

specific integrated circuit, a field-programmable gate array, a custom-designed

semiconductor device, or a complex programmable-logic device (Amidi, Figure 6, CPLD).

217.   With respect to claims 25, 42 and 43, **the set of input signals comprises a plurality of**

row/column address signals received and buffered by the register and sent from the

register to the plurality of DDR memory devices (see Amidi, Figure 6).

218.   With respect to claims 27 and 45, **two or more of the phase-lock loop device, the**

register, and the logic element are portions of a single component (see the discussion of

claim 8 above).

219.   With respect to claims 31 and 32, see the discussion of claim 3 above.

220.   With respect to claims 33 and 44, **the register receives the bank address signals and**

the input command signal of the set of input control signals (see claim 1).

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221.   With respect to claim 36, **the input command signal is a refresh signal and the output
command signal is a refresh signal** (Amidi, paragraph 52).

222.   With respect to claim 37, **the input command signal is a precharge signal and the
output command signal is a precharge signal** (Amidi, paragraph 52).

223.   With respect to claim 38, **the input command signal is a read signal or a write signal
and the output command signal is a read signal or a write signal.** See the discussion of claim
37 above.

224.   With respect to claim 39, see claims 1 and 3 above.

225.   Proposed rejection of claims 9 and 21 is **not adopted**. With respect to claim 9, the
combination as applied discloses only one register. With respect to claim 21, Requester cites
Table 6 of Micron and paragraph 61 of Amidi, without any explanation as to how the cited
passages disclose the limitation "wherein the configured to store an input signal of the set of
input signal during a row access procedure for subsequent use during a column access
procedure." The cited passages do not disclose that an input address signal stored during a row
access procedure is retained for subsequent use during a column access procedure from the cited
pages. Requester asserts that one of ordinary skill in the art would have known how to select and
store needed inputs for later use. However, requester fails to explain which "input signal from a

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row access procedure that would be needed in - but would otherwise be unavailable during -

subsequent column access procedure" would be saved for later use.

226.   The Examiner rejects claim 26 being obvious over Micron in view of Amidi.

227.   Claim 26 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron
in view of Amidi. See the rejection of this claim above (Ground 12).

228.   Requester 3 asserts that claims 52-118 are obvious over Micron in view of Amidi.
Proposed rejection of claims 52, 53, 61-65, 67-71, 75-91, 94, 96, 98, 100, and 102-118 is
adopted.

229.   Claims 52, 53, 61-65, 67-71, 75-91, 94, 96, 98, 100, and 102-118 are rejected under 35
U.S.C. 103(a) as being as being unpatentable over Micron in view of Amidi.

230.   With respect to claim 52, **the logic element is responsive at least in part to a row
address bit of the at least one row/column address signal, the bank address signals, and the
at least one chip-select signal by generating a first number of chip- select signals of the set
Of output control signals (see claim 1 above), the first number of chip-select signals
generated by the logic element equal to the first number of ranks (see Amidi, Figure 6,
CPLD 604, rcs0-4), and the at least one chip-select signal of the set of input control signals**

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comprises a second number of chip-select signals equal to the second number of ranks (cs0,

cs1).

231.   With respect to claim 53, **the register receives and buffers the bank address signals**

(see Micron, p. 8, BA0 and BA1 are buffered in the two registers) **and transmits the buffered**

bank address signals to the plurality of DDR memory devices, the phase-lock loop device

transmitting clock signals to the plurality of DDR memory devices and to both the logic

element and the register (see Amidi, Figure 6, PLL 606 transmits clock signals to Register 608;

in the combination, the two registers of Micron would receive clock signals from the PLL and

because the logic element comprising one of the two registers both the logic element the register

receive clock signals from the PLL).

232.   With respect to claim 61, **the plurality of DDR memory devices has at least one**

attribute selected from a group consisting of: a number of row address bits per DDR

memory device, a number of column address bits per DDR memory device, a number of

bank address bits per DDR memory device, a number of DDR memory devices, a data

width per DDR memory device, a memory density per DDR memory device, a number of

ranks of DDR memory devices, and a memory density per rank,

        the memory module further comprising a read-only non-volatile memory device

storing data accessible to the computer system (Amidi, Figure 4A, SPD 414; Micron, p. 9,

SPD data storage EEPROM), **wherein the data characterizes the plurality of DDR memory**

devices as having at least one value of the at least one attribute that is different from an

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actual value of the at least one attribute of the plurality of DDR memory devices (see

Bagherzadeh Declaration, ¶ 48, "One skilled in the art would understand that in order to appear

transparent to the computer system, which generally cannot use a four rank memory module, the

SPD device taught by Amidi must store data characterizing the module as a two rank module of

different memory density").

233.   With respect to claim 62, **the at least one attribute comprises the number of ranks of**

DDR memory devices and the memory density per rank (see claim 61).

234.   With respect to claim 63, **the data characterizes the plurality of DDR memory devices**

as having fewer ranks of DDR memory devices than the plurality of DDR memory devices

actually has, and as having a greater memory density per rank than the plurality of DDR

memory devices actually has (see claims 57 and 61).

235.   With respect to claim 64, **the logic element comprises means for generating rank-**

selecting signals of the set of output control signals for performing successive read accesses

from different ranks of DDR memory devices of the plurality of DDR memory devices (see

Amidi, Figure 5 and paragraph 43).

236.   With respect to claim 65, **the logic element comprises means for generating rank-**

selecting signals of the set of output control signals for performing back-to-back adjacent

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read commands which cross DDR memory device boundaries (see Amidi, Figure 5 and

paragraph 43).

237.   With respect to claims 67 and 82, **the logic element is responsive at least in part to the

bank address signals and the at least one chip-select signal of the set of input control signals

by generating a number of rank-selecting signals of the set of output control signals that is

greater than double or equal to double the number of chip-select signals of the set of input

control signals** (see claim 52).

238.   With respect to claim 68, **the plurality of DDR memory devices and the logic element

are timed to clock signals from the phase-lock loop device** (see Amidi, Figure 6), **wherein the

memory module is operable for use in a server system** (DIMM memory modules can be used

in a server system or any other system that can accept DIMM modules).

239.   With respect to claims 69, 102, and 103, see claim 64.

240.   With respect to claims 70, 78, 83, 88, 104, and 105, see claim 65.

241.   With respect to claim 71, **the bank address signals include bank address signals

received during an activate command operation and bank address signals received during

a read or write command operation subsequent to the activate command operation, and the**

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rank-selecting signals are used for the read or write command operation (these limitations

are inherent in any functioning DIMM with multiple ranks).

242.   With respect to claims 75, 80, 85, and 90, see claim 61 above.

243.   With respect to claim 76, substituting commodity DDR DRAM chips with other DDR

DRAM chips of the same family would have been obvious to one skilled in the art (see

Kozyrakis Declaration, ¶ 17).

244.   With respect to claims 77 and 87, **the logic element is responsive at least in part to the**

bank address signals and the at least one chip-select signal of the set of input signals by

generating a number of rank-selecting signals of the set of output signals that is greater

than double or equal to double the number of chip-select signals of the set of input signals

(see claim 52 above).

245.   With respect to claims 79, 84, and 89, **the plurality of DDR memory devices and the**

logic element are timed to clock signals from the phase-lock loop device (see claim 57).

246.   With respect to claims 81, 86, and 91, **the one or more attributes comprise the number**

of ranks of DDR memory devices and the memory density per rank and the data

characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory

devices than the plurality of DDR memory devices actually has, and as having a greater

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memory density per rank than the plurality of DDR memory devices actually has (see claim

63).

247.   With respect to claims 94, 96, 98, and 100, **the logic element receives a bit of a non-**

bank address signal of the set of input control signals (Figure 6, cs0 and cs1) **in conjunction**

with an activate command (activate command is used to open a row in a particular bank for

read or write) **and uses the bit to generate rank-selecting signals** (see Figure 5, cs0 and cs1

bits are used to select an active bank) **for a subsequent read or write command.**

248.   With respect to claims 106, 107, and 108, **the logic element comprises means for using**

at least one address bit received by the memory module during an activate command

operation to generate chip-select signals for a read or write command operation, the read

or write command operation subsequent to the activate command operation (see claim 94).

249.   With respect to claims 109-111, **the memory module comprises means for**

characterizing the plurality of DDR memory devices as having one or more attributes that

are different from actual attributes of the plurality of DDR memory devices (see claim 61).

250.   With respect to claims 112-114, **the logic element comprises means for performing**

sequential and combinatorial logic procedures (see Amidi, Figure 8) **to generate rank-**

selecting signals of the set of output control signals (see claim 94).

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251.   With respect to claims 115 and 117, **the first command signal is a row access
command signal, and the logic element uses sequential and combinatorial logic procedures
with at least one address bit of the set of input control signals** (see Amidi, Figure 8) **and the
at least one chip-select signal to generate chip-select signals for the second command signal**
(see claim 94).

252.   With respect to claims 116 and 118, **the logic element further uses the sequential and
combinatorial logic procedures with the at least one address bit** (see Figure 8) **to generate
chip-select signals for a column access command signal subsequent to the row access
command signal, wherein the memory module receives a second column access command
signal between receiving the row access command signal and the subsequent column access
command signal** (see claim 94).

253.   Proposed rejection of claims 54-60, 66, 72-74, 92-93, 95, 97, 99, and 101, is **<u>not</u>
<u>adopted</u>**.

254.   With respect to claims 54-60, Micron and Amidi do not disclose that the generation of the
first number of chip-select signals by the logic element is timed (or in response) to the clock
signals received from the phase-lock loop device. In the combination, the generation of chip-
select signals (CPLD output signals) is timed to the clock signals that are supplied to the PLL,
not received from the PLL.

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255.   With respect to claims 66, Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals.

256.   With respect to claims 72-74, the claims require generation of rank-selecting signal that select none of the ranks and two ranks. Micron and Amidi combination does not disclose these no-rank and two-rank selecting signals.

257.   With respect to claims 92 and 93, the claims require the logic element not to operate in response to row/column address bits (A_0 - A_n). The logic element of the combination used to reject the parent claims does operate in response to A_0-A_n.

258.   With respect to claims 95, 99 and 101, the Micron and Amidi combination does not teach that the bank address signals are used to generate rank-selecting signals. In the combination, chip-select and A_n signals are used to generate rank-selecting signals.

259.   With respect to claim 97, in the proposed combination bank address signals are not used to generate the rank-selecting signals for a subsequent read or write command.

Ground 14

260.   Requester 1 asserts that claims 57-60, 68, 76, 79, 84, and 89-91 should be rejected under 35 U.S.C §112, first paragraph. Proposed rejection is **not adopted**. Requester 1 asserts that

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persons of ordinary skill in the art would not know how the signal from the phase locked loop

was used by the logic element of the '912 patent, because neither the claims nor the description

of the '912 patent explain how this signal is used (Comment 1, p. 17). The Examiner disagrees.

The '912 patent specifically discloses that "[i]n response to signals received from the computer

system, the phase-locked loop device 50 transmits clocks signals to the plurality of memory

devices 30, the logic element 40, and the register 60" (c5:27-31). Requester 1's assertion that

one skilled in the art would not know how clock signals are used to drive digital circuit elements

of a memory decoder is not credible. Clocks are used to synchronize timing of operations of

various circuit elements in a digital device. Because clocks control the timing of operations,

generation of output signals in a logic circuit that uses clock signals to operate properly is

necessarily responsive at least in part to clock signals received.

261.   Requester 1 further asserts that "[t]he '912 patent simply does not describe any

relationship between output control signals and clock signals received from a phase-locked loop

device or a logic element time to the clock signals from a phase locked loop device" (Comments

1, p. 17). Requester 1's implicit assertion that because there is no detailed description of exactly

how the clock signals are used to operate the circuits to generate output signals the '912 does not

disclose the new claim limitations is undermined by Requester 1's allegation that Amidi teaches

the limitations of claim 57 and other claims involving the clock signals from the PLL. There is

no detailed disclosure in Amidi of how the clock signals are used to generate the claimed output

signals. Yet, Requester 1 asserted that Amidi teaches the same limitations when Amidi's

disclosure with respect to the clock signals is no more detailed than the '912 patent's.

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262.   Requester 1 asserts that claim 76 should be rejected because the claim requires DDR

DRAM packages that are chip packages beyond DDR3 chip packages and that it fails to

particularly point out and distinctly define the metes and bounds of chip packages beyond DDR3

chip packages. This is argument is not persuasive because the specification of the '912 patent

specifically discloses that "the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip

packages, or chip packages beyond DDR3 chip packages" at c12:26-29. As to the allegation of

indefiniteness, 35 U.S.C §112, first paragraph is not the proper ground for an indefiniteness

rejection.

263.   Requester 3 asserts that claims 92-101 and 115-118 should be rejected under 35 U.S.C

§112, first paragraph. Proposed rejection is **adopted.**

264.   <u>Claims 92-101 and 115-118 are rejected under 35 U.S.C. 112, first paragraph, as failing</u>

<u>to comply with the written description requirement.</u> The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention.

265.   With respect to claims 92 and 93, the claims recite the limitation "wherein the set of input

control signals include row/column address bits (A_0 - A_{n+1})." The parent claim (claim 1) requires

the "logic element" to receive the set of input control signals. Patent Owner cites c7:39-41 and

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Figures 1A and 1B as support for the limitation. However, c7:39-41 states that "the memory

module 10 receives row/column address signals or signal bits $(A_0 - A_{n+1})$. Figures 1A and 1B

clearly shows that the logic element 40 receives A_{n+1}, but not $A_0 - A_{n+1}$ as required by the claims.

266.   With respect to claims 94-101, the claims require the logic element to receive a bit of a

non-bank address signal of the set of input control signals in conjunction with an activate

command and uses the bit to generate rank-selecting signals for a subsequent read or write

command. Patent Owner cites c2:36-38, c9:18-21, c17:28-c19:52 and Figures 1A, 1B, 3A and

3B. However, the claimed limitation is not apparent from the cited disclosures and Patent Owner

has failed to explain how the cited passages and the Figures disclose the claimed limitations.

267.   Claims 95, 97, 99, and 101 also require the logic element to further receive the bank

address signals in conjunction with the activate command and uses the bank address signals to

generate the rank-selecting signals for a subsequent read or write command. Patent Owner cites

the same passages as claim 94 without any explanation as to how these claims are supported.

268.   With respect to claims 115-118, Patent Owner cites c17:28-c21:19, 52, c22:15-23:25, and

Figures 3A and 3B. The cited passages and the Figures disclose generating CAS signals not

chip-select signals as claimed.

Ground 15

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269.   Requester 3 asserts that claims 68-70, 76, 78, 83, 88, 94, 96, 98, 100, 115-118 are not

enabled. Proposed rejection of claims 115-118 is **adopted.**

270.   Claims 115-118 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply

with the enablement requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to enable one skilled in the art to which it pertains, or with

which it is most nearly connected, to make and/or use the invention. See Ground 14.

271.   Proposed rejection of claims 68-70, 76, 78, 83, 88, 94, 96, 98, and 100 is **not adopted.**

272.   Requester 3 asserts that claims 68-70, 78, 83, and 88 are not enabled because the

"wherein" clause associated with the "memory module" limitation is purely functional without

any structure. The Examiner disagrees. The "wherein" clause further describes the "memory

module" which is a structure. The scope of the claims is not all structures that can perform the

recited functions as Requester alleges. It is limited to the memory module.

273.   Requester 3 asserts that claim 76 is not enabled because the specification is insufficient to

enable one skilled in the art to make and use the claimed invention with reference the recited

limitation of "chip packages beyond DDR3 chip packages." The Examiner disagrees. The

specification makes it clear that the nature of the invention does not depend on any specific

characteristic of the DRAM device used (see specification, c6:12-16, and c12:25-29). The claim

is limited in scope to the DDR family of DRAM chips, while the disclosure itself is not so

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limited. Thus, unless Requester can provide evidence that future DDR family of DRAM chips

would somehow be incompatible with existing DRAM and DIMM designs, it is reasonable for

one skilled in the art to assume that future DDR family of DRAM would not be incompatible

with the invention.

274.   With respect to claims 94, 96, 98, and 100, Requester 3 asserts that the claims are not

enabled because the claim limitation "a non-bank address signal of the set of input control

signals in conjunction with an activate command" is broader than, and therefore not

commensurate with, the scope of what is described in the specification (see Exhibit M, p. 4).

The Examiner disagrees. The limitation above is not so broad in scope, than what is described in

the specification, so as to be non-enabled. The limitation is confined to the set of input control

signals received from the computer system as recited in the parent claims, not just any signals.

Mere allegation of non-enablement is insufficient to make a prima facie case. Requester must

provide a reasoned analysis, with evidence as appropriate, as to why the claims are so broad so

as to be not enabled when they are considered as a whole.

Ground 16

275.   Requester 1 asserts that claim 76 should be rejected under 35 U.S.C §112, second

paragraph. Proposed rejection is **not adopted**. Requester asserts that claim 76 requires DDR

DRAM chips packages that are chip packages beyond DDR3 chip packages and that the term

beyond has no outer boundary and nothing in the specification attaches special meaning to

"beyond DDR3 packages" (Comments 1, p. 19). The Examiner first notes that claim 76 does not

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require chip packages beyond DDR3 chip packages because it is claimed as an alternative

limitation. Also the term beyond is not unbounded as Requester 1 asserts. When read in the

context of the specification and the claim, "beyond DDR3 chip packages" refers to the DDR

family or series of chip packages.

276.   Requester 3 asserts that claims 64, 65, 68, 76, 89, 94, 95, 97, 99, 101, 102-108, 112-118

should be rejected under 35 U.S.C §112, second paragraph. Proposed rejection of claims 116-

118 is **adopted**.

277.   Claim 116-118 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite

for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention.

278.   With respect to claim 116, the claim recites an apparatus and a method step of using the

apparatus in a single claim.

279.   With respect to claims 117-118, the claims recite the limitation "the set of input signals."

It is unclear whether the limitation refers to "a set of input control signals" or "an input command

signal" or the combination of the two.

280.   Proposed rejection of claims 64, 65, 68, 76, 89, 94, 95, 97, 99, 101, 102-108, 112-115 is

not adopted.

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281.   With respect to claims 64-65, Requester 3 asserts that the specification fails to disclose a

structure that is clearly linked to performance of the recited functions and that the specification

does not teach generating rank-selecting signals for performing back-to-back adjacent read

commands (see Exhibit M. p. 1). The Examiner disagrees. The specification discloses a section

of Vericode that corresponds to a logic element 40 which receives one gated CAS signal from

the computer system and which generates two gated CAS signals at c17:28-c19:53. Requester

3's implicit argument that the disclosed structure or algorithm does not teach generating rank-

selecting signal is inconsistent with Requester 3's assertion that Connelly's Figure 4 discloses

this limitation (see Exhibit L, p. 6).

282.   With respect to claim 68, Requester asserts that the "operable for use" language of the

claim fails to comply with 35 U.S.C. §112, second paragraph because the language merely

recites an intended use and not a structure. This is not a persuasive argument because recitation

of an intended use language in a claim does not make the claim indefinite.

283.   With respect to claim 76, see above.

284.   Requester 3 asserts that claim 89 is indefinite because it depends from claim 87.

Requester has not proposed an indefiniteness rejection of claim 87.

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285.   Requester 3 asserts that claims 94-101 are indefinite because the phrase "in conjunction with" is impermissibly vague, making it impossible to determine the scope of what the limitation entails. However, Requester 3 has not explained why the phrase is impermissibly vague so as to make it impossible to determine the scope of the claim. The Examiner had no problem understanding what the phrase means in the context of the claim.

286.   With respect to claims 102-105, see claim 64 above.

287.   With respect to claims 106-108, see claim 64 above. See also Figures 1A, 1B and example 1 at c14:17-c17:27.

288.   With respect to claims 112-114, see claim 64 above.

289.   With respect to claims 115, Requester 3 asserts that the claim is indefinite because it recites "us[ing] sequential and combinatorial logic procedures" without reciting any active positive steps delimiting how this use is actually practiced. Requester has not explained why it is necessary to recite an active positive step in an apparatus claim to make the claim definite.

Ground 17

290.   Requester 2 asserts that claim 76 should be rejected as being obvious over Amidi in view of JEDEC and Vogt. The propose rejection is **adopted**.

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291.   Claim 76 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Amidi in view of JEDEC 21-C and Vogt.

292.   Amidi and JEDEC disclose all of the limitations of the parent claim 75 (see Ground 6). However, Amidid and JEDEC do not specifically disclose the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages. On the other hand, Vogt specifically discloses a DIMM with DDR2 chips. It would have been obvious to one of ordinary skill in the art, having the teachings of Amidi, JEDEC and Vogt before him at the time of the invention, to use DDR2 chips in the DIMM module of Amidi and JEDEC, to be able to offer upgraded DIMMs with the latest available memory chips.

Ground 18

293.   Requester 3 asserts that claims 1, 15, 28, and 39 are obvious over Micron in view of Connelly and Dell 2. Proposed rejection is **adopted**.

294.   Claims 1, 15, 28, and 39, are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Micron in view of Connolly and Dell 2. See Ground 12 above. Because these claims are obvious over Micron and Connolly, they are obvious over Micron, Connolly and Dell 2.

Ground 19

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295.   Requester 3 asserts that claim 21 is obvious over Micron in view of Amidi and Dell 2.

Proposed rejection is **not adopted**. Requester 3 asserts that a person of ordinary skill in the art

would have been motivated to consider the teachings of Dell 2, because like Connolly, Dell 2

describes techniques for address signal remapping. The teaching of Dell 2 to be applied in the

combination is the alleged storage of the value of the A12 signal to resend the BA1 signal at

CAS time to ensure that the correct bank is addressed. Contrary to Requester 3's assertion, Dell

2 does not disclose that the input signal A12 is stored. Dell 2 discloses that BA1 address, which

is a remapped address, is stored by the ASIC. BA1 is not an input signal of the set of input

signals. Also, it is not clear how Dell 2's teaching of using the remapped BA1 address to select

an active bank/rank can be combined with Amidi's teaching of using chip-select and row/column

address signals to select an active bank to produce the claimed apparatus.

Examiner's Statement of Reasons for Patentability/Confirmation

296.   Claims 2, 5, 9, 16, 17, 21, 23, 30, 51, 54-60, 66, 72-74 are deemed to be patentable and/or

confirmed over the prior art of record for the following reasons: Claim 9 recites the limitation

"the register comprises a plurality of register devices". Prior art references as applied in this

Office Action only disclose one register. Claims 2, 5, 21, 23, 30, and 51 require storage of an

input signal during a row access procedure for subsequent use during a column access procedure.

As discussed above, prior art references or combination of references applied in this Office

Action do not disclose this input signal storage feature of these claims. With respect to claims 16

and 17, Requester 1 has failed to make a prima facie case that the Examiner can adopt. As to

claims 54-60, 66, and 72-74, see Ground 6 above.

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Response to Arguments

Secondary Considerations

297.   Patent Owner asserts that Lopez and Lee Declarations submitted provide evidence of

secondary considerations (industry acceptance and praise by others) to overcome any prima facie

case of obviousness that may be presented (Response p. 36). Requester 1 asserts that Patent

Owner has not established a nexus between the claimed invention and evidence of commercial

success (Comments 1, p. 14). Requester 2 also asserts that Patent Owner has not demonstrated

any nexus between the "praise" of its HyperCloud product and the claimed features at issue

(Comments 2, p. 12). The Examiner agrees with Requesters 1 and 2, that Patent Owner has not

demonstrated any nexus between the "praise" and "acceptance" and the claimed features that are

found to be obvious.

298.   Although Patent Owner attempts to establish that the "rank multiplication" technology

disclosed in the '912 patent is responsible for the praise and acceptance with the Lee Declaration,

the inventors of the '912 patent are not the first inventors of this technology as evidenced by the

prior art of record (Amidi, Connelly, Dell 1 & 2, etc.). This "rank multiplication" technology

was well known in the art before the date of the invention. An anticipated feature cannot be non-

obvious. To overcome the prima facie case of obviousness, Patent Owner must provide

objective evidence of non-obviousness that establishes a nexus between the "praise" and

"acceptance" and features in the claims that are found to be obvious. Patent Owner has failed to

even link the claims to the evidence, much less the obvious features of the claims.

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Ground 1

299.   Requester 1 argues that "[t]he Examiner should reconsider the confirmation of

allowability of claims 1-17, 19, 21, and 23-51 over the QBMA Reference and the JEDEC DIMM

Standard" because although page 17 of the QBMA Reference does not explicitly show all of the

signals recited in the claims, page 17 is one of many pages in the QBMA (see Requester 1's

Comments, p. 68). Requester 1 alleges that the control signals used for controlling the QBM

switch are described elsewhere in the QBMA Reference and JEDEC Standard in sufficient detail

that a person of ordinary skill in the art would have been motivated and able to combine the

references in a manner that yielded the inventions claimed by the '912 patent. The Examiner

notes that the claims have not been confirmed as being allowable as Requester 1 alleges. These

claims have been rejected on other grounds. The Examiner's decision was not to adopt the

rejection as proposed by Requester 1 because the rejection was deficient.

300.   Requester 1's argument has been fully considered but is not persuasive. Requester 1

specifically identified the QBM switch shown on page 17 as the structure that teaches the

claimed logic element. The claimed logic element is required to receive a set of input control

signals specified in the claims. Although these input control signals are shown in the QBMA

and JEDEC, the references do not disclose that the control signals are received by the QBM

switch as required. Input and output signals of the QBM switch are clearly identified on page

17. They do not include the specific set of control signals claimed (at least one row/address

signals, bank address signals, and at least one chip-select signal). If the input control signals

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used for controlling the QBM switch are described elsewhere in QBMA as Requester 1 asserts,

Requester 1 has failed to explain where in the QBMA reference such a disclosure can be found.

Nor has Requester 1 shown how the combination of references discloses the claimed logic

element with all of the required input control signals, and why one skilled in the art would

modify the QBM switch of page 17 to accept the claimed input control signals.

301.   A prima facie case of obviousness cannot be made by merely throwing all the recited

structural elements from different disclosures into a combination and alleging that it would have

been obvious to make the combination. The combination must teach all of the structural

limitations and there must be an articulation of some reason to support the conclusion of

obviousness. In this case, the proposed combination simply does not teach all of the structural

limitations of the logic element and no reason has been given to modify the QBM switch to

receive all of the required control input signals.

Ground 2

302.   Requester 1 asserts that a person of ordinary skill in the art would have been familiar with

the features of DDR DRAMs as described in industry standards, including the presence of chip

select signal inputs on the devices and that one skilled in the art would have known how to

modify or generate a chip-select signal consistent with the Dell 2 address translation scheme

(Comments 1, p. 70). The Examiner agrees that one skilled in the art would have been familiar

with chip select signals. In fact, a chip select signal is well known in the art. However, issue is

not whether a chip select signal is known in the art. The real issue is whether Requester 1 has

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made a prima facie case of obviousness of modifying Dell 2's memory module so that it teaches

all the limitations of the claims. The proposed rejection is devoid of any articulation of reasons

as to why one skilled in the art would include a chip select input to the address re-mapping logic

circuit of Dell 2 and why it would have been obvious to modify the address re-mapping device to

generate output control signals. Mere allegation that these features are known in the art and that

it would have been obvious to include them is not enough to meet the burden of establishing the

prima facie case of obviousness.

Ground 3

303.   Patent Owner argues that a person of ordinary skill in the art would not interpret the term

"logic element" as encompassing both the translation logic device and the register that passes

signal onto the DRAM devices (Patent Owner's Response, p. 38). To the extent that Patent

Owner's arguments are directed to the application of Amidi in the anticipation rejection of the

last Office Action, the Examiner agrees that the "logic element" and the "register" are separate

elements in the claims. However, there is nothing in the claims or the specification that

precludes the logic element from comprising a storage device such as a register. The term "logic

element" is not a term of art. Nor is the term specifically defined in the specification. Therefore,

the term is construed using the ordinary definition of the words used in the term. Thus, the

Examiner interprets the term "logic element" as an element that performs some kind of logic

function or an element that comprises a logic circuit. This interpretation is consistent with the

specification of the '912 patent.

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304.   Patent Owner's other arguments are moot because the rejection is not adopted.

Grounds 4 and 5

305.   Patent Owner's other arguments are moot because the rejections are not adopted.

Ground 6

306.   Patent Owner's other arguments are moot because the rejection no longer relies on

Ground 3 as applied in the last Office Action.

Ground 7

307.   Requester 1 asserts that a person of ordinary skill in the art would have been motivated to

combine Murdocca's address decoding method with Dell 2 system, which provides address

remapping logic in an ASIC to handle reconfiguration of banks of memory devices (Comments

1, p. 70). As explained above, Requester 1 has failed to show how the combination results in a

device that teaches all of the limitation of the claims.

Ground 9

308.   Patent Owner's argument that the combination of Dell 1 and JEDEC 21-C does not

disclose or render obvious a memory module having a logic element that receives bank address

signals as required (Response, p. 50) is moot because the rejection in this Office Action relies on

JEDEC Register 2 to receive bank address signals.

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309.   Patent Owner next argues that the EDO devices used in Dell 1 do not have bank address

of memory locations that would be accessed using bank address signals, thus, there is no need to

receive such address signals (Response, p. 51). This is not a persuasive argument because the

rejection is based on the combination of Dell 1 and JEDEC and JEDEC discloses DDR DRAM

devices. The rejection specifically proposes using DDR DRAM devices as taught by JEDEC.

310.   Patent Owner also argues that due to the significant differences between DDR memory

technology and Dell 1's EDO technology, persons of ordinary skill in the art would not find it

obvious to replace the EDO memory devices of Dell 1 with the DDR memory devices of JEDEC

21-C as proposed (Response, p. 51). This argument is not persuasive. Although Patent Owner

asserts that Dell 1 teaches EDO devices, there is nothing in Dell 1 that confines the invention to

DIMMs made with EDO devices. Dell 1 does not identify the DRAMs used in the DIMM as

EDO DRAMs. The devices are generically referred to as DRAMs as opposed to SRAMs. In

fact, Dell 1 specifically states that "it is understood that this description is made only by way of

example, that the invention is not limited to particular embodiments described herein, and that

various rearrangements, modifications, and substitutions may be implemented without departing

from the true spirit of the invention as hereinafter claimed" (c6:63-68). As evidenced by

JEDEC, one skilled in the art would know how to make a DIMM with DDR DRAM devices at

the time of the invention.

Ground 11

311.   See Ground 9 above.

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Ground 12

312.   Patent Owner asserts that Micron does not disclose a memory module having a logic

element that receives bank address signals to generate output signals (Response, p. 57). The

Examiner disagrees. Micron discloses two registers U37 and U38 that receive bank address

signals and other signals required by the claims. As discussed above, there is nothing in the

claims or the specification that precludes the "logic element" from comprising a register so long

as there is at least one other register that teaches the claimed register limitation.

313.   Patent Owner's argument that one skilled in the art would not combine the teachings of

Micron and Connelly because of the difference between EDO and DDR addressing and

command protocols is based on Patent Owner's misinterpretation of the proposed combination.

It is not the EDO addressing teachings of Connelly, if there are such teachings in Connelly as

asserted by Patent Owner (as far as the Examiner can discern, Connelly does not specify the type

of DRAMs used in the DIMMs), that are being combined with Micron's teaching of DIMM

modules. Connelly's teaching to be adopted is the technique of generating two RAS and CAS

signals from a set of one RAS and one CAS signals, so that two banks of lower density DRAM

chips can be used in a DIMM in place of a single bank of higher density chips.

314.   With respect to claim 21, Patent Owner explains that latching of SYS RAS only occurs

by "SYS_CAS going active (which will cause SYS RAS to be latched)" and that the address bit

A11 latched during a row access procedure is used to determine whether to make RAS A or RAS

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B active during a row access procedure. Upon closer inspection of the reference, the Examiner

agrees with Patent Owner. Accordingly, the rejection of claim 21 adopted in the last Office

Action is withdrawn.

Ground 13

315.   See Grounds 6 and 12 above.

Submissions

316.   In order to ensure full consideration of any amendments, affidavits or declarations, or

other documents as evidence of patentability, such documents must be submitted in response to

this Office action. Submissions after the next Office action, which is intended to be an Action

Closing Prosecution (ACP), will be governed by 37 CFR 1.116(b) and (d), which will be strictly

enforced.

Extensions of Time

317.   Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes*

reexamination proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant"

and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c)

requires that *inter partes* reexamination proceedings "will be conducted with special dispatch"

(37 CFR 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are

provided for in 37 CFR 1.956. Extensions of time are not available for third party requester

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comments, because a comment period of 30 days from service of patent owner's response is set

by statute. 35 U.S.C. 314(b)(3).

Service of Papers

318.   Any paper filed with the USPTO, i.e., any submission made, by either the Patent Owner

or the Third Party .Requester must be served on every other party in the reexamination

proceeding, including any other third party requester that is part of the proceeding due to merger

of the reexamination proceedings. As proof of service, the party submitting the paper to the

Office must attach a Certificate of Service to the paper, which sets forth the name and address of

the party served and the method of service. Papers filed without the required Certificate of

Service may be denied consideration. 37 CFR 1.903; MPEP 2666.06.

Amendment in Reexamination Proceedings

319.   Any proposed amendment to the specification and/or claims in this reexamination

proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37

CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). Amendments in an

inter partes reexamination proceeding are made in the same manner that amendments in an *ex*

parte reexamination are made. MPEP 2666.01. See MPEP 2250 for guidance as to the manner of

making amendments in a reexamination proceeding.

Notification of Concurrent Proceedings

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320.   The patent owner is reminded of the continuing responsibility under 37 CFR 1.985(a), to

apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the

patent undergoing reexamination or any related patent throughout the course of this

reexamination proceeding. The third party requester is also reminded of the ability to similarly

inform the Office of any such activity or proceeding throughout the course of this reexamination

proceeding. See MPEP § 2686 and 2686.04.

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All correspondence relating to this *inter partes* reexamination proceeding should be directed as
follows:

By **U.S. Postal Service Mail** to:

    Mail Stop *Inter Partes* Reexam
    ATTN: Central Reexamination Unit
    Commissioner for Patents
    P.O. Box 1450
    Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
             Central Reexamination Unit

By hand to: Customer Service Window
             Randolph Building
             401 Dulany St.
             Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination
Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the
Central Reexamination Unit at telephone number (571) 272-7705.

/Woo H. Choi/

Woo H. Choi
Reexamination Specialist
Central Reexamination Unit 3992

Docket No.: 635162800300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:	
Jayesh BHAKTA et al.	Examiner: Woo H. CHOI
Control Nos.: 95/000,578; 95/000,579; 95/001,339	Art Unit: 3992
Filed: October 20, 2010; October 21, 2010; June 8, 2010	Conf. No.: 5035

For: MEMORY MODULE DECODER

RESPONSE/AMENDMENT

MS Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 14, 2011, for which a response was due on December 14, 2011, and for which a one-month extension of time to extend the time for response from December 14, 2011 to January 17, 2012 (the first business day after January 14, 2012) was requested and granted, please consider the following.

There are no amendments to the specification or drawings.

Claim amendments begin on page 1 and continue to page 45.

Status of all claims is provided at page 46.

Remarks/Arguments begin on page 47.

An explanation of support for the new claims added with this Amendment begins on page 59.

A certificate of service is provided at page 63.

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Samsung Electronics Co., Ltd.
Ex. 1010, p. 3095

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(continued)

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CLAIM AMENDMENTS

Please **cancel** claims 64-66, 94-108 and 112-118.

Please **enter** the following amendments and new claims.

1.   (Amended)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

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signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals.

2.   (Amended)   [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the

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first number of DDR memory devices arranged in the first number of ranks, wherein the circuit

further responds to a first command signal and the set of input control signals from the computer

system by generating and transmitting a second command signal and the set of output control

signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of

output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input control signal of the set of input control

signals during a row access procedure and to transmit the stored input control signal as an output

control signal of the set of output control signals during a column access procedure.

3.   (Original)   The memory module of claim 1, wherein the set of input control

signals comprises a first number of chip-select signals and wherein the set of output control signals

comprises a second number of chip-select signals greater than the first number of chip-select

signals.

4.   (Original)   The memory module of claim 3, wherein the first number of chip-

select signals is two and the second number of chip-select signals is four.

5.   (Amended)   [The memory module of claim 1] A memory module connectable to a

computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column

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address signals to the plurality of DDR memory devices during a subsequent column access
procedure.

6.   (Original)   The memory module of claim 1, wherein the logic element comprises
an application-specific integrated circuit, a field-programmable gate array, a custom-designed
semiconductor device, or a complex programmable-logic device.

7.   (Amended)   [The memory module of claim 1] A memory module connectable to a
computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board,
the plurality of DDR memory devices having a first number of DDR memory devices arranged in a
first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a
register, the logic element receiving a set of input control signals from the computer system, the set
of input control signals comprising at least one row/column address signal, bank address signals,
and at least one chip-select signal, the set of input control signals corresponding to a second number
of DDR memory devices arranged in a second number of ranks, the second number of DDR
memory devices smaller than the first number of DDR memory devices and the second number of
ranks less than the first number of ranks, the circuit generating a set of output control signals in
response to the set of input control signals, the set of output control signals corresponding to the
first number of DDR memory devices arranged in the first number of ranks, wherein the circuit
further responds to a first command signal and the set of input control signals from the computer

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system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

8.   (Original)   The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9.   (Amended)   [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR

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memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the register comprises a plurality of register devices.

10.   (Original)   The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11.   (Original)   The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the

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first side and the memory devices of the fourth set are spaced from the memory devices of the third

set in a direction along the second side.

12.   (Original)   The memory module of claim 1, wherein the plurality of DDR

memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second

rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed

circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the

second side different from the first side.

13.   (Original)   The memory module of claim 12, wherein the first rank is spaced

from the second rank and the third rank is spaced from the fourth rank.

14.   (Original)   The memory module of claim 1, wherein the set of input control

signals corresponds to a first memory density, and the set of output control signals corresponds to a

second memory density, the second memory density greater than the first memory density.

15.   (Amended)   A memory module connectable to a computer system, the memory

module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,

the plurality of DDR memory devices having a first number of DDR memory devices arranged in a

first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a

register, the logic element receiving a set of input signals from the computer system, the set of input

signals comprising at least one row/column address signal, bank address signals, and at least one

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chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to a bank address signal of the set of input signals.

16.   (Amended)   [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

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a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

17.   (Original)   The memory module of claim 16, wherein the command signal comprises a read command signal.

18.   (Original)   The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19.   (Original)   The memory module of claim 18, wherein the command signal comprises a refresh command signal.

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20.   (Original)   The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21.   (Amended)   [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

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a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

22.   (Original)   The memory module of claim 15, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

23.   (Amended)   [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals,

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the set of output signals configured to control the first number of DDR memory devices arranged in

the first number of ranks, wherein the circuit further responds to a command signal and the set of

input signals from the computer system by selecting one or two ranks of the first number of ranks

and transmitting the command signal to at least one DDR memory device of the selected one or two

ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a

row access procedure and to transmit the stored input signal as an output signal of the set of output

signals during a subsequent column access procedure.

24.   (Original)   The memory module of claim 15, wherein the logic element

comprises an application-specific integrated circuit, a field-programmable gate array, a custom-

designed semiconductor device, or a complex programmable-logic device.

25.   (Original)   The memory module of claim 15, wherein the set of input signals

comprises a plurality of row/column address signals received and buffered by the register and sent

from the register to the plurality of DDR memory devices.

26.   (Amended)   [The memory module of claim 25] A memory module connectable to

a computer system, the memory module comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices, and

wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

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27.   (Original)   The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28.   (Amended)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

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a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select

signals of the output control signals in response at least in part to a bank address signal of the set of

input control signals.

29.   (Original)   The memory module of claim 28, wherein the logic element

comprises an application-specific integrated circuit, a field-programmable gate array, a

custom-designed semiconductor device, or a complex programmable-logic device.

30.   (Amended)   [The memory module of claim 29] A memory module connectable to

a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices

coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of

DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a

register, the logic element receiving a set of input control signals from the computer system, the set

of input control signals comprising a row/column address signal, bank address signals, a chip-select

signal, and an input command signal, the set of input control signals configured to control a second

number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR

DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks

smaller than the first number of ranks, the circuit generating a set of output control signals in

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response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device, and

wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

31.   (Original)   The memory module of claim 28, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

32.   (Original)   The memory module of claim 31, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

33.   (Amended)   [The memory module of claim 28] A memory module connectable to a computer system, the memory module comprising:

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a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the register receives the bank address signals and the input command signal of the set of input control signals.

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34.   (Original)   The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35.   (Original)   The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36.   (Original)   The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37.   (Original)   The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38.   (Original)   The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39.   (Amended)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank

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address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to a bank address signal of the set of input signals.

40.   (Original)   The memory module of claim 39, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

41.   (Original)   The memory module of claim 39, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

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42.   (Original)   The memory module of claim 39, wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices.

43.   (Original)   The memory module of claim 42, wherein the logic element receives the second number of chip-select signals.

44.   (Amended)   [The memory module of claim 43] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals,

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command signals, and the first number of chip-select signals, the at least one integrated circuit

element further responsive to the plurality of input signals by selecting at least one rank of the two

or more ranks and transmitting the plurality of output signals to at least one DDR memory device of

the selected at least one rank,

wherein the row address signals and the column address signals of the plurality of input

signals are received and buffered by the register and are sent from the register to the plurality of

DDR memory devices,

wherein the logic element receives the second number of chip-select signals, and

wherein both the register and the logic element receive the bank address signals and at least

one command signal of the plurality of input signals.

45.   (Original)   The memory module of claim 39, wherein two or more of the logic

element, the register, and the phase-lock loop device are portions of a single component.

46.   (Original)   The memory module of claim 39, wherein the plurality of DDR

memory devices is arranged as the first rank of DDR memory devices on the first side of the printed

circuit board, the second rank of DDR memory devices on the first side of the printed circuit board,

a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth

rank of DDR memory devices on the second side of the printed circuit board, the DDR memory

devices of the fourth rank spaced from the DDR memory devices of the third rank.

47.   (Original)   The memory module of claim 39, wherein the DDR memory devices

of the second rank are spaced from the DDR memory devices of the first rank in a direction along

the first side.

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48.   (Original)   The memory module of claim 39, wherein the plurality of DDR
memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the
second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of
the printed circuit board.

49.   (Original)   The memory module of claim 39, wherein the plurality of input
signals corresponds to a first memory density, and the plurality of output signals corresponds to a
second memory density, the second memory density greater than the first memory density.

50.   (Original)   The memory module of claim 39, wherein the at least one integrated
circuit element is configured to respond to the plurality of input signals by selecting at least one
rank of the two or more ranks and transmitting a command signal to at least one DDR memory
device of the selected at least one rank.

51.   (Amended)   [The memory module of claim 39] A memory module connectable to
a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board,
each DDR memory device comprising one or more banks, the plurality of DDR memory devices
arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one
integrated circuit element comprising a logic element, a register, and a phase-lock loop device
operationally coupled to the plurality of DDR memory devices, the logic element, and the register,
the at least one integrated circuit element receiving a plurality of input signals from the computer

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system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

52.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set

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of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

53.   (New) The memory module of claim 52, wherein the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR

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memory devices, the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register.

54.   (New) The memory module of claim 53, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation, wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device.

55.   (New) The memory module of claim 54, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

56.   (New) The memory module of claim 54, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the

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computer system, wherein the data characterizes the plurality of DDR memory devices as having

one or more attributes that are different from the one or more attributes of plurality of DDR memory

devices.

57.   (New) A memory module connectable to a computer system, the memory module

comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board,

the plurality of DDR memory devices having a first number of DDR memory devices arranged in a

first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a

register, the logic element receiving a set of input control signals from the computer system, the set

of input control signals comprising at least one row/column address signal, bank address signals,

and at least one chip-select signal, the set of input control signals corresponding to a second number

of DDR memory devices arranged in a second number of ranks, the second number of DDR

memory devices smaller than the first number of DDR memory devices and the second number of

ranks less than the first number of ranks, the circuit generating a set of output control signals in

response to the set of input control signals, the set of output control signals corresponding to the

first number of DDR memory devices arranged in the first number of ranks, wherein the circuit

further responds to a first command signal and the set of input control signals from the computer

system by generating and transmitting a second command signal and the set of output control

signals to the plurality of memory devices, the first command signal and the set of input control

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signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

58.   (New) The memory module of claim 57, wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory devices, and the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.

59.   (New) The memory module of claim 58, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

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60.   (New) The memory module of claim 58, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

61.   (New) The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

62.   (New) The memory module of claim 61, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

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63.   (New) The memory module of claim 62, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

64-66. (Cancelled)

67.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer

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system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

68.   (New) The memory module of claim 67, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device, wherein the memory module is operable for use in a server system.

69.   (New) The memory module of claim 67, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

70.   (New) The memory module of claim 67, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

71.   (New) The memory module of claim 67, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals

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received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

72.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

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a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to a first set of values of at least one address bit and the at least one chip-select signal of the set of input control signals by generating rank-selecting signals of the set of output control signals that select none of the first number of ranks for activation, and the logic element is further responsive at least in part to a second set of values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select two ranks of the first number of ranks for activation.

73.   (New) The memory module of claim 72, wherein the logic element is further responsive at least in part to values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for activation, and the logic element is further responsive at least in part to the values of the at least one address bit and the at least one chip-select signal by generating rank-selecting signals of the set of output control signals that select one rank of the first number of ranks for read or write access.

74.   (New) The memory module of claim 73, wherein the at least one address bit comprises a row address bit and a bank address bit.

75.   (New) The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR

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DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

76.   (New) The memory module of claim 75, wherein the DDR DRAM chip packages are DDR2 chip packages, DDR3 chip packages, or chip packages beyond DDR3 chip packages.

77.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of

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input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the at least one chip-select signal of the set of input signals by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals.

78.   (New) The memory module of claim 77, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

79.   (New) The memory module of claim 77, wherein the plurality of DDR memory devices and the logic element are timed to clock signals from the phase-lock loop device.

80.   (New) The memory module of claim 15, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as

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having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

81.   (New) The memory module of claim 80, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

82.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output

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command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element is responsive at least in part to the bank address signals and the chip-select signal of the set of input control signals by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

83.   (New) The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

84.   (New) The memory module of claim 82, wherein the plurality of DDR DRAM devices and the logic element are timed to clock signals from the phase-lock loop device.

85.   (New) The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only

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memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the

computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one

or more attributes that are different from the one or more attributes of the plurality of DDR DRAM

devices.

86.   (New) The memory module of claim 85, wherein the one or more attributes

comprise the number of ranks of DDR DRAM devices and the memory density per rank and the

data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM

devices than the plurality of DDR DRAM devices actually has, and as having a greater memory

density per rank than the plurality of DDR DRAM devices actually has.

87.   (New) A memory module connectable to a computer system, the memory module

comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board,

each DDR memory device comprising one or more banks, the plurality of DDR memory devices

arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one

integrated circuit element comprising a logic element, a register, and a phase-lock loop device

operationally coupled to the plurality of DDR memory devices, the logic element, and the register,

the at least one integrated circuit element receiving a plurality of input signals from the computer

system, the plurality of input signals comprising row address signals, column address signals, bank

address signals, command signals, and a second number of chip-select signals less than the first

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number of chip-select signals, wherein the logic element receives the bank address signals and at

least one command signal of the plurality of input signals, the at least one integrated circuit element

generating a plurality of output signals in response to the plurality of input signals, the plurality of

output signals comprising row address signals, column address signals, bank address signals,

command signals, and the first number of chip-select signals, the at least one integrated circuit

element further responsive to the plurality of input signals by selecting at least one rank of the two

or more ranks and transmitting the plurality of output signals to at least one DDR memory device of

the selected at least one rank,

wherein the logic element is responsive at least in part to the bank address signals and the

second number of chip-select signals of the plurality of input signals by generating the first number

of chip-select signals of the plurality of output signals that is greater than double or equal to double

the second number of chip-select signals of the set of input signals.

88.   (New) The memory module of claim 87, wherein the memory module is operable to

perform back-to-back adjacent read commands which cross DDR memory device boundaries.

89.   (New) The memory module of claim 87, wherein the plurality of DDR memory

devices and the logic element are timed to clock signals from the phase-lock loop device.

90.   (New) The memory module of claim 39, wherein the plurality of DDR memory

devices has one or more attributes selected from a group consisting of: a number of row address bits

per DDR memory device, a number of column address bits per DDR memory device, a number of

bank address bits per DDR memory device, a number of DDR memory devices, a data width per

DDR memory device, a memory density per DDR memory device, a number of ranks of DDR

memory devices, and a memory density per rank, the memory module further comprising a read-

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only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

91.   (New) The memory module of claim 90, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

92.   (New) The memory module of claim 1, wherein the memory module receives row/column address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to row/column address bits (A_0 - A_n), wherein the logic element operates in response at least in part to row/column address bit A_{n+1} and does not operate in response to the row/column address bits (A_0-A_n), and the register operates in response at least in part to the row/column address bits (A_0 - A_n) and does not operate in response to the row/column address bit A_{n+1}.

93.   (New) The memory module of claim 39, wherein the at least one integrated circuit element receives address bits (A_0 - A_{n+1}), and the DDR memory devices are responsive at least in part to address bits (A_0 - A_n), wherein the logic element operates in response at least in part to address bit A_{n+1} and does not operate in response to the address bits (A_0 - A_n), and the register operates in response at least in part to the address bits (A_0 - A_n) and does not operate in response to the address bit A_{n+1}.

94-108.   (Cancelled)

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109.   (New) The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

110.   (New) The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

111.   (New) The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

112-118.   (Cancelled)

119.   (New) The memory module of claim 2, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

120.   (New) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density.

121.   (New) The memory module of claim 1, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

122.   (New) The memory module of claim 1, wherein the register comprises a plurality of register devices.

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123.   (New) The memory module of claim 1, wherein the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

124.   (New) The memory module of claim 123, wherein the register receives and buffers the bank address signals and transmits the buffered bank address signals to the plurality of DDR memory devices, the phase-lock loop device transmitting clock signals to the plurality of DDR memory devices and to both the logic element and the register.

125.   (New) The memory module of claim 124, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation, wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device.

126.   (New) The memory module of claim 125, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column

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address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

127.   (New) The memory module of claim 125, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

128.   (New) The memory module of claim 1, wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

129.   (New) The memory module of claim 128, wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory

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devices, and the generation of the first number of chip-select signals of the output control signals by the logic element is responsive at least in part to the bank address signals.

130.   (New) The memory module of claim 129, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

131.   (New) The memory module of claim 129, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

132.   (New) The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

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133.   (New) The memory module of claim 132, wherein the command signal comprises a read command signal.

134.   (New) The memory module of claim 25, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

135.   (New) The memory module of claim 28, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

136.   (New) The memory module of claim 43, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

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STATUS OF CLAIMS

Pursuant to 37 C.F.R. §§ 1.530(e) and 1.941, and with entry of this Amendment, claims 1-63, 67-93, 109-111 and 119-136 are pending, with claims 64-66, 94-108 and 112-118 cancelled. The following sets forth in more detail the status of the claims, and an explanation of support for the changes is provided in Section XIV of the Remarks.

A.   Original Claims (Claims 1-51)

In this Amendment, the Patent Owner amends original independent claim 1 to include the recitation of allowable claim 66. Original independent claims 15, 28 and 39 have been similarly amended. Original dependent claims 2, 5, 7, 9, 16, 21, 23, 26, 30, 33, 44 and 51 have been placed in independent form. The remaining original dependent claims are also pending.

B.   Previously Added Claims (Claims 52-118)

Claims 52-118 were added in the previous response by the Patent Owner. In this Amendment, the Patent Owner places previously added claims 52, 57, 67, 72, 77, 82 and 87 in independent form. Claims 64-66, 94-108 and 112-118 have been cancelled. The remaining previously added claims are pending, with claims 92 and 93 amended.

C.   Newly Added Claims (Claims 119-136)

In this Amendment, the Patent Owner adds new claims 119-136.

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REMARKS

I.   Introduction

In the present reexamination of U.S. Patent No. 7,619,912 B2 (the '912 Patent), the Examiner issued a non-final Office Action on October 4, 2011. This Office Action, however, was superseded by a new Office Action on October 14 to take into account the comments of one of the Requesters. In the October 14 Office Action, the Examiner confirmed certain original dependent claims and found that certain previously added claims recited allowable subject matter.

The '912 Patent is currently the subject of two co-pending litigations that have been stayed. In an effort to expedite the reexamination and to simplify the issues, the Patent Owner hereby amends the claims based on the Examiner's indication of confirmed claims or allowable claims, with a few exceptions as discussed below, cancels some previously added claims without prejudice and adds new claims 119-136. Neither the amendments nor these Remarks should be in any way construed that the Patent Owner agrees or acquiesces to any of the rejections in the October 14 Office Action.

II.   Summary of Amendments

A.   Original Claims 1-51

In the October 14 Office Action, the Examiner found claim 66 to recite allowable subject matter. (*See, e.g.*, October 14 Office Action at 84.) The Patent Owner amends original independent claim 1 to recite the subject matter of claim 66. Original independent claims 15, 28 and 39 have been similarly amended.

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In addition, the Examiner confirmed original dependent claims 2, 5, 9, 16, 17, 21, 23, 30 and 51. The Patent Owner has placed these claims in independent form, with the exception of claim 17 as it depends from claim 16.

Original dependent claims 7, 26, 33 and 44 have also been placed in independent form. All of these claims stand rejected, which the Patent Owner respectfully traverses as discussed below.

The remaining original dependent claims depend from claims 1, 15, 28 or 39 and are not amended.

B.   Previously Added Claims 52-118

Based on the allowance of claim 66, it is believed that claims 52, 67, 77, 82 and 87 should also be allowed as discussed in more detail below. The Patent Owner has placed each of these previously added dependent claims in independent form.

The Examiner found claims 57 and 72 to recite allowable subject matter. (*See, e.g.*, October 14 Office Action at 84.) The Patent Owner has placed claims 57 and 72 in independent form.

The remaining previously dependent claims depend from claims 1, 15, 28, 39, 52, 57, 67, 72, 77, 82 or 87 and are not amended, except for claims 92 and 93. Previously added dependent claim 92 has been amended to recite "wherein the memory modules receives" as opposed to "wherein the set of input control signals includes," while claim 93 has been amended to recite "wherein the at least one integrated circuit element receives."

Finally, previously added claims 64-66, 94-108 and 112-118 have been cancelled without prejudice.

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C.   Newly Added Claims 119-136

The Patent Owner submits new claims 119-136. These claims are added to replace some of the dependent claims that have been placed in independent form. All the newly added claims depend from claims 1, 15, 28 and 39 and thus are allowable.

III.   **Ground 6**

In view of the above amendments, the Patent Owner will address each pending ground of rejection beginning with Ground 6.

A.   Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Amidi and JEDEC 21-C. (*See* October 14 Office Action at 18-20 and 22.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 31.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 10-14, 18-20, 22, 24, 25, 27, 29, 31, 32, 34, 36-38, 40-43 and 45-50 under Ground 6. The Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B.   Previously Added Claims

The Examiner rejected claim 52 under Ground 6. (*Id.* at 25-26.) The Patent Owner notes that claim 52 recites "the logic element is responsive at least in part to . . . the bank address signals . . . by generating a first number of chip-select signals of the set of output control signals . . . ." The Examiner cited his analysis of claim 1 for meeting this recitation. (*Id.* at 25.) The analysis of claim

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1, however, does not address any such recitation. Indeed, later in the October 14 Office Action, the Examiner expressly found that "Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals" with respect to claim 66. (*Id.* at 31.) The Patent Owner thus respectfully submits that claim 52 should have been allowed over Ground 6. Claim 52 has been placed in independent form.

The same conclusion applies to previously added claims 67, 77, 82 and 87 which have similar recitations as claim 52 with respect to the bank address signals. The Examiner cited his analysis of claim 52 for meeting the recitations of these claims. (*Id.* at 27-29.) The analysis of claim 52 which, in turn, refers to claim 1 is not sufficient as discussed above. The Patent Owner thus respectfully submits that claims 67, 77, 82 and 87 should have been allowed over Ground 6. These claims have been placed in independent form. Claims 68-71, 78, 79, 83, 84, 88 and 89 depend from claims 67, 77, 82 and 87 and are likewise patentable over Ground 6.

The Examiner further rejected previously added (and currently pending) claims 61-63, 75, 80, 81, 85, 86, 90, 91 and 109-111 under Ground 6. All these claims depend from claims 1, 15, 28 and 39. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 6 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

IV.   **Ground 9**

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Dell 1 and JEDEC 21-C. (*See* October 14 Office Action at 35-37 and 38.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 9. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 9 as to claims 1, 15, 28 and 39.

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The Examiner further rejected original dependent claims 3, 4, 6, 8, 18-20, 22, 24, 25, 27, 29, 31, 32, 36-38, 41-43, 45 and 50 under Ground 9. The Patent Owner respectfully requests that the Examiner withdraw Ground 9 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

V.   **Ground 11**

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Wong and JEDEC 21-C. (*See* October 14 Office Action at 42-45.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 11. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 11 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 18-20, 22, 24, 25, 27, 29, 31, 32, 36-38, 41, 42, 43, 45 and 50 under Ground 11. The Patent Owner respectfully requests that the Examiner withdraw Ground 11 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

VI.   **Ground 12**

A.   Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron and Connolly. (*See* October 14 Office Action at 48-50 and 52.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 58.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 12 as to claims 1, 15, 28 and 39.

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The Examiner further rejected original dependent claims 3, 4, 6, 8, 10, 11, 18-20, 22, 24, 25, 27, 29, 31, 32, 35-38, 41-43, 45 and 50 under Ground 12. The Patent Owner respectfully requests that the Examiner withdraw Ground 12 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B.   Claims 7, 26, 33 and 44

Original dependent claim 7 recites "wherein the bank address signals of the set of input control signals are received by both the logic element and the register." Claim 26 also recites the bank address signals being received by the logic element and the register: "wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system." Claim 33 recites "wherein the register receives the bank address signals and the input command signal of the set of input control signals" and claim 28, from which claim 33 depends, recites the logic element receiving bank address signals. Finally, claim 44 recites "wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals." In short, all four of these claims recite the register receiving bank address signals.

In the October 14 Office Action, the Examiner relied on Micron, particularly Fig. 4, for these claims. (*See* October 14 Office Action, at 51, 54 and 55.) The bottom of Fig. 4 of Micron discloses a single unit Register that is designated with U37 and U38 receiving 22 input signals. Because the Examiner relied on U37 and U38 as meeting the logic element and register limitations and both appear to receive 22 input signals, the Examiner concluded that the register also receives bank address signals as recited in claims 7, 26, 33 and 44. The Patent Owner respectfully disagrees.

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Micron discloses that the U37 and U38 designations refer to the SSTV16859 type which is compatible with JEDEC standard JESD82. (*See, e.g.*, Micron at Table 12 ("Register Specifications SSTV 16859 devices or equivalent JESD82-4B . . . Detailed Information for this register is available in JEDEC Standard JESD82.").) The cited JEDEC standard in turn defines each such register as a 13-bit registered buffer. (*See, e.g.*, JEDEC 82-4B, at page 1 and Fig. 1.) Therefore, Fig. 4 of Micron in fact refers to U37 and U38 as a single 22-bit register, as it takes two SSTV16859 registered buffers to register the 22 input signals (RAS, CAS, CKE0-1, WE, A0-A12, BA0-1, S0-1). Because each SSTV16859 can only register a portion of the 22 designated input signals, and nowhere does Micron describe which signals are registered by U37 versus U38, then Micron fails to disclose which of the 22 input signals are received by the logic element (U37), and which signals are received by the register (U38) to meet the claim recitation that the register receives bank address signals.

Even if one were to use input signals designations of Registers 1 and 2 of JEDEC 21-C, as shown on page 4.20.4-18 and referenced in Ground 6, to correspond to Micron's U37 and U38 registers respectively, then (i) the logic element (U37) would receive A0, A10, S0, S1, CAS, RAS, BA0, BA1, and WE which are associated with Register 2, and (ii) the register (U38) would receive A1-A9, A11, A12, CKE0, and CKE1 which are associated with Register 1. It is very clear that the Examiner's combination still would not result in a register that receives the bank address signals as clearly required by claims 7, 26, 33 and 44.

Therefore, the Patent Owner respectfully requests that the Examiner withdraw the rejection as to claims 7, 26, 33 and 44 under Ground 12.

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VII.   Ground 13

A.   Original Claims

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron and Amidi. (*See* October 14 Office Action at 60-62 and 64.) The Examiner did not adopt the rejection as to claim 66. (*Id.* at 74.) Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to claims 1, 15, 28 and 39.

The Examiner further rejected original dependent claims 3, 4, 6, 8, 10, 11, 18-20, 22, 24, 25, 27, 29, 31, 32, 34, 36-38, 41-43 and 45 under Ground 13. The Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

B.   Previously Added Claims

The Examiner rejected claim 52 under Ground 13. (*Id.* at 67.) The Patent Owner notes that claim 52 recites "the logic element is responsive at least in part to . . . the bank address signals . . . by generating a first number of chip-select signals of the set of output control signals . . . ." The Examiner cited his analysis of claim 1 for meeting this recitation. (*Id.* at 60 and 67.) The analysis of claim 1, however, does not address any such recitation. Indeed, later in the October 14 Office Action, the Examiner expressly found that "Amidi does not disclose that CAS or chip-select signals are generated in response to bank address signals" with respect to claim 66. (*Id.* at 74.) The Patent Owner thus respectfully submits that claim 52 should have been allowed over Ground 13. Claim 52 has been placed in independent form. Claim 53 depend from claim 52 and is likewise patentable over Ground 13.

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The same conclusion applies to previously added claims 67, 77, 82 and 87 which have similar recitations as claim 52 with respect to the bank address signals. The Examiner cited his analysis of claim 52 for meeting the recitations of these claims. (*Id.* at 70-71.) The analysis of claim 52 which, in turn, refers to claim 1 is not sufficient as discussed above. The Patent Owner thus respectfully submits that claims 67, 77, 82 and 87 should have been allowed over Ground 13. These claims have been placed in independent form. Claims 68-71, 78, 79, 83, 84, 88 and 89 depend from claims 67, 77, 82 and 87 and are likewise patentable over Ground 13.

The Examiner further rejected previously added (and currently pending) claims 61-63, 75, 76, 80, 81, 85, 86, 90, 91 and 109-111 under Ground 13. All these claims depend from claims 1, 15, 28 and 39. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 13 as to these claims at least in view of the amendment to claims 1, 15, 28 and 39.

C.   Claims 7, 26, 33 and 44

All four of these claims recite the register receiving bank address signals as discussed above. As with Ground 12, the Examiner again relied on Micron for disclosing this limitation in his analysis for Ground 13. (*See* October 14 Office Action at 63, 65 and 67.) Therefore, the Patent Owner respectfully requests that the Examiner withdraw the rejection as to claims 7, 26, 33 and 44 under Ground 13 for the reasons discussed above.

VIII.   **Grounds 14 and 15**

The Examiner rejected previously added claims 92-101 and 115-118 under § 112, first paragraph, for lack of written description, and claims 115-118 additionally for lack of enablement. (*See* October 14 Office Action at 76-78.)

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With respect to the rejection of claims 92 and 93, claim 92 has been amended to recite

"wherein the memory module receives" while claim 93 has been amended to recite "wherein the at

least one integrated circuit element receives." It is believed that these amendments overcome the

Examiner's rejection under Ground 14.

With respect to the rejection of claims 94-101 and 115-118, the Patent Owner has cancelled

these claims without prejudice in order to expedite the reexamination and to simplify the issues.

Thus, the rejections are moot. For clarity of record, the Patent Owner believes that these claims are

supported and enabled by the specification. For example, the specification specifically discloses

generating chip-select signals in at least Example 1 (spanning Columns 14-17), Fig. 1A (illustrating

generated chip-select signals) and at Col. 23, lines 18-24, which provides:

> In certain embodiments, the PLD 42 uses sequential and combinatorial logic
> procedures to produce the gated CAS signals which are each transmitted to a
> corresponding one of the four ranks 32, 34, 36, 38. In certain other embodiments,
> the PLD 42 instead uses sequential and combinatorial logic procedures to produce
> four gated chip-select signals (e.g., CS.sub.0a, CS.sub.0b, CS.sub.1a, and
> CS.sub.1b) which are each transmitted to a corresponding one of the four ranks
> 32, 34, 36, 38.

Nothing in this response should be construed that the Patent Owner agrees or acquiesces to

these rejections.

IX.   Ground 16

The Examiner rejected previously added claims 116-118 under § 112, second paragraph.

(*See* October 14 Office Action at 80.) These claims have been rejected without prejudice in order to

expedite the reexamination and to simplify the issues. Thus, the rejection is moot.

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X.   Ground 17

The Examiner rejected previously added dependent claim 76 as being obvious in view of Amidi, JEDEC 21-C and Vogt. (*See* October 14 Office Action at 83.) Claim 76 depends from claim 1 as amended. Neither the Requesters nor the Examiner challenged claim 66 under Ground 17. Moreover, the Examiner found claim 66 to be allowable over Amidi and JEDEC 21-C, and Vogt was not cited for the deficiencies of Amidi and JEDEC 21-C as to the recitation of claim 66. Accordingly, the Patent Owner respectfully requests that the Examiner withdraw Ground 17 as to claim 76 for at least this reason.

For clarity of record, the Patent Owner does not concede that Vogt is prior art to the claimed invention or that Vogt is a printed publication.

XI.   Ground 18

The Examiner rejected original independent claims 1, 15, 28 and 39 as being obvious in view of Micron, Connolly and Dell 2. (*See* October 14 Office Action at 83.) Neither the Requesters nor the Examiner challenged claim 66 under Ground 18. Given that claims 1, 15, 28 and 39 have been amended to recite the recitation of claim 66, the Patent Owner respectfully requests that the Examiner withdraw Ground 18 as to claims 1, 15, 28 and 39.

XII.   Response to Arguments

In the October 14 Office Action, particularly at pages 85-92, the Examiner made a number of statements, such as relating to the state of the art. The Patent Owner does not agree or acquiesce to these statements, and nothing in this response should be construed as agreeing or acquiescing to them. In fact, for clarity of record, the decision to not directly address in this Response any specific points, whether due to a claim cancellation or otherwise, does not indicate that Patent Owner agrees

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with or acquiesces to these specific points. The Patent Owner reserves its rights to seek or defend similar claims in related applications or patents, which may be in reexamination. Furthermore, the Patent Owner discusses above only some of the claim features of the '912 patent for the sake of brevity. These discussions should not be interpreted as Patent Owner asserting or acquiescing that the claims are not disclosed or rendered obvious because of only these features.

Finally, with respect to the secondary considerations analysis, the Examiner appears to require a nexus between the praise/acceptance and the "claimed features that are found to be obvious." (*See* October 14 Office Action at 85.) This is not the proper legal standard. Instead, what is required is a nexus between the merits of the claimed invention and the evidence of secondary considerations. (*See* MPEP 716.01(b).) In addition, "[t]o be pertinent to the issue of nonobviousness, the commercial success of devices falling within the claims of the patent must flow from the functions and advantages disclosed or inherent in the description in the specification." (*See* MPEP 716.03(b).) Here, at minimum, the claimed invention as a whole achieves the laudable properties provided by the HyperCloud product, as described in the previously submitted Lee and Lopes declarations.

XIII. Notice of Copending Proceedings

Pursuant to 37 C.F.R. § 1.985(a), the Patent Owner identifies the co-pending litigations styled *Netlist, Inc. v. Inphi Corporation*, Case No. CV-09-6900-DSF (RNBx), in the United States District Court for the Southern District of California, and *Google v. Netlist*, 4:08-cv-04144-SBA (CAND), in the Northern District of California. These actions were stayed on May 18, 2010 and January 11, 2011 pending the present reexaminations of three other related patents: U.S. Patent No. 7,289,386 being reexamined in reexaminations bearing control nos. 95/000,546 and 95/000,577

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(*Google* litigation only); U.S. Patent No. 7,532,537 being reexamined in the reexamination bearing control no. 95/001,381 (*Inphi* litigation only); and U.S. Patent No. 7,636,274 being reexamined in the reexamination bearing control no. 95/001,337 (*Inphi* litigation only).

In addition, the '912 Patent is related to following patents and pending applications: U.S. Patent No. 7,864,627 being reexamined in the reexamination bearing control no. 95/001,758; four newly issued patents, *i.e.*, U.S. Patent Nos. 8,072,837; 8,081,535, 8,081,536; and 8,081,537, as well as U.S. Patent Nos. 7,286,436, 7,881,150 and 7,916,574; and pending applications 12/912,623, 13/287,042 and 13/287,081.

XIV.   Explanation of Support for Claim Changes

With respect to the amendment to independent claims 1, 15, 28 and 39, support for the amendment can be found in the specification and drawings including, without limitation, at Col. 14, line 17 to Col. 19, line 53, Col. 22, lines 50-63, Col. 23, lines 6-25 and Figs. 3A and 3B.

With respect to claims 2, 5, 7, 9, 16, 21, 23, 26, 30, 33, 44, 51, 52, 57, 67, 72, 77, 82 and 87, all of these claims have placed into independent form. Thus, they have been changed by adding the recitations of independent claims 1, 15, 28 or 39 to them. The support for the recitations of the independent claims 1, 15, 28 and 39 can be found in the specification and drawings including, without limitation, at Col. 5, lines 6-36, Col. 6, lines 12-16 and 31-38, Col. 6, line 55 to Col. 7, line 34, Col. 7, lines 35 to Col. 9, line 21, Col. 11, line 43 to Col. 12, line 10, Col. 22, lines 15-63, Col. 23, lines 6-25, Col. 28, lines 25-32 and Figs. 1A, 1B, 3A, 3B, 11A and 11B.

With respect to claims 92 and 93, support for the changes to claims 92 and 93 can be found in the specification and drawings including, without limitation, at Col. 7, lines 39-41 and Figs. 1A and 1B.

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The Patent Owner respectfully submits new claims 119-136 for consideration with this Amendment. Almost all of these claims are added to replace some of the dependent claims that have been placed in independent form. All the newly added claims depend from claims 1, 15, 28 and 39 and thus are allowable for at least the reasons set forth above.

Claim 119 is identical to original claim 3, but depends from claim 2. Support for claim 119 can be found in the specification and drawings including, without limitation, at Col. 6, line 55 to Col. 7, line 19 and Figs. 1A and 1B.

Claim 120 depends from claim 1. Support for this claim can be found in the specification and drawings including, without limitation, at Col. 10, lines 49-55 and Col. 12, lines 12-15.

Claims 121 and 122 correspond to original dependent claims 7 and 9, which have been placed in independent form. Support for claims 121 and 122 can be found in the specification and drawings including, without limitation, at Col. 7, lines 50-53 for claim 121, and at Col. 5, lines 36-37 for claim 122.

Claims 123-127 depend from claim 1. The newly added dependent claims correspond to previously added dependent claims 52-56, as claim 52 has been placed in independent form. Support for claims 123-127 can be found in the specification and drawings including, without limitation, at the citations to the specification and drawings set forth at pages 21-22 of the Patent Owner's July 5 Response for claims 52-56 respectively.

Claims 128-131 depend from claim 1. The newly added dependent claims correspond to previously added dependent claims 57-60, as claim 57 has been placed in independent form. Support for claims 128-131 can be found in the specification and drawings including, without

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limitation, at the citations to the specification and drawings set forth at pages 22-23 of the Patent Owner's July 5 Response for claims 57-60 respectively.

Claims 132-134 depend from claim 15. The newly added dependent claims correspond to original dependent claims 16 and 26, which have been placed in independent form, and claim 17. Support for claims 132-134 can be found in the specification and drawings including, without limitation, at Col. 8, lines 50-54 for claim 132; Col. 8, lines 44-54 for claim 133; and Col. 7, lines 50-53 for claim 134.

Claim 135 depends from claim 28. The newly added dependent claim corresponds to original dependent claim 33, which had been placed in independent form. Support for claim 135 can be found in the specification and drawings including, without limitation, at Col. 21, lines 54-66 and Figs. 2A and 2B.

Claim 136 depends from claim 39. The newly added dependent claim corresponds to original dependent claim 44, which has been placed in independent form. Support for claims 136 can be found in the specification and drawings including, without limitation, at Col. 7, lines 50-53.

XV.   Conclusion

For the above reasons, the Patent Owner respectfully submits that the pending claims should be confirmed or allowed.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, the Patent Owner petitions for any required relief, including extensions of time, and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **635162800300.**

Dated: January 13, 2012

Respectfully submitted,

By_____

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR 1.903, the undersigned, on behalf of the Patent Owner, hereby certifies that a copy of the following documents:

1.   Transmittal dated January 13, 2012 (1 page); and
2.   Response/Amendment dated January 13, 2012 (66 pages, including this certificate of service);

was served on the Third Party Requesters via first class mail on January 13, 2012. The names and addresses of the parties served are as follows:

For Requester 95/000,578: Michael Heafey, Orrick, Herrington & Sutcliffe LLP, 1000 Marsh Road, Menlo Park, CA 94025.

For Requester 95/000,579: Hans Troesch, Fish & Richardson P.C., 500 Arguello Street, Suite 500, Redwood City, CA 94063.

For Requester 95/001,339: David A. Jakopin, Pillsbury Winthrop Shaw Pittman, LLP, P.O. Box 10500, McLean, VA 22012.

_____
Mehran Arjomand

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and
95/001,579
Patent 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges.*

POTHIER, *Administrative Patent Judge.*

DECISION ON APPEAL

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/001,579
Patent 7,619,912 B2

STATEMENT OF THE CASE

Requesters 1–3 made three separate requests for *inter partes* reexamination of U.S. Patent No. 7,619,912 B2 ("the '912 patent") issued to Jayesh R. Bhakta and Jeffrey C. Solomon, entitled *Memory Module Decoder*. The '912 patent issued November 17, 2009 and is assigned to Patent Owner, Netlist Inc. Requestor 1 requested reexamination of claims 1–51 of the '912 patent, which was assigned Control No. 95/001,339; Requester 2 requested reexamination of claims 1, 3, 4, 6–11, 15, 18–22, 24, 25, 27–29, 31–34, 36–39, 41–45, and 50 of the '912 patent, which was assigned Control No. 95/000,578; Requester 3 also requested reexamination of the same claims of the '912 patent as Requester 2, which was assigned Control No. 95/000,579. R1 Request 6; R2 Request 1; R3 Request 1.[1] On February 28, 2011, Control Nos. 95/001,339, 95/000,578 and 95/000,579 were merged into a single proceeding. Dec. *Sua Sponte* to Merge Reexamination Proc. 6.

Although indicating claims 1–136[2] are subject to reexamination in the RAN, the Examiner further states claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and

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[1] Throughout this opinion, we refer to (1) the Appeal Briefs filed by Requester 1, Requester 2, Requester 3, and Owner as R1 App. Br., R2 App. Br., R3 App. Br., and PO App. Br. respectively; (2) the Respondent Briefs filed by Owner (for Requesters 1–3), Requester 1, Requester 2, and Requester 3 as PO-R1 Resp. Br., PO-R2 Resp. Br., PO-R3 Resp. Br., R1 Resp. Br., R2 Resp. Br., and R3 Resp. Br. respectively ; (3) the Rebuttal Briefs by Requester 1, Requester 2, Requester 3, and Owner as R1 Reb. Br., R2 Reb. Br., R3 Reb. Br., and PO Reb. Br.; (4) the Examiner's Answer (Ans.) mailed January 14, 2015; (5) the Examiner's Right of Appeal (RAN) mailed June 18, 2014, (6) the Action Closing Prosecution (ACP) mailed March 21, 2014, and (7) Requests for Reexaminations by Requester 1, Requester 2, and Requester 3 as R1 Request, R2 Request, and R3 Request respectively.

[2] Claims 52-136 were added during the course of reexamination. *See* RAN 4.

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112–118 have been canceled. RAN 1. Accordingly, claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136 remain pending. Of those claims, claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119 have been rejected and claims 1, 3, 4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 are indicated as patentable. *Id.*

Requesters 1–3 appeal from the decision in the RAN not to adopt various rejections. R1 App. Br.; R2 App. Br.; R3 App. Br. Patent Owner filed respondent briefs. PO-R1 Resp. Br.; PO-R2 Resp. Br.; PO-R3 Resp. Br. Each Requester filed a rebuttal brief to their respective appeals. R1 Reb. Br.; R2 Reb. Br.; R3 Reb. Br.

Owner cross appeals from the decision in the RAN, rejecting claims 2, 5, 7, 21, 23, 26, 30, 33, and 119 of the '912 patent. PO App. Br. 2. Owner states that rejected claims 9 and 57 are not being appealed. PO App. Br. 47. Requesters 1–3 filed respondent briefs, and Owner filed a rebuttal brief. *See generally* R1 Resp. Br., R2 Resp. Br., R3 Resp. Br., and PO Reb. Br; *see also* Ans. 2.

The Examiner's Answer relies on the RAN, incorporating it by reference. *See* Ans. 1.

An oral hearing was conducted on November 24, 2015. A transcript has been made of record.

We have been informed that the '912 patent relates to (1) U.S. Patent Nos. 7,289,386, 7,532,537, 7,636,274, and 7,864,627 (the '386, '537, '274, and '627 patents, respectively), (2) merged reexamination Control Nos. 95/000,546 and 95/000,577 for the '386 patent, which was appealed to the Board as Appeal No. 2014-007777, and where the rejection of pending claims was affirmed on February

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25, 2015,[3] (3) reexamination Control No. 95/001,381 for the '537 patent, which was appealed to the Board as Appeal No. 2013-009066 and where the Examiner's decision to confirm the patentability of the claims was affirmed on January 16, 2014,[4] (4) reexamination Control No. 95/001,337 for the '274 patent, which has been reopened based on the Board decision dated January 16, 2014 (Appeal No. 2013-009044),[5] (5) reexamination Control No. 95/001,758 for the '627 patent, which was appealed to the Board as Appeal No. 2015-007761 and was heard on December 11, 2015, (6) various AIA proceedings, including IPR2014-00882, IPR2014-00883, and IPR 2014-01011,[6] and (7) several court proceedings.[7] R1 App. Br. 1; R2 App. Br. 2, 18; R3 App. Br. 1, 65; PO App. Br. 1.

We have jurisdiction under 35 U.S.C. §§ 134(b) and 315 (2002).

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[3] Subsequent to the decision, Patent Owner and Requester 3, Google Inc., filed notices of appeal to the Federal Circuit on October 26, 2015 and October 30, 2015, respectively. On February 15, 2016, the appeal was dismissed. *Netlist, Inc. v. Google Inc.*, Nos. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016).
[4] Subsequently, Requester appealed the Board decision to the Federal Circuit, which affirmed the Board's decision on November 13, 2015. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350 (Fed. Cir. 2015).
[5] On January 16, 2014, the Board affirmed-in-part and presented new grounds of rejection for various claims. The proceeding has been remanded to the Central Reexamination Unit.
[6] *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00882, Paper No. 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2), *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 8,081,536 B1), and *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-01011, Paper No. 34 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2).
[7] *Netlist, Inc. v. Inphi Corp.*, Case No. 2:09-cv-6900 (C.D. Cal.), *Netlist, Inc. v. Google, Inc.*, Case No. 4:09-cv-05718 (N.D. Cal.), and *Google, Inc. v. Netlist, Inc.*, Case No. 4:08-cv-04144 (N.D. Cal.), all stayed due to the reexamination proceedings of the '912, '537, and '274 patents.

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We affirm-in-part the Examiner's decision to reject or not to reject claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136.

Illustrative claims 7 and 21 read as follows with emphasis added:

7. [The memory module of claim 1] <u>A memory module connectable to a computer system, the memory module comprising:</u>
   <u>a printed circuit board;</u>
   <u>a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;</u>
   <u>a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and</u>
   <u>a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,</u> *wherein the bank address signals of the set of input control signals are received by both the logic element and the register.*

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21. [The memory module of claim 15] <u>A memory module
connectable to a computer system, the memory module comprising:</u>
<u>a printed circuit board;</u>
<u>a plurality of double-data-rate (DDR) memory devices coupled to
the printed circuit board, the plurality of DDR memory devices having
a first number of DDR memory devices arranged in a first number of
ranks;</u>
<u>a circuit coupled to the printed circuit board, the circuit comprising
a logic element and a register, the logic element receiving a set of
input signals from the computer system, the set of input signals
comprising at least one row/column address signal, bank address
signals, and at least one chip-select signal, the set of input signals
configured to control a second number of DDR memory devices
arranged in a second number of ranks, the second number of DDR
memory devices smaller than the first number of DDR memory
devices and the second number of ranks less than the first number of
ranks, the circuit generating a set of output signals in response to the
set of input signals, the set of output signals configured to control the
first number of DDR memory devices arranged in the first number of
ranks, wherein the circuit further responds to a command signal and
the set of input signals from the computer system by selecting one or
two ranks of the first number of ranks and transmitting the command
signal to at least one DDR memory device of the selected one or two
ranks of the first number of ranks; and</u>
<u>a phase-lock loop device coupled to the printed circuit board, the
phase-lock loop device operatively coupled to the plurality of DDR
memory devices, the logic element, and the register,</u> *wherein the
circuit is configured to store an input signal of the set of input signals
during a row access procedure for subsequent use during a column
access procedure.*

PO App. Br. 51–54, Claims App'x.[8]

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[8] Underlining in claims indicates added language present in originally issued
independent claims 1 and 15 respectively.

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The Invention

The '912 patent illustrates an exemplary memory module 10 in Figure 1A below:
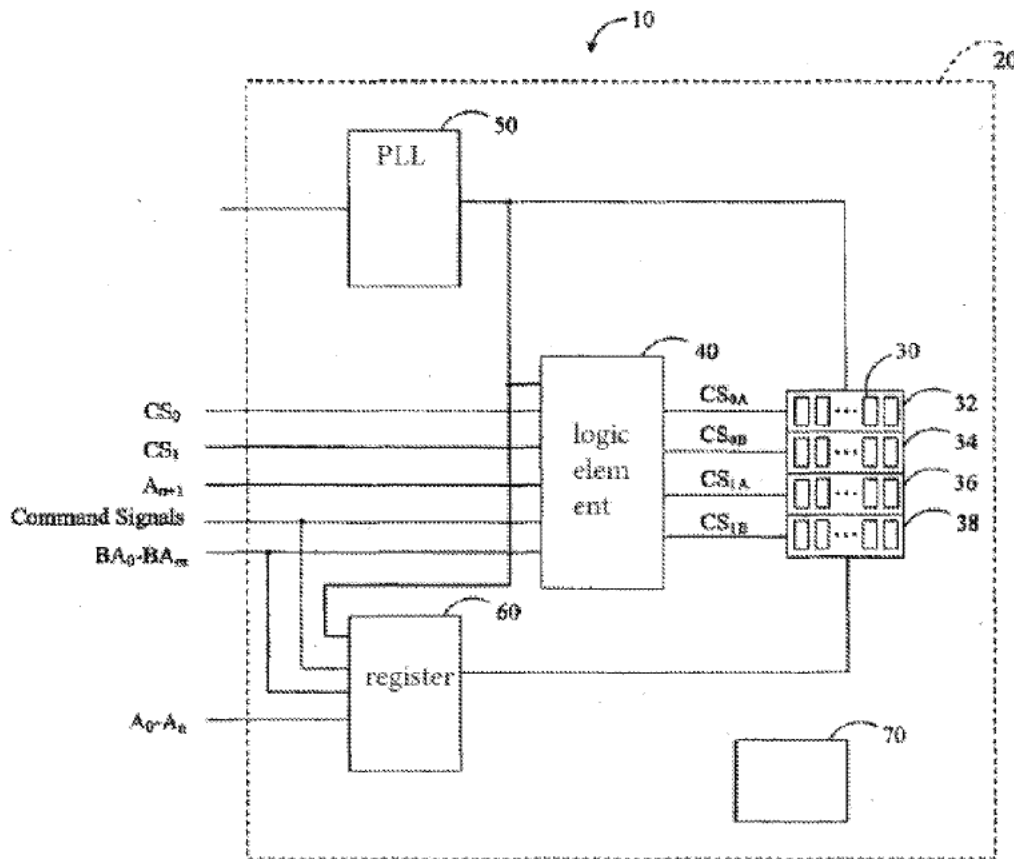
Annotated Memory Module illustrated in Figure 1A

The '912 patent 3:32–34, 5:6–8; Fig. 1. Memory module 10 contains printed circuit board 20. Memory devices 30, phase lock loop (PLL) 50, logic element 40, and register 60 are coupled to printed circuit board 20. The '912 patent 5:13–14, 22–27; Fig. 1A.

Memory devices 30 are a first number of memory devices (e.g., 4 DDR devices). The '912 patent 5:11–12, 6:12–16; Fig. 1A. The logic element 40

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receives input control signals that correspond to a second number of memory devices smaller than the first number of memory devices (e.g., 2). The '912 patent 2:37–39, 5:14–20; Fig. 1A. Input control signals includes address signals, such as bank address signals (e.g., BA_0-BA_m), row address signals, column address signals, gated column address strobe signal, and rank or chip-select signals (e.g., CS_0 and CS_1), and command signals (e.g., refresh and precharge). The '912 patent 2:37–39, 6:56–61; Fig. 1A. Logic element 40 generates output control signals (e.g., CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) in response to the input control signals, the output control signals corresponding to the first number of memory devices (e.g., 4). The '912 patent 5:18–21; Fig. 1A.

Additionally, in certain embodiments, the output control signals correspond to a first number of ranks (e.g., 4) in which the memory devices 30 are arranged. The '912 patent 6:55–67, 7:36–38. On the other hand, the input control signals correspond to a second number of ranks (e.g., 2) per memory module, for which the computer system is configured. The '912 patent 6:67–7:9, 7:20–29, 38–39; Fig. 1A. The second number of ranks is smaller than the first number of ranks. *See id.* In such a scenario, memory module 10 simulates a virtual memory module, and this may occur when the number of memory devices 30 of memory module 10 is larger than the number of memory devices 30 per memory module the computer system is configured to use. The '912 patent 7:9–19. This arrangement can improve memory module performance, capacity, or both. The '912 patent 1:21–24.

As shown above in Figure 1A, the bank address signals, $BA_0 - BA_m$, are received by both register 60 and logic element 40.

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In addition, Figure 2B shows that logic element 40 can save or latch an input control signal (e.g., A_{13}) during a row access procedure (e.g., column access strobe (CAS) high) at program logic device (PLD) 42 and can transmit this signal as an output control signal during a subsequent column access procedure (e.g., CAS low). The '912 patent 21:54–66; Fig. 2A. Figure 2B illustrates this below:
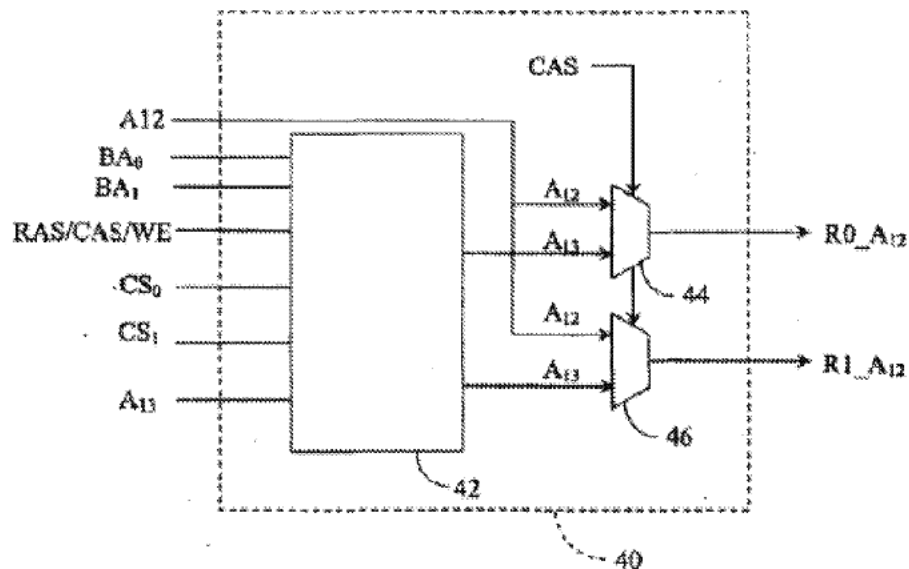
Figure 2B showing Logic Element 40 with PLD 42 Storing Signals

The '912 patent 3:44–45; Fig. 2B. In this exemplary logic element, ranks 32 and 34 (shown in Figure 2A) interpret the previously-saved row address (e.g., A_{13}) as a current column address (e.g., A_{12}), and logic element 40 translates the extra row address into an extra column address. The '912 patent 21:66–22:4; Fig. 2A–B.

Cited Prior Art

The Examiner relies on the following as evidence of unpatentability:

Connolly	US 5,745,914	Apr. 28, 1998
Dell (Dell 1)	US 5,926,827	July 20, 1999
Dell (Dell 2)	US 6,209,074	Mar. 27, 2001

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Olarig	US 6,260,127 B1	July 10, 2001
Wong	US 6,414,868 B1	July 2, 2002
Dell (Dell 184)	US 6,446,184 B2	Sept. 3, 2002
Amidi	US 2006/0117152	June 1, 2006
		(filed Jan. 5, 2004)

Miles J. Murdocca and Vincent P. Heuring, Principles of Computer Architecture (Chapter 7) 243–252 (2000) (Murdocca)

Micron, *DDR SDRAM RDIMM, MT36VDDF12872 - 1GB, MT36VDDF25672 - 2GB* 1–20 (2002) (Micron)

JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C)

JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C (Rev. of JESD79B) 1–75 (Mar. 2003) (JEDEC 79C)

JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A) 1–12 (May 2003) (JEDEC 82-4B)[9]

HP Printer Memory Explained 1–7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained)

> The following Declarations are presented in this merged proceeding:
>
> Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),
>
> Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),
>
> Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),
>
> Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),
>
> Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

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[9] Notably, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

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Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.), and

Declaration of Dr. Bruce Jacob dated October 19, 2010.

Adopted Rejections

Patent Owner appeals the following rejections adopted by the Examiner:

Reference(s)	Basis	Claims	RAN
Amidi (Ground 3[10])	§ 102	2, 5, 7, 9, 21, 23, 30, 33, and 119	11, 22–26

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[10] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters 1–3 refer to the various rejections by ground number. *See, e.g.,* RAN 11. We include the ground number here and in the Opinion.

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Amidi (Ground 4)	§ 103(a)	2, 5, 7, 9, 21, 23, 30, 33, 57, and 119	12, 28
Amidi and Dell 2 (Ground 5)	§ 103(a)	2, 5, 7, 9, 21, 23, 26, 30, and 33	12, 30
Amidi and JEDEC (Ground 6)	§ 103(a)	7, 9, 21, 33, 57, and 119	12, 32–33
Dell 1 and JEDEC (Ground 9)	§ 103(a)	9 and 21	RAN 13, 36–39
Wong and JEDEC (Ground 11)	§ 103(a)	9 and 21	RAN 13, 41–43
Micron and Connolly (Ground 12)	§ 103(a)	7, 9, 21, 26, and 33	RAN 13, 44–47
Micron and Amidi (Ground 13)	§ 103(a)	7, 9, 21, 26, 33, and 57	RAN 14, 49–52
Micron, Amidi, and Dell 2 (Ground 19)	§ 103(a)	21	RAN 14, 55

PO App. Br. 11.

ISSUES ON APPEAL

We review the appealed rejections for error based upon the issues identified by Owner in its appeal brief, and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)). "Any arguments or authorities not included in the brief[s] permitted under this section or [37 C.F.R.] §§ 41.68 and 41.71 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.67(c)(1)(vii).

Based on the arguments and evidence presented by Owner, the main issues on appeal are whether the Examiner erred in determining:

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(I) Amidi alone or in combination with at least one other reference (Grounds 3–6) disclose or teach:

(A) "the bank address signals of the set of input control signals are received by both the logic element and the register" recited in claim 7 and similarly recited in claims 26 and 33 (bank address limitation)?

(B) "wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure" recited in claim 21 and similarly recited in claims 2, 5, 23, and 30 (storing limitation)?

(II) Micron and Amidi (Ground 13) teach

(A) the bank address limitation recited in claim 7 and similarly recited in claims 26 and 33?

(B) the storing limitation recited in claim 21?

(III) the proposed rejections of certain claims should not be adopted?

ANALYSIS

Patent Owner's Appeal

Preliminary Matters

Patent Owner states it "is not appealing the rejections of claims 9 and 57." PO App. Br. 47; R3 Resp. Br. 1. These claims have been rejected under Grounds 3–6, 9, and 11–13. RAN 11–14. Because no arguments have been presented for these claims, we summarily sustain the rejections of these claims. *See Hyatt v. Dudas*, 551 F.3d 1307, 1314 (Fed. Cir. 2008) (explaining that when appellant fails to contest a ground of rejection, the Board may affirm the rejection without considering its substantive merits).

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Claim Construction

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations and internal quotation marks omitted). We presume that claim terms have their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning 'is the meaning that the term would have to a person of ordinary skill in the art in question.'") (internal citations omitted). However, patentees may rebut this presumption by acting as their own lexicographer, providing a definition of the term in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Claims 2, 5, 7, 21, 23, 26, 30, and 33 recite a circuit comprising "a logic element." The '912 patent states that logic element 40 in certain embodiments can be a PLD, an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex PLD (CPLD). The '912 patent 6:39–43. The '912 patent also describes the logic element in certain embodiments as "a custom device," "compris[ing] various discrete electrical elements," or being "one or more integrated circuits" in certain embodiments. The '912 patent 6:43–44, 48–52. As such, the '912 patent describes "a logic element" in expansive terms, but none of the above passages define or limit the meaning of "logic element" with sufficient precision.

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The Examiner similarly determines the '912 patent has not defined "a logic element" and further finds this phrase is not a term of art. RAN 69. The Examiner thus construes the phrase "logic element" to have its plain meaning to include "an element that performs some kind of logic function or an element that comprises a logic circuit." *Id.* Requester 1 proposes that one skilled in the art would have understood a logic element "to mean any circuit that implements one or more logic functions using combinational or sequential logic functions. [*See* Declaration of David Wang, Ph.D., filed Aug. 29, 2011 ("1st Wang Decl.", attached as Exhibit B-1) at ¶¶ 7, 30]." R1 Resp. Br. 5. Requester 2 also proposes an interpretation of "logic element," urging that is "at least as broad" as Patent Owner proposed in litigation. R2 Request 22 (citing R2 Request, Evid. App., Ex. OTH-C 7). In that context, Patent Owner urged "a logic element" to mean a "hardware circuit that performs a predefined function on input signals and presents the resulting signal as its output." *Id.*

Given the record and that the '912 disclosure fails to define the term, we accept the Examiner's understanding of "a logic element" as reasonable, which includes "an element that performs some kind of logic function or an element that comprises a logic circuit." RAN 69. This understanding is consistent with the expansive discussion in the '912 patent that includes a "custom device" or a generic device comprising "various discrete electrical elements." The '912 patent 6:43–44, 48–50.

The Examiner also states "there is nothing in the claims or the specification that precludes the logic element from comprising a storage device such as a register." RAN 69. Notably, each of claims 2, 5, 7, 21, 23, 26, 30, and 33 recites "a register" separate from "a logic element." This distinction in claim language

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presumably supports that the recited "logic element" is something different from a register. Both the Examiner and Dr. Sechen also note they "are separate elements in the claims." RAN 69, 74; Sechen Decl. ¶ 20. Dr. Sechen further argues that one skilled in the art "would understand that the term 'logic element' implies something inherently different than the term 'register.'" Sechen Decl. ¶ 19.

We agree that the recited "logic element" is distinct element from the recited "register." RAN 69, 74. However, the expansive examples in the '912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers. Requester 1 also provides the testimony of Dr. Wang, supporting that a register performs logical operations and is a logical element. R1 Resp. Br. 5 (citing Wang Decl. ¶ 7). That is, Dr. Wang testifies that "[r]egisters are logic elements," because they implement one or more logic functions (e.g., AND, NAND, OR, NOR, etc.). Wang Decl. ¶ 7. Also, even Dr. Sechen, Patent Owner's own expert, admits that a register includes "a small amount of control logic" (Sechen Decl. ¶ 19), indicating that registers perform some type of logic function or comprise a logic circuit.

Accordingly, we determine that a reasonably broad interpretation of "a logic element," in light of the '912 patent's disclosure and the testimony of what one of ordinary skill in the art would have understood, includes custom devices and devices with various discrete electrical components that implement logic operations, including registers. We further determine the recited "logic element" is also not limited to a single component, given that the disclosure states the logic element can comprise various discrete electrical components.

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I. Amidi

Patent Owner argues the Examiner erred in adopting the proposed rejections based on Amidi, separately arguing the claims in two groups — (1) claims with the bank address limitation (i.e., claims 7, 26, and 33) and (2) claims with the storing limitation (i.e., claims 2, 5, 21, 23, and 30). PO App. Br. 11. We in turn will address each group separately.

A. Claims 7, 26, and 33 (Claims with the Bank Address Limitation)

Patent Owner argues claims 7, 26, and 33 as a group. PO App. Br. 12–25. As addressed below, claim 26 is only rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5) and we only address claim 26 for that rejection. To the extent these claims are argued together, we select claim 7 as representative. 37 C.F.R. § 41.67(c)(1)(vii).

Claim 7 recites, in pertinent part, that a "memory module comprising . . . a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising . . . bank address signals, . . . the bank address signals of the set of input control signals are received by both the logic element and the register."

1. Anticipation Rejection – Ground 3

The Examiner indicates that both Requester 1 and Requester 2 present a rejection under 35 U.S.C. § 102 based on Amidi for claims 7 and 33. RAN 11, 22, 24, 25; *see also* R1 February 13, 2012 Comments 6–12 and R2 Request 39, 943–961, 965–969, 1025–1026 (referring to Ex. CC–G). The Examiner adopted the proposed rejection of Requesters 1 and 2 for claims 7 and 33. RAN 11, 22–26.

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Specifically, the Examiner maps register 418 in Amidi's Figure 4B to the recited "register" and CPLD 410 and register 408 in Amidi's Figure 4A to the recited "logic element." RAN 23[11]; R1 February 13, 2012 Comments 2–12, 27–28 (referring to R1 Request). Based on our construction of "logic element" discussed above, we do not find error in the mapping of register 418 in Amidi to the recited "register" and register 408 to the separately recited "logic element" (RAN 23) given that a register performs some amount of logic (Sechen Decl. ¶ 19). Contrary to Patent Owner's contentions (PO App. Br. 17–18), we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited "logic element." By its very name (i.e., Complex Programmable Logic Device), CPLD 410 discloses that it performs logical operations. Moreover, as discussed above, a "logic element" can comprise various discrete electrical components.

As to whether "Figure 6" of Amidi discloses that both registers (e.g., 408, 418) receive bank address signals, Amidi shows bank address signals are received by register 608 (e.g., BA[1:0]) in Figure 6A. *See* RAN 24 (stating "registers 408 and 418, shown as 608 in Figure 6, receive BA signals."). Patent Owner argues that Amidi fails to teach bank address signals are received by both a register and a logic element, arguing Amidi teaches receiving the bank address signals only at a single register for passing to the DDR memory devices. PO App. Br. 14–15; PO Reb. Br. 4; *see* 2d Sechen Decl. ¶ 18.

Patent Owner's position is grounded in what Patent Owner contends one skilled in the art would have understood given Amidi's disclosure. That is, during

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[11] Although this portion of the RAN discusses claim 5, claim 7 includes the same limitation of a "circuit comprising a logic element and a register." *Compare* PO App. Br. 50, Claims App'x., *with* PO App. Br. 51, Claims App'x.

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examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad.*, 367 F.3d at 1364 (citations and internal quotation marks omitted). Patent Owner argues that one skilled in the art would have interpreted Amidi's figures (e.g., Figs. 6A–B) based on industry standards, namely JEDEC. PO App. Br. 13–15, 18–21 (citing JEDEC 79C 6–7 and 11–12; JEDEC 21-C 4.20.4–16, 4.20.4–18, and 4.20.4-33; 2d Sechen Decl. ¶¶ 18–23, 34–36, 40, 42–46; 2d Bagherzadeh Decl. ¶ 31; and 3d Bagherzadeh Decl. ¶¶ 8, 42, 43); PO Reb. Br. 6–8 (citing JEDEC 21-C; 2d Sechen Decl. ¶¶ 34–54; Wang Decl. ¶ 9; 2d Bagherzadeh ¶ 31; 3d Bagherzadeh Decl. ¶¶ 8, 42, 43; Jacob Decl. ¶ 19; and 4th Kozyrakis Decl. ¶ 19).

Specifically, Patent Owner contends that "[s]tandards set the default position in an industry" (PO Reb. Br. 9) and "a POSITA's [person of ordinary skill in the art's] default position would be to understand Amidi's registers in light of [the] JEDEC specification, including JEDEC 21-C." PO Reb. Br. 10. Where Amidi is silent concerning its memory module design, in Patent Owner's view, an ordinarily skilled artisan "would begin with JEDEC reference designs to achieve a JEDEC-compliant memory module." PO Reb. Br. 9.

Patent Owner contends that JEDEC 21-C shows only one register (e.g., Register 2) receiving the bank address signal. PO App. Br. 14 (citing JEDEC 21-C 4.20.4-18). Requester 1 disagrees, arguing that both register 408 and register 418 receive bank address signals.[12] R1 Resp. Br. 6–7. Requester 1 asserts that Amidi

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[12] Patent Owner asserts that the anticipation rejection was not opposed by Requester 1, because Requester 1 focuses on the obviousness rejection based on Amidi. PO Reb. Br. 14; R1 Resp. Br. 9. However, Requester 1's discussion

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is not strictly JEDEC-compliant. R1 Resp. Br. 7–8, 10 (citing 3d Wang Decl. ¶ 17). Requester 2 notes that the Examiner correctly found that Amidi discloses both a register and a logic element receiving bank address signals. R2 Resp. Br. 5–6 (citing RAN 26).[13] Specifically, Requester 2 asserts that both registers 408 and 418 in Amidi receive bank address signals. R2 Resp. Br. 6 (citing Amidi, Fig. 6A). Requester 3 does not specifically address the anticipation rejection of Amidi. R3 Resp. Br. 4.

Amidi shows bank address signals are received by register 608 (e.g., BA[1:0]) in Figure 6A. Amidi, Fig. 6A. Unlike the address signals (A0-A11) that Amidi explicitly states are received by both registers 408 and 418 (Amidi ¶ 49), the accompanying disclosure in Amidi does not discuss whether the bank address signals are also received by both registers 408 and 418 shown in Figures 4A and B. *See* Amidi ¶¶ 49–52. Rather, one must infer from Amidi's Figures 6A and 6B that both registers 408 and 418 receive bank address signals. Amidi also fails to describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD 410 or 604. *See* Amidi, Figs. 4A–B, 6A–B.

As stated,

> If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is "inherent" in its disclosure. . . . "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."

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addresses what Amidi discloses. *See, e.g.,* R1 Resp. Br. 6–7, 8–10. In essence, Requester 1 has argued that Amidi anticipates various recited features of the claims. *Id.* Moreover, Requester 2 echoes Requester 1's position. R2 Resp. Br. 5–6.

[13] Requester 2 failed to include page numbers in the respondent brief. We refer to the page numbers sequentially as submitted.

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In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999) (internal citations omitted). We thus turn to other evidence in the record, such as the JEDEC standards and expert testimony, to determine whether receiving bank address signals at both registers 408 and 418 would have been an inherent feature that would necessarily flow from the teachings in Amidi.

Amidi refers to JEDEC standard only when discussing "defined height limits" (Amidi ¶ 7) and does not discuss any other JEDEC design specifications. Dr. Wang states Amidi's devices and modules "are not restricted to JEDEC specifications-compliant devices and modules" and that the '912 patent, like Amidi, deviates from JEDEC standards by using, for example, twice as many DRAM devices in its arrangement. 3d Wang Decl. ¶¶ 17–18. That is, Amidi also discusses creating a transparent four rank memory module that fits into a memory socket having two chip select signals. Amidi ¶¶ 11–12. On the other hand, Dr. Bagherzadeh states "Amidi discloses JEDEC compliant DIMMs [dual in-line memory module]." 3d Bagherzadeh ¶ 43. But, Dr. Bagherzadeh also states that an ordinary artisan would understand Amidi's DIMMs "conform to standards authored by JEDEC" without indicating to which "standards" Amidi conforms. *See* 2d Bagherzadeh ¶ 31. Weighing the evidence, we agree with Requester 1 that Amidi is not compliant with all of the design specifications set forth for memory module design of JEDEC 21-C.

Even so, Amidi fails to discuss whether both registers 408 and 418 necessarily receive bank address signals. We thus turn to the JEDEC 21-C specification and the testimony of record for any insight as to whether both registers receiving bank address signals is an inherent feature of Amidi.

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Dr. Sechen indicates that JEDEC 21-C is a design specification for DDR SDRAM (synchronous dynamic random access memory) registered DIMMs, including 72-bit registered DIMMs using 36 stacked memory devices arranged in four ranks. 2d Sechen Decl. ¶¶ 18–19 (citing JEDEC 21-C, 4.20.4-16, 4.20.4-18). Amidi in Figure 4A and B also describes a 72-bit registered DDR module, but the record does not indicate clearly whether the cited portions of JEDEC 21-C are directed to a 72-bit embodiment. *Compare* Amidi ¶¶ 37, 42, Figs. 4A–B (describing "Transparent 72-bit Registered DDR Module") *with* JEDEC 21-C, 4.20.4-16 (discussing two physical banks of x4 DDR SDRAMs (synchronous dynamic random access memory)). Even so, the JEDEC 21-C embodiments, including 72-bit embodiments, repeatedly show a single register box receiving the bank address signals (e.g., BA0-BA1). JEDEC 21-C, 4.20.4-10–4.20.4-16. Moreover, concerning the register functional assignments, all the raw card versions in the JEDEC specification show two registers (e.g., Register 1 and Register 2) but only one register (e.g., Register 2) receiving the input bank address signals (e.g., BA0 and BA1). JEDEC 21-C, 4.20.4-18, *reproduced at* 2d Sechen Decl. ¶ 19.

Given the above discussion of JEDEC 21-C, Dr. Sechen asserts that the register function, like that in register 608 in Figure 6A, is shown as a single box but that the register box is implemented using one or two registers. 2d Sechen Decl. ¶ 19. In the two register case, Dr. Sechen testifies that the JEDEC 21-C design specification uses only one of the two registers to receive the input bank address signals. *Id.* ¶¶ 19–21 (citing JEDEC 21-C, 4.20.4-18 and 4.20.4-22). We agree. Similarly and because Amidi does not discuss explicitly whether bank address signals are received by both registers 408 and 418, the record reflects the possibility that Amidi's two registers (e.g., registers 408, 418) may function as a

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single register box, such as that shown in JEDEC 21-C. We thus determine that Amidi does not anticipate the bank address recitation of claim 7.

Regarding Amidi's CPLD, Patent Owner further contends that the bank address signals in Amidi are not passed to the CPLD of Amidi. PO App. Br. 16. Patent Owner states that address signals (e.g., Add(n) in Fig. 6A) are received by CPLD (e.g., 604), but these signals are not *bank* address signals (e.g., BA[1:0]). PO App. Br. 17; *See* PO Reb. Br. 5. Rather, they are, in Patent Owner's view, row/column address signals, which are separately recited in claim 7 and which are separately described and shown in Amidi. *See* Amidi ¶¶ 49–51, Fig. 6A. We agree. Accordingly, the Examiner has not demonstrated that Amidi necessarily discloses a register (e.g., 418) and a logic element (e.g., register 408 alone or register 408 and CPLD 410 collectively) receiving bank address signals as recited in claim 7.

On the other hand, Requester 2 points out that claim 33 differs in scope from claim 7. *See* R2 Resp. Br. 6. We agree. Namely, claim 33 does not require both a logic element and a register to receive the input bank address signals, rather *only* "the register receives the bank address signals." *Id.* As discussed above, Amidi discloses a register receiving the bank address signals (*see* R1 Request 148 (citing Amidi ¶ 50, Fig. 6A))— a finding undisputed by Patent Owner. *See* PO App. Br. 15.

For the above reasons, under 35 U.S.C. § 102, we determine that the Examiner erred in rejecting claim 7 and but did not err in rejecting claim 33 based on Amidi.

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2. *Obviousness Rejection Based on Amidi Alone or Amidi and JEDEC — Grounds 4 and 6*

We next consider whether Amidi renders obvious to one of ordinary skill in the art that (1) both registers 408 and 418 receive bank address signals or (2) one of register 408 or 418 and CPLD 410 receive bank address signals. The Examiner states that claims 7 and 33 are rejected under 35 U.S.C. § 103, "[b]ecause these claims are anticipated by Amidi." RAN 28. As previously stated, we agree claim 33 is anticipated by Amidi. Thus, we further agree with the Examiner that claim 33 is obvious. *See In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002) (citations omitted) (indicating that anticipation is the epitome of obviousness).

Regarding claim 7, the Examiner does not discuss features missing from Amidi or what in Amidi renders the claim obvious. The rejection refers to proposed rejections presented by Requesters 1 and 2 and thus relies on the proposed analysis for these grounds. RAN 12 (referring to proposed rejections of Requesters 1 and 2 and "modified 2/13/13"), 61–62 (stating Requester 1's Comments filed February 13, 2013[14] related to claim 7 and 33 are convincing), and RAN 74 (stating "Requesters' (both 1 and 2) argument that Amidi discloses a logic element . . . is persuasive.") Requester 1 discusses that one skilled in the art would have recognized various memory modules that do not follow JEDEC standards. R1 February 13, 2013 Comments 4–5 (referring to 3d Wang Decl. ¶¶ 18–19); *see*

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[14] Requester 1 filed comments both on February 13, 2012 (previously discussed) and February 13, 2013. Requester 2 also filed comments on February 13, 2012 and February 13, 2013. Requester 2's February 13, 2013 Comments were found defective, and corrected comments were subsequently filed on August 14, 2013. Requester 3 filed comments on February 23, 2012.

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also February 13, 2012 Comments 4–5 (referring to 2d Wang Decl.), 15–19, 28–29, 41 (referring to claim charts in R1 Request).

Patent Owner contends there is no suggestion in Amidi (1) to make each of registers 408 and 418 into register 608 or (2) to duplicate the register function. PO App. Br. 21–23 (citing 2d Sechen Decl. ¶ 46); PO Reb. Br. 5–6, 10–12. Patent Owner admits that Amidi instructs ordinarily skilled artisans to deviate from JEDEC design specifications where expressly disclosed. PO Reb. Br. 9. But, Patent Owner contends "where Amidi does not expressly instruct a POSITA to depart from JEDEC reference designs, a POSITA—familiar with relevant JEDEC standards—would begin with JEDEC reference designs to achieve a JEDEC-compliant memory module." *Id.* Patent Owner also asserts one would closely adhere to these standards to avoid "operational failure." PO App. Br. 29.

Requester 1 disagrees, asserting that a skilled artisan "was not limited to constructing JEDEC compliant modules," including "dimensional and power requirements." R1 Resp. Br. 8 (citing 3d Wang Decl. ¶ 17). Requester 1 also argues that one skilled in the art would have known of the existence of "multitudes of memory modules . . . that did not follow JEDEC specifications." R1 Resp. Br. 8; *see* R1 Resp. Br. 9 (citing Wang Decl. ¶¶ 17–21 and 3d Wang Decl. ¶¶ 17–19).

Before we determine what Amidi suggests, we must resolve the level of skill in the pertinent art. *See Graham v. John Deere Co.*, 383 U.S. 1, 11 (1966). Requester 1 states that the level of skill "was high," but provides no further details describing the skill level. R1 Resp. Br. 4 (referring in general to the Wang Declarations); *see generally* Wang, 2d Wang, and 3d Wang Decls. Dr. Bagherzadeh states

> the level of skill in the art related to the '912 patent in my opinion is a
> person with a degree in either electrical or computer engineering or in

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> a closely related discipline, and at least 1-2 years of experience in designing computer memory systems and would have an understanding of industry standards adopted by Joint Electronic Devices Engineering Council (JEDEC).

Bagherzadeh Decl. ¶ 16; 3d Bagherzadeh Decl. ¶ 10. Dr. Kozyrakis states he believes

> a person of ordinary skill in the art as of the priority date of the '912 patent would have the following training, knowledge, and experience: an undergraduate degree in Electrical Engineering or Computer Engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market.

Kozyrakis Decl. ¶ 8; 2d Kozyrakis Decl. ¶ 12; 3d Kozyrakis Decl. ¶ 9; 4th Kozyrakis Decl. ¶ 12. Dr. Sechen does "not necessarily agree with Dr. Kozyrakis's definition of a POSITA in the technical field," but adopts this understanding for purposes of analysis. Sechen Decl. ¶ 10.

Based on the testimony of these various experts,[15] we determine a person of ordinary skill in the art is a person with (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline and (2) at least two years of experience in designing computer memory systems. This ordinarily skilled artisan would also have familiarity with and understanding of (1) JEDEC standards related to memory devices and modules, such as DDR SDRAM devices and DIMMs, and (2) the latest DRAM memory

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[15] None of the parties in this proceeding dispute these individuals' qualifications. We thus presume these experts are qualified to address the technology in the '912 patent and the skill level in the art.

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devices in the market. We additionally note that the prior art, including Amidi, reflects the appropriate skill level at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).[16]

Next, we turn to Amidi and the differences between Amidi and the claims at issue. *See Graham*, 383 U.S. at 11. As stated above, Amidi explicitly discusses address signals (e.g., A0-A11), but not bank address signals, are received by registers 408 and 418. Amidi ¶ 49. However, under an obviousness analysis, we consider further what an ordinary skilled artisan would have recognized from Amidi's disclosure, when employing one's inferences and creative steps. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Amidi states "address lines A0-A11 go to module register 408 and 418 and address lines A12 goes into CPLD." Amidi ¶ 49. Amidi also shows address signals Add[n-1:0] (e.g., A0-A11) entering register 608 in Figure 6A and Add(n) (e.g., A12) entering CPLD 604. Amidi, Fig. 6A. When considering these teachings collectively, Amidi suggests that register 608 may be both registers 408 and 418 in Figures 4A and B. Amidi, Figs. 4A–B, 6A–B. That is, the teaching in paragraph 49 in Amidi related to where the address lines connect combined with the signals shown entering register 608 in Figure 6A suggests that register 608 represents both register 408 and 418. *See* R3 Resp. Br. 4. Importantly, this teaching in Amidi deviates from JEDEC standards, such as JEDEC 21-C, which shows only certain address signals are inputted into one register (e.g., register 1) and other address signals are inputted into another register (e.g., register 2). JEDEC 21-C, 4.20.4-18.

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[16] This position is consistent with at least IPR2014-00883. *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No. 33, slip op. at 13 (PTAB December 14, 2015).

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Amidi's Figure 6A shows various other signal lines entering register 608, including bank address signal lines. Amidi, Fig. 6A. Following from the above discussion that Amidi's registers 408 and 418 receive address lines A0 through A11, Amidi's Figure 6A and B thus suggests that both registers 408 and 418 may receive other signals shown entering register 608, including bank address signals. *See* R3 Resp. Br. 4. We agree that combining the teachings in Amidi at least suggest to an ordinary skilled artisan that signals other than the explicitly-disclosed address signals A0-A11, such as bank address signals BA0 and BA1, may be received by each of register 408 and 418 in a similar fashion.

Moreover, Amidi teaches deviating from JEDEC design specifications in at least one other aspect. Amidi discusses creating a transparent four rank memory module that fits into a memory socket having two chip select signals (e.g., a configured two rank memory module). Amidi, Title, ¶¶ 1, 4, 8, 11–12, 49; 3d Wang Decl. ¶ 17; R3 Resp. Br. 2–3 (citing Amidi ¶ 10–12). Amidi further states its memory module emulates a two rank memory module with a four rank memory module. Amidi ¶¶ 23, 41, 49, 57, 59, 62, Fig. 7. As understood, JEDEC 21-C design examples do not discuss such a transparent four rank memory module. *See generally* JEDEC 21-C. Thus, Amidi discloses at least one more example of deviating from the JEDEC design specifications.

Even further examples include the register in JEDEC includes two additional input signals, S0 and S1, which are described as chip select lines (*see* JEDEC 21-C, 4.20.4-6 and 4.20.4-16), which contrast with Amidi's chip select lines, cs0 and cs1, entering CPLD 604 (*see, e.g.*, Amidi, Fig. 6A).

As previously stated when addressing the anticipation rejection, Patent Owner accepts that one skilled in the art would have recognized that Amidi

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deviates from JEDEC design specifications where expressly stated. PO Reb. Br. 9. However, Patent Owner argues where Amidi is silent concerning departing from JEDEC, "a POSITA's default position would be to understand Amidi's registers in light of JEDEC specification, including JEDEC 21-C." PO Reb. Br. 10. Based on this understanding, Patent Owner asserts that one skilled in the art would have understood Amidi's register 608 in the context of the described register functional assignments in JEDEC 21-C, where only one register receives the bank address signals. PO App. Br. 14–15 (discussing and reproducing part of JEDEC 21-C 4.20.4-18), 20–21 (discussing and reproducing part of JEDEC 21-C4.20.4-16).

We agree with Patent Owner to the extent that an ordinary skilled artisan having two years of experience designing memory modules would have *consulted* with the JEDEC specifications, including JEDEC 21-C, when designing a circuit for a memory module or DIMM. However, we depart from Patent Owner's position that one skilled in the art would always adhere to JEDEC specifications wherever Amidi is silent. Other than the explicit disclosure to the "standard defined height limits by JEDEC" which restricts the number of TSSOP (thin-shrink small outline package) placements per side or per module (Amidi ¶ 7), Amidi does not discuss any further restrictions or adherence to JEDEC (*see generally* Amidi). As another example discussed above, Amidi teaches emulating a two rank memory module using a transparent four rank memory module. Amidi ¶¶ 23, 41, 49, 57, 59, 62, Fig. 7. As such, an ordinary skilled artisan would have recognized that not all designs, including Amidi's, follow JEDEC specifications.

Moreover, one having ordinary skill is not an automaton and would have employed their background knowledge and creative steps when designing memory modules. That is, one skilled in the art would have recognized that memory

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modules that explicitly differ from JEDEC design specifications, such as Amidi's (e.g., emulating a two rank memory module on a four-rank memory module), may affect the memory module in other ways and require further unspoken differences, including other signals being received by registers in Amidi. For instance, one skilled in the art would have recognized that directing other signals, including bank address signals, to two registers can further assist in emulating a two rank memory module in a four rank memory module in a cost effective manner. *See* Amidi ¶¶ 11, 23, 41, 49, 57, 59, 62, Fig. 7.

And even if one skilled in the art would defer to JEDEC 21-C designs, JEDEC 21-C itself teaches the ordinarily skilled artisan that modifications to the reference design may be required. Specifically, JEDEC 21-C discusses reference design examples as "an initial basis for Registered DIMM designs" but further clarifies that modifications to the reference designs may be required to meet "all system timing, signal integrity, and thermal requirements." JEDEC 21-C, 4.20.4-5, *cited in* R3 Resp. Br. 3–4. Additionally, we agree with Requester 1 that JEDEC does not state that two registers are sufficient for all types of memory modules. *See* R1 Resp. Br. 10 (citing 3d Wang Decl. ¶ 19).

Accordingly, when comparing JEDEC 21-C with Amidi, an ordinary skilled artisan would have recognized Amidi's memory module design differs from JEDEC reference designs and that modification from the JEDEC reference designs would need to occur. JEDEC 21-C, 4.20.4-5, *cited in* R3 Resp. Br. 3–4; *see also* R1 Resp. Br. 10 (indicating that POSITA is not "limited to constructing JEDEC compliant modules" and citing 3d Wang Decl. ¶ 19). These modification suggests signals other than address signals (e.g., bank address signals) being received by registers to meet system timing, signal integrity, and thermal requirements. We

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therefore disagree with Patent Owner that "there would be no suggestion or motivation in Amidi to have each Registers 408 and 418 be Register 608." PO App. Br. 21 (citing 2d Sechen Decl. ¶ 46).

Additionally, there is testimony supporting Requester 1's position that Amidi is not JEDEC compliant in all aspects where Amidi is silent. *See* R1 Resp. Br. 9–10; R3 Resp. Br. 3; 3d Wang Decl. ¶ 17. Dr. Wang indicates that an artisan is not limited by the conventional uses and is aware of variations from the JEDEC specification. 3d Wang Decl. ¶ 17. Requester 3 echoes Requester 1's position, contending that a person of ordinary skill is not limited to JEDEC reference designs. R3 Resp. Br. 3. Dr. Wang also states an ordinarily skilled artisan "would know that there exist multitudes of memory modules and supporting devices that do not follow JEDEC specification." 3d Wang Decl. ¶ 17, *cited in* R1 Resp. Br. 8, 10. Patent Owner contends Dr. Wang's testimony undermines (1) his own earlier testimony in this regard, (2) Dr. Bagherzadeh's, and (3) Dr. Sechen's. PO App. Br. 23 (citing Wang Decl. ¶ 9,[17] 2d Bagherzadeh Decl. ¶ 31, and 2d Sechen Decl. ¶ 34).

In response, Requester 1 asserts that Patent Owner took Dr. Wang's discussion in his first declaration "out of context." R1 Resp. Br. 11. In paragraph 9, Dr. Wang indicates that a logic circuit designer would have been guided by standard bodies such as JEDEC "[i]n many instances" and "would have configured a logic circuit to meet the functional requirements of the JEDEC standards." Wang Decl. ¶ 9. However, Dr. Wang further states that "the exact implementation is also driven by *other design requirements and designer preferences.*" *Id*. (emphasis

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[17] Requester 1 indicates that Patent Owner mistakenly referred to paragraph 10 of Wang's declaration. R1 Resp. Br. 11 n.2.

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added). For example, "a logic circuit designer" would have weighed various

factors, including the

> decision to combine control logic, flip-flops and other elements of a register
> with combinational logic may be made to obtain reduction in cost, gate count,
> reduced loading, reduced power consumption and to lower complexity of
> DIMM layout, although such decisions may also be influenced by the 'best
> practices' approach of JEDEC[.]"

Id. As such, we determine that Dr. Wang's later testimony related to deviating

from JEDEC specifications is consistent. That is, artisans are influenced by

JEDEC design specification but also weigh *other* design factor and preferences

beyond JEDEC design specifications. *See id.*

Concerning the other experts, we agree with Dr. Bagherzadeh that an artisan

would have looked to JEDEC 21-C for guidance when designing a DIMM, as

stated previously, but disagree that "the DDR DIMMs taught by Amidi conform to

[the] standards authorized by JEDEC" (2d Bagherzadeh Decl. ¶ 31) in *every* aspect

as previously discussed. Notably, Dr. Bagherzadeh is not specific as to which

JEDEC standards Amidi conforms. *Id.* Nonetheless, because Amidi differs from

JEDEC design standards as previously explained, we determine Dr. Bagherzadeh's

testimony is less probative than Dr. Wang's regarding JEDEC design specification

conformance. Dr. Sechen also urges us that one skilled in the art would have

followed JEDEC when the prior art is silent. PO App. Br. 23 (citing 2d Sechen

Decl. ¶ 34). But, as stated previously, we disagree.

We further find that Dr. Wang's testimony is aligned with Amidi, which

deviates from JEDEC designs, and has probative value in determining that there

are a "broad range of design considerations that a logic circuit designer would take

into account," and may also be influenced "by other design requirements and

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designer preferences [than JEDEC,]" including those concerning reducing costs, loading, power consumption, and complexity of DIMM layout. R1 Resp. Br. 11 (quoting Wang Decl. ¶ 9). When referring to Figure 6A of Amidi specifically and when designing a memory module, Dr. Wang states that one "would have understood . . . it would be prudent to connect all or substantially all of the address, control and other signals to . . . registers . . . in order to provide the logic designer with maximum flexibility." Wang Decl. ¶ 21. Amidi further recognizes that many memory device families or densities may be used to build Amidi's memory module. Amidi ¶ 71. Although the record may not support that one would have recognized to connect *all* signals to registers in Amidi, we agree with Dr. Wang that Amidi suggests to an ordinary artisan to connect some of signals in Amidi to both registers as previously discussed.

When considering collectively (1) Amidi deviates from JEDEC design specifications in multiple ways, including (a) disclosing receiving address signals A0–A11 at registers 408 and 418, (b) emulating a two rank memory module using a transparent four rank memory module, and (c) diverting its chip-select signals to a logic element, (2) the suggestion in Amidi that one skilled in the art would have recognized based on deviations from JEDEC design specifications that signals other than address signals also enter Amidi's register shown in Figure 6A, and (3) the background knowledge and creative steps of an ordinarily skilled artisan would have employed given Amidi's teachings and suggestions alone or in combination with JEDEC, we determine that one skilled in the art would have recognized both registers (e.g., one mapped to the recited "register' and the other mapped to the recited "logic element") receiving bank address signals to account for the design requirements of Amidi and preferences of the artisan. To the extent that changes

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are needed to Amidi to connect signals other than row/column address signals, such as bank address signals to the registers, such a change permits the logic circuit designer the flexibility to design a logic circuit for multiple purposes and applications as discussed previously. We therefore disagree with Patent Owner that Requesters have not provided any rebuttal to demonstrate why a person of ordinary skill in the art would have bank address signals enter both registers in Amidi. *See* PO Reb. Br. 11–12.

Patent Owner contends that bank address signals entering both registers (e.g., 408 and 418) implies duplication of the register function, including receiving "the same set of input signals" and that this duplication makes no sense to one skilled in the art when considering power and dimensional requirements as well as costs. PO App. Br. 21–22 (citing 2d Sechen Decl. ¶¶ 46–51); PO Reb. Br. 10–11. For support, Dr. Sechen testifies that an ordinarily skilled artisan would have been aware of dimensional requirements for JEDEC modules, including height requirements discussed by Amidi, and that given these concerns, one would not have understood Amidi suggests each register 408 and 418 to be the entire register function. 2d Sechen Decl. ¶ 47–48.

We are not persuaded. First, the above discussions concerning Amidi and what one of ordinary skill in the art would have understood from Amidi teach the input address signals are received by both registers 408 and 418 contrary to JEDEC 21-C. *See* Amidi ¶ 49, Fig. 6A. Also, these teachings in Amidi do not require that the *entire* register function be duplicated in each of register 408 and 418.

Second, even if duplicated in its entirety occurs, such as the *alternative* rejection presented for Ground 6 (RAN 33), Amidi's statement related to considering the "standard defined height limits by JEDEC" for TSSOP placement

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per side and per module (Amidi ¶ 7) do not require compliance in other design aspects as previously discussed. Third, there is inadequate evidence in the record between the height or dimensional requirements discussed in Amidi that are according to JEDEC specifications (*id.*) and how Dr. Sechen concludes that this sole dimensional requirement would lead an ordinarily skilled logic circuit designer not to understand Amidi suggests each of registers 408 and 418 to receive at least some of the signals shown in Figure 6A entering register 608. *See* 2d Sechen Decl. ¶ 47–48.

Dr. Sechen further discusses the power requirements that would result from each register 408 and 418 if duplicated. 2d Sechen Decl. ¶¶ 49, 51. In particular, Dr. Sechen states that one skilled in the art would have concluded that two registers behave as a single register according to JEDEC design specifications so as to "minimize power." 2d Sechen Decl. ¶ 51. To be sure, power consumption would be a factor to an ordinarily skilled artisan when designing a memory module. However, as explained above, Amidi does not possess a traditional JEDEC logic circuit design and requires modifications from JEDEC design specifications. Thus, although we appreciate Dr. Sechen's insights that "JEDEC 21-C at page 4.20.4-62 explains that a single Register (comprising Registers 1 and 2) is sufficient to handle a module having 36 DDR DRAM devices in a stacked arrangement" (2d Sechen Decl. ¶ 50), we are not persuaded sufficiently that any increased power consumption in Amidi resulting from directing bank address signals to both registers 408 and 418 would be unworkable.

Even if more power is consumed in Amidi's memory module when the registers are duplicated, balancing the relative advantages (e.g., flexibility of using less expensive chips) and disadvantages (e.g., increased power consumption) are

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engineering tradeoffs well within the level of ordinarily skilled artisans. That is, Amidi teaches creating a transparent four rank memory module that fits into a memory socket having two chip select signals (e.g., emulating the function of a two rank memory module) because such lower density memory devices are cheaper and more readily available. *See* Amidi ¶¶ 1, 4, 8, 11–12; R3 Resp. Br. 3. The record thus supports that a logic circuit designer employing their background knowledge would have considered various design factors (e.g., cost, loading, power consumption, complexity) when designing a memory module.

As to whether Amidi additionally suggests that CPLD 604 receives bank address signals, we indicated previously that Amidi does not disclose bank address signals are received by CPLD 604. Amidi, Figs. 6A–B; October 14, 2011 Non-Final Act. 15 (stating "Figure 6 clearly shows that only the register 608 receives the bank address signals.") But, as stated above, our analysis based on obviousness does not stop here.

When addressing Ground 4, the record reflects that the Examiner did not adopt Requester 1's position that "it would have been obvious to one or [sic] ordinary skill in the art at the time of the invention to provide such control signals to the [CPLD] to improve the active bank/rank determination." Non-Final Act. 15–16 (quoting from R1 Request 128). In particular, the Examiner states "[t]his is merely an allegation without any reasoned analysis as to how and why providing 'such control signals' to [the] CPLD would be obvious and improve . . . or duplicate the control signals so as to be received by [the] CPLD and how this improves the memory module." October 14, 2011 Non-Final Act. 16. We agree with Patent Owner that subsequent actions maintain this position. PO Reb. Br. 13. That is, when addressing claim 7, the Examiners adopted the analysis that Amidi

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teaches or suggests both registers received the bank address signals but not the CPLD. *See* November 13, 2012 Non-Final Act. 18, ACP 24, and RAN 24 (referring to "Figure 6, registers 408 and 418, shown as 608 in Figure 6, receive BA signals" for Grounds 3 and 4 when discussing claim 7); ACP 28 and RAN 28 (referring to Ground 3 when discussing Ground 4).

As such, the record reflects that the Examiner determined that there is insufficient reasoning with a rational underpinning why one skilled in the art would have recognized providing Amidi's CPLD with a bank address signal.

Dr. Wang, Requester 1's expert, addresses Amidi's CPLD (e.g., 410 in Figure 4A or 604 in Figure 6A) stating one skilled in the art "would have considered connecting all address signals, including bank address signals, to the Amidi CPLD to allow flexibility in design of an address mapping scheme." Wang Decl. ¶¶ 17, 21. Dr. Wang states:

> Amidi describes the use and operation of a logic element to reassign address signals when a memory module is designed to emulate a memory module having a different number of ranks. For example, where a memory module having two lower density ranks is used to emulate a memory module with one rank having double the memory density, Amidi would have been used to remap address signals, including rank address signals. A person of ordinary skill in the art of memory system design would have known to remap address signals by reassigning one or more bank address signals for rank selection purposes.

Wang Decl. ¶ 19.

Dr. Wang also states, when addressing supplying bank address signals to a logic device, "[p]ersons of ordinary skill in the art related to memory system design would have known that many different address mapping schemes . . . and that the choice of address mapping scheme would have been made based on various design goals." Wang Decl. ¶ 24. As such, Dr. Wang contends connecting

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address signals, including bank address signals, to the CPLD allows for flexibility in design of address mapping scheme and for reconfiguring to receive different configurations and memory densities. Wang Decl. ¶¶ 17, 21. In an attempt to corroborate the position that an ordinary skilled artisan would have known to use different mapping schemes for the CPLD, including using a bank address signal as a density transition bit to generate a chip-select signal, Dr. Wang discusses an attached exhibit, Exhibit A, and an Intel 450NX chip set. 3d Wang Decl. ¶ 14 (citing Ex. A, 2-5, 212 – 2-15). Notably, this exhibit is not part of the obviousness rejections based on Grounds 4 and 6. Moreover, Dr. Wang does not demonstrate that these Intel chip sets were known to be used in DIMMs, like Amidi's. *See id.*

Upon review, we determine this exhibit is inconclusive and does not demonstrate adequately that a "RAS/CAS generator accepts External (Input) signals as Bank[2:0]#, CARD#, CMND[1:0], MA[13:0]# and decodes the Bank[2:0]# signals as CAS and RAS signals to directly drive banks of DRAM devices." Exhibit A, 2-5, 2-12–2-15. At best, the exhibit discusses column and row access strobes (CAS/RAS) signals are used to latch column and row addresses into the DRAMS. *See* Exhibit A, 2-14. This discussion in no way addresses why one skilled in the art would have recognized Amidi's CPLD receiving a bank address signal.

Moreover, Dr. Wang indicates "the Intel 82452NX RAS/CAS generator datasheet is a datasheet that describes the functionality of the chipset as a whole rather than a logic specification of the 82452NX RAS/ CAS generator." 3d Wang Decl. ¶ 14. Without further discussion, he further concludes that

> it would have been clear to a person of ordinary skill in the art at the relevant time that the 82452NX RAS/CAS generator accepts BANK[2:0]# signals as inputs, and upon assertion of the Access

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> command and Command strobe signals, the 82452NX RAS/ CAS
> generator creates command sequences, including RAS and CAS signals
> at least in part to the BANK address signals.

Id. Yet, even presuming without deciding that Dr. Wang is correct, we disagree that this data sheet, as discussed above, demonstrates to an ordinarily skilled artisan to use Amidi's CPLD to receive a bank address signal. *See id.*

Granted, Amidi has a general teaching to modify its memory module design. Amidi ¶ 71. But, as stated above, the record for Requester 1's adopted rejection does not support the specific modification of using a bank address signal in place of a row or column address signal (e.g., Add(n)) in Amidi. Amidi, Figs. 6A–6B. Other than conclusory remarks made by Dr. Wang, this is insufficient evidence in Amidi, JEDEC, or elsewhere in the record to demonstrate a reason with rational underpinning that one skilled in the art would have inputted a bank address signal, as opposed to a row/column address signal, into Amidi's CPLD.

Thus, to the extent Patent Owner has argued Requester 1's proposed obviousness rejections based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a CPLD receiving BA signals, we agree.

Lastly, although not argued by Patent Owner (*see* R1 Resp. Br. 2), we agree with the Examiner's findings and conclusion concerning the evidence of secondary considerations failing to outweigh the case for obviousness. RAN 65–66.[18]

For the above-discussed reasons, we sustain the adopted rejection of claims 7 and 33 based on Amidi alone (Ground 4) or Amidi in combination with JEDEC (Ground 6) under § 103.

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[18] The Examiner refers to the Declaration of Dr. Hyun Lee dated July 5, 2011 and the Declaration of Christopher Lopes dated July 5, 2011. RAN 65.

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3. *Obviousness Rejection Based on Amidi and Dell 2 – Ground 5*

Claims 7, 26, and 33 are also rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. RAN 12 (referring to "Proposed by Requesters 1 and 2; modified 8/14/13"[19]), 30. As a preliminary matter, the RAN states claim 26 is rejected under Ground 5. RAN 12, 30. However, the body of the rejection does not discuss claim 26 and refers to Ground 3, which does not reject claim 26. *See id.* The Examiner did not clarify this anomaly in the Answer. Both Patent Owner and Requester 1 indicate the discrepancy, each reaching the opposite conclusion as to whether this claim has been rejected under Ground 5. *See also* PO Reb. Br. 14; R1 Resp. Br. 10 n.1, 13–14.

We determine that Patent Owner has been put on notice that claim 26 is rejected under this ground and has had the opportunity to respond to the rejected claim. First, claim 26 has been included in the rejection for Ground 5 since November 13, 2012. *See* November 13, 2012 Non-Final Act. 7 and ACP 7–8. Second, Patent Owner states "the recitations of claim 26 do not differ much from the recitations of claim 7." PO App. Br. 6, *quoted in* R3 Resp. Br. 6. And Patent Owner also grouped claim 26 with claims 7 and 33 in its opening brief, presuming claim 26 had been rejected based on Amidi under Grounds 3–6. PO App. Br. 12, 24 (stating "the Examiner's adoption and maintenance of Grounds 3-6 for claims 7, 26 and 33 was accordingly in error"). Thus, given that the record, claim 26 has been rejected for reasons similar to claim 7, and for purposes of this appeal, we treat claim 26 as having been rejected under § 103 based on Amidi and Dell 2 (Ground 5).

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[19] Requester 2 filed corrected comments on August 14, 2013.

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Turning to the merits of the rejection, Patent Owner does not dispute the teachings of Dell 2 related to this rejection. *See generally* PO App. Br. 12–24. Because Dell 2 is not disputed, Requester 1 contends that Patent Owner has waived its rights to appeal to the rejection. R1 Resp. Br. 14. In the Rebuttal Brief, Patent Owner contends that the Examiner's rejection on this ground expressly relies on Amidi alone and that Patent Owner "did not need to address Dell 2 to properly appeal the rejection of claim 26." PO Reb. Br. 14. We agree that Patent Owner has appealed this ground of rejection.

For Ground 5, the Examiner refers to Ground 3, concluding that claims 7 and 33 are obvious because they are anticipated. RAN 30. For the reasons discussed above, we agree that claims 7 and 33 are rendered obvious based on Amidi and the registers 408 and 418 mapped to the recited "register" and "logic element."

However, contrary to Patent Owner's position (PO Reb. Br. 14), this rejection *also* refers to the obviousness rejection over Amidi and Dell 2 proposed by Requester 1 and 2. RAN 12 (referring to "Proposed by Requesters 1 and 2; modified 8/14/13"); *see also* R2 August 14, 2013 Comments 4–12 (citing Amidi ¶¶ 8, 40–43, 45–52, 71; Dell 2, Abstract, 2:40–3:5, 4:62–6:14, 8:5–64; 3d Bagherzadeh Decl. ¶¶ 12–17, 21–22, 24, 26, 37; 2d Bagherzadeh Decl. ¶ 25) and R1 February 13, 2012 Comments 22 (referring to claim charts in R1 Request, which cite Dell 2, 2:32–38, Fig. 1 at R1 Request 159, 166, 176, 182). Thus, the RAN indicates that the proposed rejections of Requester 1 and 2 were adopted by the Examiner. *See* RAN 30 (indicating the proposed rejection of claims 7, 26, and 33 are adopted and these claims were proposed by Requester 1), 12 (referring to the proposals of Requester 1 and 2 *as modified on August 14, 2013,* which is the

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date of Requester 2's comments). Accordingly, when viewing the RAN as a
whole, the adopted rejection does not just rely on Amidi but is a combination of
Amidi and Dell 2.

Patent Owner contends that Requester 2's arguments for Ground 5 are not
permitted. PO Reb. Br. 17. Specifically, Patent Owner argues that the adopted
rejection for Ground 5 rejected claims 7 and 33 "for Requester 1, but not for
Requester 2." *Id.* (citing RAN 30). As noted above, we disagree. Also, although
the Examiner states that the proposed combination with Dell 2 as presented by
Requester 2 does not overcome "the deficiency" of Amidi (RAN 32), the
deficiency discussed appears to concern limitations recited in claim 52, for
example, which differ in scope from claim 7. *Id.* (referring to Ground 3); *see also*
RAN 26–27 (discussing Ground 3).

We therefore determine that the Examiner has adopted Requester 1's and 2's
proposed rejection, including that concerning the bank address limitation. To
summarize, Requester 2 relies on the discussion of claim 1 when rejecting claim 7.
R2 August 14, 2013 Comments 45–46 (referring to claim 1). Requester 2 in
general states Amidi suggests other types of memory devices or densities can be
used to build the four rank memory module. Amidi ¶ 71, *cited in* R2 August 14,
2013 Comments 8, 10–12, 29, 38. Additionally, Dell 2 teaches a technique for
using various types of memory devices or densities other than those in Amidi,
where the memory device is configured with M banks, but the logic circuit
receives address and bank address inputs corresponding to N bank memory device.
Dell 2, Abstract, claim 1, *cited in* R2 August 14, 2013 Comments 9, 29–30, 38–39.
For example, Dell 2 teaches a logic circuit that receives address and bank address
inputs where the memory devices of the memory module are configured with a

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different number of banks than the system's expected number of banks (e.g., memory module has memory devices having greater or fewer internal banks than expected). Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, *cited in* R2 August 14, 2013 Comments 9–10, 12, 30, 39, 45–46.

The above teachings in Dell 2 teach or suggest a logic element receiving and using free signals, including a bank address signal, to provide the needed bank address signals based on the difference between the actual and expected number of banks for the memory devices of the memory module system. Combining this teaching with Amidi's suggestion to use other types of memory devices (Amidi ¶ 71) would have predictably yielded the recited "both the bank address signals of the set of input control signals are received by both the logic element and the register" in claim 7 so that the necessary rank chip select signals discussed in Amidi are produced. That is, Amidi and Dell 2, collectively, teach that ranks and banks both may be expanded; therefore, a skilled artisan would recognize various combinations of inputs to achieve expansion including bank address inputs as broadly recited. This combination also addresses the demand for increased memory capacity and compatibility issues. *See, e.g.,* R2 August 14, 2013 Comments 12 (citing 3d Bagherzadeh Decl. ¶ 37), 29–30, 38 (citing Amidi ¶ 71). Moreover, this combination further teaches using the logic circuit or element (e.g., Amidi's CPLD) to receive bank address signals for the above-discussed purpose.

Finally, we agree with the Examiner's findings and conclusion concerning the evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, for previously stated reasons, we sustain the adopted rejection of claims 7, 26 and 33 based on Amidi and Dell 2 under § 103.

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B. *Claims 2, 5, 21, 23, 30, and 119 (Claims with the Storing Limitation)*
   wherein the circuit is configured to store an input signal of the set of
   input signals during a row access procedure for subsequent use
   during a column access procedure.

1. Anticipation Rejection Based on Amidi (Ground 3)

Claims 2, 5, 21, 23, 30, and 119 have been rejected under 35 U.S.C. § 102 based on Amidi. RAN 22–26. Patent Owner argues these claims as a group. PO App. Br. 25–38. We select claim 21 as illustrative. Notably, claim 21 requires the circuit to be configured to store an input signal without reciting the type of input signal stored or the location within the circuit where the signal is configured to be stored.

To teach the "storing" limitation, the Examiner refers to (1) Amidi's Figure 6A, (2) the input signal RAS into the registers transmitted as rRAS, (3) Add(n) discussed in paragraph 52, and (3) Requester 2's Comments filed March 30, 2012 discussing using Add(n) as an input into CPLD 604 to generate rcs2 and rcs3, which Requester 2 contends are needed for the duration of the read/write cycle. RAN 24–25 (addressing both claims 2 and 21). The Examiner also adopts Requester 1 and 2's proposed rejections (RAN 22 (indicating proposed rejection by Requester 1 and 2 are adopted for claim 21)), which include a discussion of paragraph 61 of Amidi. *See, e.g.,* R2 Request 997 (citing Amidi ¶ 61). Thus, although Patent Owner asserts that the Examiner repeatedly relies on an input RAS signal being stored in a register and transmitted as output rRAS signal (PO App. Br. 32–33), we determine that this is only *part* of what the Examiner cites in formulating the rejection. *See also* R2 Resp. Br. 16.

Requester 1 contends Patent Owner is focusing on an improper low level of skill in the art, where the ordinary artisan would "blindly follow certain JEDEC

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standards." R1 Resp. Br. 12. As stated above, we agree that Amidi is not JEDEC compliant in all aspects of its memory module design and thus one skilled in the art would not have followed all of the design specifications discussed in JEDEC designs.

Requester 1 also asserts that an ordinary artisan would have been familiar with DDR2 devices "which supports posted CAS [column access strobe] commands" and a DDR2 SDRAM memory controller will "treat a row activation command (part of a row access procedure) and a column access command as a unitary command pair to be issued in consecutive cycles." R1 Resp. Br. 13 (citing Wang Decl. ¶ 22). Requester 1 presumably contends that a posted CAS command is an input signal stored during a row access procedure for subsequent use during a column access procedure. *Id.* Yet, even assuming that Requester 1 is correct, this contention does not address sufficiently where the command or signal is stored. *Id.* In particular, Requester 1 states that the entire CAS command would be posted (e.g., stored) in the memory device (e.g., the DRAM device)— not the circuit recited as a separate component from the memory devices in claim 21. *See* PO Reb. Br. 22–23; Wang Decl. ¶ 22. Thus, even assuming that the RAS and CAS commands are treated as a unitary command and stored in memory devices (R1 Resp. Br. 13), there is insufficient disclosure that Amidi's circuit—separate from the memory devices — is configured to store input signals during a row access procedure for a subsequent column access procedure as recited.

Requester 2 contends Amidi discloses the "storing" feature in claim 21 when registering the row address for use with the column address in a separate cycle. R2 Resp. Br. 12–13 (citing Amidi ¶¶ 38, 61[20]). Amidi specifically discusses internal

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[20] Requester 2 mistakenly referred to paragraph 60. R2 Resp. Br. 12.

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circuity within a CPLD for Row Address Decoding (e.g., a row access procedure) and Column Address Decoding (e.g., a column access procedure). Amidi ¶ 61, *cited in* R2 Resp. Br. 12 and R2 Request 997. Here, Amidi states the column address decoding scheme is unique, requiring two sets of addresses rather than the standard DDR memory module where only one set of address lines is required in order to access a cell. Amidi ¶ 61. Amidi even further states the first set includes the row address provided with proper control and command signals and the second set, on a separate cycle, includes the column address provided with its proper control and command signals in order to read or write "to that particular cell." *Id.*

Although both the row and the column address require "control and command signals" (*id.*; *see* R2 Resp. Br. 12–13), Amidi does not discuss explicitly storing the proper control and command signals (e.g. input signals) during a row access procedure for later use during a column access procedure. Amidi ¶ 61. Amidi also does not state explicitly which "control and command signals" are used during each step. *See id.*

Amidi further states register 408, which is considered part of the recited circuit in claim 21, "may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out." Amidi ¶ 38, *cited in* R2 Resp. Br. 11. We fail to find a discussion of how the register stores signals *during a row access procedure* for subsequent use during a column access procedure. *Id.* Nor do we determine that eliminating loading of memory devices as discussed in Amidi implies that a logic element will inherently store the information during a row access procedure for subsequent use during a column access procedure as recited in claim 21.

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Turning to cited paragraph 52, Amidi discusses generating signals (e.g., rcs0–rcs3) that exit CPLD 604 from the input signals (i.e., CS0, CS1, and Add(n)) to "ensure[] that all command for a two rank memory module . . . are also performed on the four rank memory modules." Amidi ¶ 52, *cited in* RAN 24–25. Amidi discusses generating rcs0-rcs3 signals, when various CS0 and CS1 commands are issued (e.g., Auto Precharge all Banks, Auto Refresh, Load Mode Register). *Id.* Yet, Requesters 1 and 2's proposed rejection, adopted by the Examiner, have not demonstrated sufficiently that the input signals (e.g., CS0, CS1, or Add(n)) are necessarily stored in part of the circuit (e.g., CPLD) during a row access procedure for later use during a column access procedure. As Patent Owner indicates, the Add(n) signal enter an OR logic in Figure 8 and then a multiplexer along with other signals. PO Reb. Br. 24–25 (citing Amidi ¶¶ 69–70, Fig. 8 (logic 812, 814)).

Although Requester 2 states that its rejection does not rely on the concept of inherency (R2 Resp. Br. 18), Patent Owner further discusses the "storing" claims in the context of inherency, asserting that Requester 2 is incorrect. PO App. Br. 34–36 (citing Requester 2's March 2012 Comments); PO Reb. Br. 25–26. In a nutshell, Requester 2 contends that Dr. Bagherzadeh's testimony supports that "the missing descriptive matter, *i.e.*, storing, is necessarily present." R2 Resp. Br. 19–20. We agree that this discussion relies on the concept of inherency and that Amidi's circuit necessarily at least temporarily stores an extra row address bit that is received in order to identify the correct memory device. R2 Resp. Br. 18–20 (citing 2d Bagherzadeh Decl. ¶ 22); *see also* PO App. Br. 35 (citing 2d Bagherzadeh Decl. ¶ 22).

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However, Requester 2 presents insufficient evidence to support that Amidi's circuit *must* store the extra row address bit during a row access procedure for later use during a column access procedure. Whether Amidi's disclosure demonstrates that storing the bit between these procedures is probable or possible is not sufficient for an anticipation rejection. *See Robertson*, 169 F.3d at 745. Additionally, Patent Owner offers the testimony of Dr. Kozyrakis which describes at least two possible options (e.g., store an address bit for subsequent use during a column access procedure *or* store resulting signals— not the input address signals— from a decoding process) that one skilled in the art would have been aware of to address how Amidi's four rank memory module can emulate a two rank memory module. 2d Kozyrakis Decl. ¶ 33, *cited in* PO App. Br. 35.

Lastly, Requester 3 discusses Amidi only in the context of the obviousness, thus alluding to Requester 3's position that Amidi alone or in combination with at least one additional reference suggest or teach the storing limitation in claim 21 but does not anticipate the disputed features of claim 21. *See generally* R3 Resp. Br.

We therefore determine the Examiner erred in rejecting (1) claim 21, (2) claims 2, 5, 23, 30, which recite similar limitations, and (3) claim 119, which depends from claim 2, based on Amidi under § 102.

Because we determine Amidi does not anticipate claim 21, we need not reach whether Amidi is enabled for the storing limitation. PO App. Br. 36–38; PO Reb. Br. 32–34.

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2. *Obviousness Rejection Based on Amidi Alone or in Combination with JEDEC (Grounds 4 and 6)*

Turning to the obviousness rejection of illustrative claim 21 based on Amidi, we initially note that "[a] non-enabling reference may qualify as prior art for the purpose of determining obviousness under [35 U.S.C.] § 103." *In re Antor Media Corp.*, 689 F.3d 1282, 1288, 1292 (Fed. Cir. 2012) (quoting *Symbol Techs. Inc. v. Opticon Inc.*, 935 F.2d 1569, 1578 (Fed. Cir. 1991)); *see also Beckman Instruments v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989) (stating "[e]ven if a reference discloses an inoperative device, it is prior art for all that it teaches.") Thus, although Patent Owner argues Amidi is not enabled (PO App. Br. 36–38), Amidi is available as prior art for all that it teaches in the context of the adopted obviousness rejections.

Patent Owner repeats the argument that one skilled in the art would have adhered to the conventional JEDEC design standards. PO App. Br. 26–33; PO Reb. Br. 19. We are not persuaded for reasons previously discussed. As such, we determine that one skilled in the art would have recognized that at least some Amidi's input signals into the circuit of the memory module deviate from some of JEDEC's design conventions.

Moreover, in Grounds 4 and 6, the Examiner refers to the discussion of Ground 3. RAN 28, 33. As noted above, we determine that in formulating the rejection based on Amidi, the Examiner addresses various input signals, including Add(n), and control and command signals discussed in paragraph 61, in determining that input signals are stored during a row access procedure for later use in a column access procedure. RAN 25 (discussing address signal is needed for the duration of the read/write cycle); *see also* R2 Resp. Br. 16. The Examiner

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further refers to pages 32 through 35 of Requester 2's Comments filed March 30, 2012 when rejecting claim 21. RAN 25. We thus disagree with Patent Owner's argument that the rejection only discusses storing an input RAS signal. PO App. Br. 32–33; PO Reb. Br. 19–21.

Turning to the storing of address signals and "proper control and command signals" for use during a column access procedure as discussed in Amidi, Patent Owner argues that "Amidi's register 408 appears to have conventional DDR command operation, including the conventional DDR one-clock-cycle, single-use operating principle." PO Reb. Br. 24 (underlining omitted). That is, in Patent Owner's view, each DDR operation (e.g., active, read, write) has its own complete instantiated set of signal values and each is handled for a single cycle only. PO App. Br 26–27, 29. As such, Patent Owner asserts that all input values are discarded and replaced in a subsequent command such that no values are stored for subsequent use. PO App. Br. 27–28, 31–32 (citing 2d Sechen Supp. Decl. ¶¶ 65–66).

As discussed above, we determined that Amidi is not a conventional DDR memory module in accordance with all JEDEC design specifications. We further note that even Patent Owner does not commit to Amidi using conventional DDR commands. PO Reb. Br. 24 (stating "Amidi's register 408 *appears* to have a conventional DDR command operation") (emphasis added). Amidi further supports that it is not conventional. *See* Amidi ¶¶ 8, 11–12, *cited in* R3 Resp. Br. 7 (stating "[c]ontrary to the assertions by the Appellant, a person of ordinary skill would understand that Amidi's non-standard module <u>must</u> deviate from standard DDR command processing in order to operate properly."). Based on the above

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discussion, the record has not illustrated adequately that Amidi behaves
conventionally in accordance with JEDEC.

Patent Owner further contends that the input signals in Amidi are eliminated
every cycle from Amidi's register 408 and 418 and adhere to JEDEC 79C design
specifications. PO App. Br. 26–29; *see* 2d Sechen Decl. ¶¶ 65, 69; 3d Kozyrakis
Decl. ¶ 13. Even presuming that Patent Owner is correct, registers 408 and 418 are
not the only part of Amidi's memory module circuit that is separate from the
memory devices. For example, Amidi's memory module circuit also includes at
least a CPLD (e.g., 410 or 610). Amidi, Figs. 4A, 6A.

Amidi states that during row address decoding, the first address set is
provided with proper control and command signals. Amidi ¶ 61. Amidi further
states that, on a separate cycle, the column address decoding provides the second
address set that includes its proper control and command signals in order to read or
write "to that particular cell." *Id.* Although we indicated above that control and
command signals used during row and column address decoding are not disclosed
as being necessarily the same signals (*id.*), Amidi teaches that the later column
address decoding step "needs to be provided with its proper control and command
signals in order to read or write *to that particular cell.*" *Id.* (emphasis added).

We determine that Amidi's teaching suggests that the *proper* control and
command signals to read or write to the particular cell (e.g., address and bank
address signals) would involve at least some of the same signals received during
the row address decoding step, when applying the background and creative steps
one skilled in the art would have employed. *See* R2 Resp. Br. 12–13; R3 Resp. Br.
8–9. As such, one skilled in the art would have recognized that some efficiencies
are to be gained from designing a circuit that stores input signal values during a

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row access decoding procedure that are also *used later* during a column access decoding procedure. Additionally, there are a finite number of identified, predictable solutions (e.g., repeat or store values) for using the same signal values from one procedure to another (e.g., row to column) and one skilled in the art would have reasons to pursue these known options (e.g., design and processing considerations) in order to read or write to the correct cell at the column address step.

To illustrate this point, we refer to Truth Table 1a in JEDEC 79C. JEDEC 79C 12, *reproduced at* 2d Sechen Decl. ¶ 65. Some of the signals in Truth Table 1a or certain command/control signals are the same. *Id.* For example, each of an ACT or active command (e.g., a row access procedure) and a RD or read command (e.g., a subsequent column access procedure) have the same bank address (e.g., Bank under ADDR) and chip select signals (e.g., L under CS). *Id.* JEDEC 79C also explains READ or WRITE commands occur after ACTIVE commands and are issued "to that row." JEDEC 79C 21. JEDEC 79C even further discusses a subsequent ACTIVE command to a different row in the same bank can be only issued after the previous row has been closed. *Id.*

Patent Owner also identifies Bank Y values that are the same for the ACT and RD/WR commands. PO App. Br. 27 (discussing Figure 9 of JEDEC 79C); *see also* JEDEC 79C 21. This table along with Amidi's teaching in paragraph 61 suggest to one skilled in the art that some signals for both row access procedures and column access procedures are the same. Given that some of the values do not change between procedures (e.g., row and column address procedures), the teachings further suggest to an ordinary skilled artisan employing background knowledge and creative steps that Amidi's memory module can benefit (e.g., less

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processing) from storing unchanged values for later use. *See, e.g.,* R3 Resp. Br. 7,
11–12 (citing 3d Kozyrakis Decl. ¶¶ 18–19 and 2d Kozyrakis Decl. ¶ 33).

As such, Amidi alone or in combination with JEDEC teach or suggests a
circuit "configured to store an input signal of the set of input signals during a row
access procedure for subsequent use during a column access procedure" as recited
in claim 21. Thus, although not disclosing storing input signals explicitly as
explained previously, JEDEC designs suggest a benefit to storing such signals for
later use, and in particular, the combined teachings of the references suggest to a
skilled artisan that modifying Amidi's CPLD, to the extent necessary, to store an
input signal (in particular, an input signal used to perform expansion) during a row
access procedure for subsequent use during a column access procedure would have
been obvious.

Even more, Requester 2 discusses that the Truth Table in Amidi's Figure 5
shows storing the address signals, including transition bits, to determine the active
rank. March 30, 2012 Requester 2 Comments 34–35. In order to determine the
same rank during a later column access, Requester 2 argues that Amidi suggests
storing relevant information. *See id.* Requester 3 similarly asserts that rank-
multiplying memory modules must store information from the row access
procedure to match later with the column access procedure that completes a read
operation (e.g., while the row remains open) due to interleaving techniques. R3
Resp. Br. 5 (citing 3d Kozyrakis Decl. ¶¶ 15–19 and 2d Kozyrakis Decl. ¶ 33).
Requester 3 indicates the proper bank is identified by using chip select and bank
address signals. 3d Kozyrakis Decl. ¶ 17. But, in a rank-multiplying memory
module, Requester 3 identifies that incoming bank and address signals are not

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sufficient to identify the bank for the CAS command. R3 Resp. Br. 7 (quoting 3d Kozyrakis Decl. ¶ 18).

Dr. Kozyrakis testifies that a designer would have recognized in a rank-multiplying scheme, for every "activate, read or write command" issued, the controller of the memory module must identify a bank using bank address and chip select signals, and if the command is a CAS command, the controller must further identify the open row to execute the command using the same bank and chip select signals. 3d Kozyrakis Decl. ¶ 18. Dr. Kozyrakis states this can be achieved by using an address bit of the RAS command, which is later free to be used for this purpose during the CAS command because the address bit is not provided with the CAS command. 3d Kozyrakis Decl. ¶ 19 and 2d Kozyrakis Decl. ¶33, *cited in* R3 Resp. Br. 7–9; Sechen Decl. ¶ 96 (stating that in Amidi the row address bit is not available during column access command). This is further echoed by Requester 2 as indicated by Patent Owner. Requester 2's March 30, 2012 Comments 32–35 (citing 2d Bagherzadeh Decl. ¶¶ 21–22).

Given the record, we agree that one skilled in the art would have recognized the column access procedure for an open row occurs subsequent to a row access procedure and needs to be matched. We further determine, employing inferences and creatives steps, one skilled in the art would have recognized that storing and using previous input signals having information that is needed for subsequent column procedures would have improved Amidi's memory module design. And even though Dr. Kozyrakis offers two alternative options for generating the correct chip-select and bank address signals, we determine that both options, including storing an address bit from a row access procedure for use during a subsequent

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column access procedure, were known by ordinary artisan. 2d Kozyrakis Decl. ¶ 33, *quoted at* PO App. Br. 35.

We also disagree that Dr. Kozyrakis's testimony conflicts with Dr. Bagherzadeh's. PO App. Br. 36. Rather, as discussed above, Dr. Kozyrakis provides alternatives ways of storing values— one of which is storing input values within the memory module's circuit as recited in claim 21.

Patent Owner contends that Requester 3's position is flawed. PO Reb. Br. 28. In particular, Patent Owner contends that the teachings come from Requester 3 (e.g., Dr. Kozyrakis) and not from Amidi. We find no error in formulating an obviousness rejection based on what one skilled in the art would have recognized given Amidi as well as one's inferences and the creative steps an artisan would have employed rather than precise teachings from Amidi. *See KSR*, 550 U.S. at 418. Nor do we determine that the position taken by Requester 3 is based on impermissible hindsight. PO Reb. Br. 28–30. For example, as discussed above, Amidi and JEDEC suggest that at least some of the same proper control and command signals are needed during both a row and column address procedure in order to isolate, read from, and write to the desired particular cell, such that storing relevant input signal values (e.g., bank address signal) for later use would create design efficiencies and benefits. *See* Amidi ¶ 61.

Patent Owner further argues that storing the address bit for subsequent use during a column access procedure introduces a new principle of operation to and intended purpose for Amidi's address bit and further argues that Requester 3's position implies that the storing necessarily occurs. PO Reb. Br. 28. We disagree. First, Requester 3's comment concerning Amidi are in the context of an obviousness rejection— not anticipation where features must be necessarily

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present in one prior art reference. Second, Patent Owner does not demonstrate adequately that introducing a purportedly new operation into Amidi would teach away from Amidi, render Amidi inoperable, or destroy Amidi's device intended purpose. Moreover, as Requester 3 notes, such storage may "require storing only a single bit," further illustrating that if such design modifications are needed to Amidi, they are minor. R3 Resp. Br. 10.

Patent Owner further contends that the modification proposed by Requester 3 of Amidi "could not have been a predictable solution." PO Reb. Br. 30 (emphasis omitted). Rather, pointing to Dr. Kozyrakis' testimony, Patent Owner contends that there are barriers to overcome, including DDR standard-compliance and verification. *Id.* (citing 4th Kozyrakis Decl. ¶¶ 15–21). We are not persuaded. As stated previously, we disagree that Amidi is a DDR standard memory module. As a result, while we do not determine that an ordinarily skilled artisan would have necessarily performed every step discussed in Dr. Kozyrakis' testimony (4th Kozyrakis Decl. ¶¶ 15–21), we agree that some implementing, testing and verification of a logic circuit design would be commonplace to an ordinarily skilled artisan and not beyond this person's skill (*see* 4th Kozyrakis Decl. ¶ 21).

Concerning whether there is a reasonable expectation of success that the stored address bit in Amidi will perform as recited, Patent Owner repeats that such a change would create barriers to the "identified DDR standard-compliance and verification." PO Reb. Br. 30. Patent Owner also repeats the assertion that the modification introduces a new principle of operation. PO Reb. Br. 30–31. We are not persuaded for the above-stated reasons.

Further, Patent Owner contends that Dr. Kozyrakis' testimony demonstrates no reasonable expectation. PO Reb. Br. 31–32. Specifically, Patent Owner asserts

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that Dr. Kozyrakis anticipates a mistake when designing a logic circuit that would require storage of an address bit as proposed by Requester 3 and thus teaches away from storing the address bit. PO Reb. Br. 31 (citing 4th Kozyrakis Decl. ¶ 23). We are not persuaded. Dr. Kozyrakis testifies to two mistakes that could occur when remapping logic in its circuit during simulation. 4th Kozyrakis Decl. ¶¶ 22–23. This does not imply there is no reasonable expectation of success of storing an address bit. Rather, Dr. Kozyrakis is highlighting what would occur during functional verification if the logic circuit designer made the identified mistakes. *Id.* Conversely, this paragraph implies that if the mistakes do not occur (e.g., address bit is stored) a successful and error-free simulation will result with proper verification. *See id.*

Finally, we agree with the Examiner's findings and conclusion related to the evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Based on the record, the Examiner has not erred in rejecting claims 2, 5, 21, 23, 30, and 119 when considering the background knowledge of an ordinary skilled artisan or Amidi in combination with JEDEC.

3. *Obviousness Based on Amidi and Dell 2 (Ground 5)*

For this ground, the Examiner adopts the proposed rejection of claims 2, 5, 21, 23, 26, and 30, referring to Requesters 1 and 2 as modified on August 14, 2013. *See* RAN 12. As explained above, we thus disagree with Patent Owner that Requester 2's remarks for this ground are improper. PO Reb. Br. 40. Also, according to the Examiner, Requester 1 proposed to reject claims 2, 5, 21, 23, and 30 on this ground, and Requester 2 proposed to reject other claims. RAN 30; *see also* R1 February 13, 2013 Comments 11–16 and R2 August 14, 2013 Comments

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5–17 (citing Amidi ¶¶ 8, 40–43, 45–52, 71; Dell 2, Abstract, 2:40–3:5, 4:62–6:14, 8:5–64; 3d Bagherzadeh Decl. ¶¶ 12–17, 21–22, 24, 26, 37; and 2d Bagherzadeh Decl. ¶ 25).

As a preliminary matter, Requester 1 contends that claim 119 was missing from the Examiner's listing of its claims proposed to be rejected under Ground 5. R1 Resp. Br. 14 (citing RAN 30). Claim 119 is also missing in the summary of the adopted grounds. RAN 12 (omitting claim 119 from Ground 5). Even so, Requester 1 asserts that claim 119 should also be adopted due to the Examiner's statement that Amidi and Dell 2 is obvious because the claims are anticipated by Amidi. R1 Resp. Br. 14. Requester 1 also contends that it proposed to reject claim 119 based on Amidi and Dell 2 in its "response to the Second Office Action" at pages "43-48."[21] R1 Resp. Br. 14 n.3. Patent Owner contends that claim 119 has not been rejected. PO Reb. Br. 38. The Examiner fails to comment on the status of claim 119 in the Examiner's Answer.

Upon review, we agree that Requester 1 did propose to reject claim 119 based on Amidi and Dell 2 and that claim was omitted from the Examiner's listing of the proposed rejection in the RAN. R1 February 13, 2012 Comments 43–44; RAN 30 (listing only claims 1–43 and 45–50 when addressing Requester 1). Even so, the adopted rejection does not include claim 119. RAN 30. We thus ultimately agree with Patent Owner that claim 119 has not been rejected under Ground 5.

Turning to the merits of the rejection, Patent Owner does not address Dell 2 in its opening brief. *See generally* PO App. Br. In its rebuttal brief, Patent Owner contends that the rejection "presumably relies on Amidi's teachings alone as the

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[21] We assume this response is Requester's Comments filed February 13, 2012 entitled "THIRD PARTY REQUESTER COMMENTS AFTER NETLIST RESPONSE TO THE SECOND OFFICE ACTION."

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Examiner found the combination of Amidi and Dell 2 deficient." PO Reb. Br. 14
(citing RAN 30). We disagree. Although some portions of the RAN discussed
that claims 2, 5, 21, 23, 30, and 33 are rejected based on Ground 3 (RAN 30), the
Examiner adopts the proposed rejection of Requesters 1 and 2 as modified on
August 14, 2013, which is the date Requester 2 filed comments, in other portions
as previously explained. *See* RAN 12.

Accordingly, when viewing the RAN as a whole, the adopted rejection does
not just rely on Amidi, but also on Dell 2. We therefore determine that the
Examiner has adopted Requester 2's proposed rejection, including that concerning
the "storing" feature. Moreover, any discussion related to Requester 1 and a lack
of motivation to combine Amidi with Dell 2 (RAN 31) is addressed in the context
of the non-adopted rejection of other claims based on Amidi and Dell 2.

As for the pending rejection, we refer to the reasoning above concerning
Amidi, Dell 2, the background knowledge of one skilled in the art, and inferences
and creative steps one skilled in the art would have employed. Additionally,
regarding Dell 2, we refer to the further findings discussed by Examiner. *See* RAN
12, 32 (discussing Dell 2, 2:48–59); Requester 2's August 14, 2013 Comments 60–
61 (referring to claim 2), 40–41 (citing Dell 2 8:36–41, which discusses the need to
store bank address values applicable to each option). That is, Dell 2 also teaches
that one skilled in the art would have recognized storing signals for later use,
including during a column access procedures, to ensure the correct bank is
addressed. Dell 2 8:36–40. Moreover, Requester 2 provides additional
explanation concerning this rejection and Dell 2, which is essentially undisputed.
R2 Resp. Br. 21–22.

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Patent Owner also refers to its arguments in its Respondent Brief to Requester 1's appeal. PO Reb. Br. 39 (citing PO-R1 Resp. Br. 12–20). The arguments essentially repeat the discussions above concerning standard and compliant memory modules, how bank addresses are used in JEDEC designs, and there is no reason provided to combine the references. PO-R1 Resp. Br. 12–16. We are not persuaded for reasons previously discussed. That is, as discussed above, the combined teachings of the references suggest to a skilled artisan that modifying Amidi's CPLD, to the extent necessary, to store an input signal (e.g., an input signal used to perform expansion) during a row access procedure for subsequent use during a column access procedure would have been obvious.

Finally, we adopt the Examiner's findings concerning secondary considerations evidence not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claims 2, 5, 21, 23, 30, and 33 based on Amidi and Dell 2.

II. Micron and Amidi (Ground 13)

A. Claims 7, 26, and 33 (Claims with Bank Address Limitation)

Claims 7, 26, and 33 are even further rejected based on Micron and Amidi. RAN 14 (referring to Requester 3's proposed rejection). The Examiner refers to Grounds 3 through 6 and states that "[b]ecause these claims are anticipated or rendered obvious by Amidi they are obvious over Micron and Amidi." RAN 49. The Examiner also provides an alternative rejection. RAN 49–52 (stating "[a]lternatively" at RAN 49); November 13, 2012 Non-Final Act. 45–48. This alternative rejection does not specifically discuss Amidi when addressing claims 7, 26, and 33, but discusses Amidi's teaching of creating a four rank transparent memory module fitting into a memory socket intended for two ranks. RAN 51–52.

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For claims 7 and 33, the Examiner also adopted the proposed rejection by Requester 3 that discusses Amidi's teachings and Dr. Kozyrakis's testimony. RAN 14 (indicating Requester 3's proposed rejection is adopted). That is, Requester 3 proposes that Amidi teaches the recited bank address limitation or alternatively one skilled in the art would have known to modify Amidi's CPLD to receive the input signals as recited for purposes of decoding and remapping signals. R3 Request 18–20 (referring to the claim chart in Appendix H), App'x. H, H-14–H-15, H-46.

Patent Owner only presents argument concerning Micron and Amidi individually. PO App. Br. 17–25, 32–34, 44, 46–47. We are not persuaded by such individual attacks. *See In re Merck*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). That is, the arguments that focus exclusively on Micron do not consider the collective teachings of Micron and Amidi as well as what an ordinarily skilled artisan would have recognized. For the previous set forth reasons, we are not persuaded of error by the Examiner and refer to the above discussion concerning Amidi. As discussed previously when addressing Ground 4 based on Amidi, which is referred to the RAN under Ground 13 (RAN 49), we determined that Amidi, when considering its teaching and the background knowledge of an artisan, suggests bank address signals being received by both a logic element and register. Also, as indicated above, claim 33 is anticipated by Amidi.

Moreover, Dr. Kozyrakis states that one skilled in the art would have recognized DDRs, like Amidi's (Amidi ¶¶ 37, 46–49) follow different generation specifications (e.g., DDR-1, DDR-2). Kozyrakis Decl. ¶ 26. Similarly, the '912 disclosure also discusses existing DRAMs at the time of the invention include DDR-1, DDR-2, and DDR-3. The '912 patent 6:15–16, 12:26–27. Dr. Wang acknowledges the same. Wang Decl. ¶ 29. Concerning DDRs, Dr. Kozyrakis

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states an ordinary skilled artisan would have known more recent DDR-2 devices have a bank address field that is 3 bits rather than the conventional two bits used by DDR-1 devices, for example. Kozyrakis Decl. ¶ 26. Patent Owner does not rebut this finding. PO Reb. Br., PO-R3 Resp. Br.

Thus, Requester 3 provides additional evidence that one skilled in the art would have recognized, when using a more recent DDR-2 memory device, bank address signals are free in certain situations for address remapping in particular memory module designs. That is, like Amidi's teaching of using an extra row/column address bit for generating the proper chip-select signals (e.g., rank expansion) for emulating a two rank memory module (Amidi ¶¶ 51, 59), Dr. Kozyrakis provides a reason with some rational underpinning that an ordinary skilled artisan would have used other known, extra address bits (e.g., the extra bank address in more recent DDR devices) to create the desired rank expansion in Amidi by directing such extra signals to Amidi's CPLD.

Patent Owner argues that "bank address signals are not treated in the same way as row and column address signals." PO App. Br. 17 (citing Sechen Decl. ¶¶ 36, 48). Specifically, Patent Owner contends that bank address signals are used to supply certain initialization values to various control registers within DDR DRAM devices, including three identified purposes— (1) define a bank that a read, write, active, or precharge command is applied, (2) program a mode register used to define specific mode operations of a DDR SDRAM, and (3) to identify banks for deactivating an open row during a precharge command). *Id.* (citing Sechen Decl. ¶¶ 36, 48); *id.* at 13–14 (referring to JEDEC 79C 6–7, 11–12, 20). According to Patent Owner, one skilled in the art would not have recognized using bank address signals in a way other than that described by Patent Owner and

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JEDEC 79C, such as directing bank address signals to a CPLD, and such use would result in failure. PO App. Br. 13–17. We are not persuaded.

We have been referred to no evidence of record to support the opinion testimony of Dr. Sechen that directing bank address signals to CPLD would result in failure in Amidi. *See* Sechen Decl. ¶¶ 36, 48. Nor has Patent Owner presented persuasive evidence on this record to provide that the modifications made to Amidi would have been beyond the level of an ordinarily skilled artisan. As such, we agree with Requester 3 that the functionalities of the bank address "would not present a barrier to [implementing] the techniques discussed in the [Patent Owner's] appeal brief." R3 Reb. Br. 2; *see also* R3 Resp. Br. 11–12 (citing 4th Kozyrakis Decl. ¶¶ 16, 19–23).

Additionally, in that the signals connections in Amidi's Figure 6A differ from Figure 6B. Amidi, Figs. 6A–6B, *cited in* Wang Decl. ¶ 20. Specifically, Amidi shows an address signal (e.g., Add(n)) entering CPLD 604 and a different address signal (e.g., Add[n-1:0]) entering register 608 in Figure 6A. Amidi ¶ 50–52, Fig. 6A. Amidi also shows address signals (e.g., Add[n:0] or A0-12) entering register 608 and one of the same address signals (e.g., Add(n-1) or A11) also entering CPLD 604 during a column address decoding. Amidi ¶ 57–60, Fig. 6B. These differences illustrates two points.

First, Amidi teaches and suggests address signals are being used in a manner that deviate from JEDEC specifications. For example, JEDEC 21-C states address signals are used to define row and column addresses during bank and read commands. JEDEC 21-C 4.20.4-7. But, Amidi uses an extra row or column address signal as an input to the CPLD to generate a rank chip-select signal for emulating a two rank memory module. Amidi ¶¶ 50–52, 57–60, Figs. 6A–B.

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Thus, an ordinary skilled artisan in logic circuit design would have recognized based on Amidi's teaching to use address signals in an unconventional manner. Second, Amidi also teaches using the same column address signal (e.g., A11) in a memory module for multiple purposes. For example, Amidi teaches in Figure 6B using an address signal (e.g., A11) both to be inputted into a register (e.g., to determine the column within the memory device) and to be inputted into a CPLD (e.g., to select the proper rank). Amidi ¶¶ 57–60, Fig. 6B. Thus, Amidi also illustrates to one skilled in the art that address signals can have multiple purposes.

Granted, the address signals discussed in Amidi are row or column address signals— not the recited bank address signals. But, Dr. Kozyrakis' testimony discussed above concerning certain known DDRs would have an extra bank address bit, coupled with the recognition in the '912 patent that these DDRs existed, provides a reason with some rational underpinning to an ordinarily skilled artisan to use a bank address signal in a manner similar to the Amidi's free row/column address signals. We determine Requester 3 provides adequate evidence that one skilled in the art having (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline, (2) at least two years of experience in designing computer memory systems, and (3) familiarity with JEDEC standards, DRAMS, and DIMMS would have recognized using bank address signals in a manner similar to the row and column address signals taught as being received by Amidi's CPLD.

Patent Owner also refers to previous comments made in its respondent brief to Requester 3. PO Reb. Br. 12–13 (citing PO-R3 Resp. Br. 12–20). Although addressing the rejection based on Micron and Amidi (Ground 13) on page 12 through 20, many of the arguments concerning Amidi are similar to those above

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and have been address previously. *See, e.g.,* PO-R3 Resp. Br. 14–16. Patent Owner also asserts that using a third address bit would present barriers with DDR standard-compliance and cast doubt on a reasonable expectation of success. *See* PO-R3 Resp. Br. 16–20. But, as stated above, Amidi's memory module is not JEDEC compliant. Thus, even if the third address bit is used for other purposes, we explained above that this does not establish that one of ordinary skill would not have recognized also using a free, third address bit in an address remapping scheme. Nor has Patent Owner presented persuasive evidence on this record to provide that the modifications made to Amidi would have been beyond the level of an ordinarily skilled artisan. *See* PO-R3 Resp. Br. 19–20 (citing 2d Kozyrakis Decl. ¶ 25).

According to Patent Owner, both Examiners Choi and Peikari dismissed the position taken by Requester 3. PO Reb. Br. 13. We disagree. As stated previously, the discussion in the Non-Final Action mailed October 14, 2011 was directed to Requester 1's proposed rejection and evidence — not Requester 3. *See* Non-Final Act. 15–16 (discussing Requester 1's proposed rejection). This however does not demonstrate that examiners have dismissed *Requester 3*'s proposal to modify Amidi's CPLD to receive bank address signals. Notably, as discussed above, the record for Requester 3 provides some additional evidence, not presented by Requesters 1 or 2, that one skilled in the art would have recognized, when using a more recent DDR-2 memory device, bank address signals are free in certain situations for address remapping in particular memory module designs. Accordingly, although we determine that Requester 1 and 2's adopted rejections and evidence does not demonstrate that bank address signals are received by Amidi's CPLD (e.g., a logic element), we determine that Requester 3 has provided

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additional evidence sufficient to demonstrate that one skilled in the art would have recognized using extra bank address signals to be received by Amidi's CPLD for a remapping scheme to generate the needed rank signals.

Given that one skilled in the art have recognized that: (1) Amidi is unconventional memory module that is not compliant with JEDEC design specifications in various ways, (2) Amidi teaches emulating memory module having a lower rank of the memory devices by using extra address signals to generate the necessary chip-select signals for the actual memory device, (3) Amidi teaches address signals, including bank address signals, have multiple purposes, and (4) some DDR devices include bank address bits that are free to be used in certain situations, we determine that an ordinarily skilled artisan would have known to direct bank address signals to Amidi's CPLD in a similar manner to the row/column address signals explicitly taught by Amidi. As such, we disagree with Patent Owner that the record does not demonstrate to direct bank address signals to Amidi's CPLD such that they are received by both a register and a logic element (e.g., CPLD) as recited in claim 7.

Lastly, we adopt the Examiner's findings and conclusion concerning the secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claims 7, 26, and 33 based on Micron and Amidi.

B. Claim 21 (Claim with Storing Limitation)

As for claim 21, the proposed rejection for Requester 3 is similar to those for Requesters 1 and 2. *See* RAN 49 (referring to Grounds 3–6) and R3 Request, App'x H, H-29–H-30 (citing Amidi ¶ 61 and Kozyrakis Decl. ¶ 26). Patent Owner repeats that the Examiner relies upon Amidi's "Figure 6" and the input RAS and

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output rRAS. PO App. Br. 33. As indicated above, the Examiner only relies on this finding for part of the adopted rejection. Patent Owner further asserts the Examiner has not identified a column access procedure. *Id.* Moreover, Patent Owner repeats the argument concerning the signals in the register of Amidi are gone during any subsequent column access procedure and that Amidi would be standardized and have conventional DDR command operations. PO App. Br. 33–34.

We disagree and refer to the above discussion of Amidi when addressing Ground 4 for more details. We also adopt that the Examiner's findings and conclusion related to evidence of secondary considerations not outweighing the case for obviousness. RAN 65–66.

Accordingly, we are not persuaded that the Examiner erred in rejecting claim 21 based on Micron and Amidi.

Remaining Rejections (Grounds 9, 11, 12, and 19)

The above discussions address all the claims on appeal and are dispositive, rendering it unnecessary to reach the propriety of the remaining, adopted rejections. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009); 37 C.F.R. 41.77 (a) ("The Patent Trial and Appeal Board . . . may affirm or reverse each decision of the examiner on all issues raised on each appealed claim.")

III. Withdrawn or Non-Adopted Rejections

The Examiner withdrew or did not adopt the following proposed rejections:

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Reference(s)	Basis	Claims	RAN
Amidi (Ground 3)	§ 102	1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46	RAN 11
Amidi (Ground 4)	§ 103(a)	1, 3, 4, 6, 8, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135	RAN 12
Amidi and Dell 2 (Ground 5)	§ 103(a)	1, 3–4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136	RAN 12
Amidi and JEDEC (Ground 6)	§ 103(a)	56, 60–63, 90, 91, 109–111, 127, and 131	RAN 12
Murdocca and Dell 2 (Ground 7)	§ 103(a)	1–11, 14, 15, 19, 21, 23–25, 28–34, 36, and 39–42	RAN 12
Micron and Amidi (Ground 13)	§ 103(a)	1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31,	RAN 14

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		32, 36–39, 41–43, 45, 50, 52–54, 56,[22] 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136	
Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)	§ 103(a)	1, 15, 28, 39, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136	RAN 14
Amidi and Dell 184 (Ground 20)	§ 103(a)	52–54, 56, 67–71, 77–79, 82–84 and 87–89	RAN 15
Micron, Amidi, and Olarig (Ground 21)	§ 103(a)	52–54, 67–71, 77–79, 82–84, and 87–89	RAN 15
Micron, Amidi, Olarig, and Memory Explained (Ground 22)	§ 103(a)	56	RAN 15
Lack of written description (Ground 14)	§ 112, ¶ 1 (pre-AIA)	57, 58, 60, 68, 79, 84, 89–91, and 128–131	RAN 14

R1 App. Br. 6–7; R3 App. Br. 2–3.

We will address Requesters 1–3 appeals separately.

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[22] As noted by Patent Owner, claim 57 is presently rejected under Micron and Amidi (Ground 13). RAN 98; PO-R3 Resp. Br. 6. We thus omit claim 57 from the non-adopted rejections under Grounds 13 and 19.

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1. Requester 1's Appeal

Requester 1 appeals the Examiner's decision not to adopt the proposed rejections of various claims based on Ground 3–7 and 14. R1 App. Br. 6–7. Requester 1 generally asserts that the subject matter of the claims that the Examiner confirmed "is actually directed to engineering design choices not properly entitled to patentable weight" and that "patentability [has been] based on design choices that would normally be readily dismissed[.]" R1 App. Br. 7. Requester 1 further asserts that the proper level of skill in the art has not been contemplated. *See* R1 App. Br. 8.

a. Amidi (Grounds 3)

Independent claim 52 is illustrative and recites a logic element generating a CAS or chip-select signal in response in part to an input bank address signal. Concerning Ground 3, Requester 1 explicitly states "[f]or purposes of this appeal" that it "focuses on the obviousness rejection," which is Ground 4. R1 App. Br. 16. By focusing on the obviousness rejection, Requester 1 has not discussed any error in the Examiner not adopting the anticipation rejection (Ground 3) of various claims based on Amidi. PO-R1 Resp. Br. 11 (stating that Requester 1 has waived the "ground in substance.")

However, Requester 1 expressly discusses what Amidi discloses. R1 App. Br. 8–11. From this discussion, Requester 1 asserts Amidi discloses receiving a bank address signal input in Figure 6A (R1 App. Br. 10) and that this circuit matches exactly Figure 1A and 1B of the '912 patent showing bank address input signals and chip-select output signals (R1 App. Br. 10–11). Amidi's Figure 6A shows bank address signals inputted into Register 608 and rCAS signals outputted out of Register 608. Yet, other signals are also outputted out of Register 608,

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including but not limited to rRAS, rAdd[n-1:0], and rWE. Amidi, Fig. 6A. As such, we do not find Requester 1's evidence probative that Amidi's Figure 6A discloses a logic element that generates a CAS signal *in response* at least in part to a bank address signal of the set of input control signals. *See* RAN 26–27. Also, as discussed above when addressing Patent Owner's appeal, Requester 1's comments, and the Examiner's response to Requester 1's comments, we determined that Amidi does not disclose a bank address signal inputted into CPLD 604 (e.g., a logic element) in Figure 6A. *Id.*

We additionally adopt the Examiner's comments related to Ground 3 and agree that Requester 1 and 2's comments do not illustrate Amidi discloses the limitation of generating a CAS or chip-select signal in response to a bank address signal as recited in claim 52 and other independent claims of similar scope. RAN 26–27.

We therefore refer to the above discussion related to Ground 3 and sustain the Examiner's decision not to adopt the anticipation rejection (Ground 3) of various claims based on Amidi.

b. *Amidi (Grounds 4 and 6)*

Concerning Ground 4, we must further consider what an ordinarily skilled artisan would have known, along with the creativity and common sense of a person of ordinary skill, and what Amidi would have suggested to one skilled in the art to determine whether the claimed invention would have been obvious under 35 U.S.C. § 103. *See* PO-R1 Resp. Br. 11. Requester argues claims 1, 15, 28, 39, 52, 58,[23] 67, 77, 82 and 87 as a group. R1 App. Br. 15–18; R1 Reb. Br. 4–7. These claims recite the same or similar recitations. We select claim 1 as illustrative.

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[23] Claim 58 depends from independent claim 57, which was not argued.

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Claim 1 recites, in pertinent part, "wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals." Concerning this limitation, the RAN states

> Requester 1 has not presented any evidence of obviousness of modifying Amidi's circuits to generate CAS or chip-select signals in response to a bank address signal. As discussed above, in Amidi, bank signals are stored in registers and transmitted as output signals. They are not used to generate any other control signal. Conclusion of obviousness requires some teaching of usage of bank signals to generate control signals and *an articulation of some reason to combine the teaching with Amidi's teaching with some rational underpinning to support the conclusion.* Requester 1 has provided neither.

RAN 75–76 (emphasis added). For the following reasons, we agree with the Examiner.

As noted previously when addressing Grounds 4 and 6, the Examiner concluded that Amidi teaches or suggests that one skilled in the art would have recognized that bank address signals are received by the registers 408 and 418 and that one of these registers is mapped to the recited "register" and the other to the recited "logic element" in claim 7. RAN 28 (referring to the discussion of Ground 3 at RAN 24), 69, 74. However, we further agree that the record presented by Requester 1 does not provide sufficient evidence that one would have known to direct bank address signals to Amidi's CPLD. That is, other than the mere assertions presented by Dr. Wang to direct bank address signals to a CPLD to provide for "flexibility" and "various design goals" (*see, e.g.,* Wang Decl. ¶¶ 17, 19, 24), there is insufficient evidence to substantiate that one skilled in the art would have recognized to direct bank address signals in Amidi to CPLD 604. Accordingly, as the Examiner found, we agree that there is an insufficient rational

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underpinning to support that the non-adopted claims are obvious based on Amidi's teachings.

Citing to paragraph 62, Requester 1 asserts Amidi teaches generating a command signal in response to another command signal. R1 App. Br. 17 (citing Amidi ¶ 62). Amidi discusses a CPLD receiving command (e.g., cs0, cs1) and address signals (e.g., Add(n)) from a controller to determine the correct rank to activate (e.g., rcs0–3). Amidi ¶¶ 60, 62, Figs. 6A–B, 7. Despite Requester 1's urging (see R1 App. Br. 17), there is no discussion to use a bank address signal (e.g., BA) to generate the chip-select (e.g. cs0, cs1) signal as recited in claim 1. See RAN 26; PO-R1 Resp. Br. 9–10.

Next, relying on Dr. Wang's testimony, Requester 1 contends that one skilled in the art would have known of techniques that use bank address bits to generate chip-select signal. R1 App. Br. 17 (citing 3d Wang Decl. ¶ 14). Requester 1 asserts that the type of transition bit (e.g., row, column, or bank) used by logical circuit design of memory density multiplication is "a simple design choice." R1 App. Br. 17 (citing RAN 75). Requester 1 further points to Dr. Wang's testimony in his first declaration to support one skilled in the art would have known to reassign address signal, including bank address signals, depending on the application. R1 Reb. Br. 5–6 (citing Wang Decl. ¶¶ 10–15, 19–21).

We indicated previously that Dr. Wang's testimony is uncorroborated. Although we recognized that bank address signals, along with row and column address signals, play a role in determining the location of memory in DRAMs (Wang Decl. ¶¶ 11–15), that relationship by itself does not provide a sufficient reason to substitute a bank address signal for the extra row and column address signals used in Amidi to generate chip-select signals. Amidi ¶¶ 51, 59. As such,

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we agree with the Examiner that Requester 1 has not provided an adequate reason with a rational underpinning that Amidi in combination with background knowledge of an ordinarily skilled artisan or JEDEC would yield the recited "logic element [that] generates . . . chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals" in claim 1. Moreover, Requester 1's "design choice" rationale does not provide ample reason to use interchangeably one signal over another for generating the chip-select signals in Amidi. *See* R1 App. Br. 16–17.

Notably, we agree with Patent Owner that Exhibit A,[24] which Dr. Wang discusses (3d Wang Decl. ¶ 14), forms no part of the rejection of Ground 4 as currently proposed. RAN 27; PO-R1 Resp. Br. 12. That is, the rejection as formulated relies solely on Amidi (Ground 4) or Amidi and JEDEC (Ground 6). RAN 27, 32–33. Nor as explained above, does Exhibit A illustrate or teach a feature in Amidi or does Dr. Wang illustrate that one skilled in the art would have recognized using an Intel® 450NX PCIset with Amidi's memory module. *See* 3d Wang Decl. ¶ 14; R1 App. Br., Evid. App'x, Ex. A. We therefore comment no further on Exhibit A.

Requester 1 further contends that the language "in response at least in part to" in claim 1 is ambiguous and should not be construed as "use." R1 App. Br. 17–18 (citing RAN 75). Rather, Requester 1 argues the limitation should be construed broader than the Examiner's understanding. R1 App. Br. 17. Yet, Requester 1 provides no alternative construction that would lead one skilled in the art to conclude that Amidi teaches or suggests the disputed limitation. *See id.*; PO-R1 Resp. Br. 14. Given the record, we agree with the Examiner that his

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[24] Exhibit A is entitled "Intel® 450NX PCIset, Rev. 1.3" (March 1999).

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construction of this phrase is reasonable. *See* RAN 27 (stating "[i]f the bank signal is not used in any way to generate the output signals, the generation of output signals cannot be in response to the bank signal.")

Based on Requester 1's proposed rejection and evidence, one skilled in the art would not have recognized (1) receiving bank address signals at Amidi's CPLD and thus (2) generating chip-select signals in response to the bank address signals. We thus determine that the proposed rejection does not teach or suggest to an ordinarily skilled artisan the recitation of "the logic element generates . . . chip-select signals of the output control signals in response at least in part to a bank address signal of the set of input control signals" in claim 1. Requester 1 also does not provide any additional evidence of generating gated CAS signals in response at least in part to a bank address signal as recited. *See* R1App. Br. 15–18.

Patent Owner contends similar limitations to independent claim 1 are found in independent claims 15, 28, 39, 52, 67, 77, 82, and 87. PO-R1 Resp. Br. 9. We agree that these claims recite either generating a chip-select, CAS, or a rank-selecting signal in response at least to a bank address signal. As such, we further determine that the Examiner did not err in not adopting the rejection of these claims for the same reason as discussed above when addressing claim 1.

Concerning independent claim 16, Requester 1 argues that Amidi teaches the limitation of "the command signal is transmitted to only one DDR memory device at a time." *See* R1 App. Br. 18 (citing Amidi ¶ 61); R1 Reb. Br. 9. Amidi discloses that "the Column address needs to be provided with its proper control and command signals in order to read or write to that particular cell." Amidi ¶ 61. Requester further relies on Dr. Wang and Murdocca to support that Amidi

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inherently teaches claim 16. R1 App. Br. 18 and R1 Reb. Br. 9 (citing 2d Wang Decl. ¶ 13 and Murdocca 248).

We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. *See* Amidi ¶ 61. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. R1 App. Br. 18; R1 Reb. Br. 9. Yet, as the Examiner indicates:

> Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. . . . . The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank.*

RAN 29 (emphasis added).

That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A–6B (stating "Signals to Memory Devices" at the far right) Moreover, Amidi's Figures 6A and 6B undermines Requester 1's assertion that delivering command signals to two or more memory cells at a time would create data bus contention. *See* R1 Reb. Br. 9. That is, Amidi's Figures 6A and 6B further teach or suggest that the command signal is transmitted to a cell within *multiple* memory devices at a time. Thus, although Dr. Wang's testimony states that the RAS and CAS signals are used to isolate a particular memory cell in an array of a memory device (2d Wang Decl. ¶ 13), there is countering evidence in

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Amidi to demonstrate that isolating a cell relates to isolating a cell within multiple memory devices at the same time.

Lastly, Murdocca does not form any part of the rejection based on Grounds 4 and 6. *See* R1 App. Br. 18. Even so, Murdocca's cell that is formed by an intersection of the row and column address does not refute Amidi's teaching that the command signals are transmitted to memory *devices*.

Accordingly, we are not persuaded that the Examiner erred in not adopting the rejection of claims 16 and 132, which has similar limitations, based on Amidi or Amidi and JEDEC.

Requester 1 provides arguments for dependent claims 17 and 133. R1 App. Br. 18–19. We will sustain the Examiner's decision not to reject these claims, because these claims depend from claim 16 and claim 132 respectively.

As for dependent claim 58, Requester 1 argues the rejection of this claim should be adopted based on its previous contention. R1 App. Br. 18. As discussed above, claim 57, from which claim 58 depends is not disputed. PO App. Br. 47. Claim 58 has similar limitations to claim 1. Thus, for the above reasons when addressing claim 1, we will sustain the Examiner's decision not to reject claim 58 based on Amidi.

Requester 1 further argues specifically that dependent claims 56 and 60 should be rejected based on Amidi and JEDEC (Ground 6). R1 App. Br. 25–26. These claims depend indirectly from claims 52 and 57 respectively. Because we agree that the Examiner did not err in not adopting the rejection of claims 52 and

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57, we also determine the Examiner did not err in not adopting the rejection of claims 56 and 60.[25]

Accordingly, we sustain the Examiner's decision not to reject claims 1, 15–17, 28, 39, 52, 56, 58, 60, 67, 77, 82, 87, and 132 and the remaining claims not separately argued based on Amidi alone and in combination with JEDEC.

c. Amidi and Dell 2 (Ground 5)

Requester 1 disputes the Examiner non-adoption of the proposed rejection of claims 1, 3, 4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136 based on Amidi and Dell 2. R1 App. Br. 7; RAN 12. The Examiner states "the assertions [presented by Requester 1] fail to provide any reason why one of ordinary skill in the art at the time the invention was made would have been motivated to combine the Amidi and Dell 2 systems. Absent a motivation to combine these references, the combination is deemed unobvious." RAN 31.

Requester 1 again argues the claims as a group, and we select claim 1 as illustrative. First, Requester 1 argues that the Examiner erred in determining that, because no motivation was provided to combine Amidi with Dell 2, the combination is deemed unobvious. R1 App. Br. 20 (citing RAN 31). Requester 1 argues that there are several places where motivation was provided. R1 App. Br. 20 (citing 3d Wang Decl. ¶ 16, quoting a portion of the February 13, 2013 Comments, and incorporating the R1 Request), 21–25 (citing 3d Wang Decl. ¶ 10–16).

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[25] Similar claim limitations to claims 56 and 60 were addressed by another panel in another reexamination proceeding. See Google Inc. v. Netlist, Inc., Appeal No. 2014-007777, 2015 WL 799035, at *3–7 (PTAB February 24, 2015) (affirming a similar limitation based on Amidi and JEDEC for U.S. Patent No. 7,289,386) (ordering appeal dismissed at Netlist, Inc. v. Google Inc., No. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016)).

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The original request provides a reason with some rational underpinning for combining Amidi and Dell 2, including

> It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the methods for emulating larger RAMs using smaller RAMs disclosed in '152 publication with the logic element disclosed in the '074 patent to realize larger memory capacity at a lower cost.

R1 Request 162. The original request also states Dell 2 teaches addressing the demand for increased memory capacity and to overcome certain related compatibility issues. R1 Request 159–160 (citing Dell 2, 2:32–38). Additionally, Dell 2 discusses an address remapping function that provides a memory module with "more flexib[ility] in terms of its compatibility with different computer systems" and further creates a computer systems, which permits "dynamically to negotiate available memory module functions and modes." Dell 2, 2:33–36, *cited in* R1 Request 159. Thus, Dell 2 provides another reason to be combined with Amidi. We further note whether or not the Dell 2's memory devices can be bodily incorporated into Amidi's system is not the test for obviousness. *See In re Keller,* 642 F.2d 413, 425 (CCPA 1981)). "Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *Id.*

We therefore disagree with Patent Owner that Requester 1's explanation is merely "a technological result of what Requester 1's expert had the capability of building" or that Requester 1 provides no reason to combine Amidi and Dell 2. PO-R1 Resp. Br. 16.

On the other hand, Amidi teaches emulating a smaller memory module by using an address signal, such as an extra row or column line, but does not specifically discuss using a bank address line. We refer to our above discussion of

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Grounds 4 and 6 for any details concerning Amidi and the evidence of record concerning what an ordinary skilled artisan would have recognized based on Requester 1's proposed rejection. As such, although Requester 1 provides a reason to combine Dell 2 with Amidi, the question remains whether the references when combined teach or suggest generating a chip-select, CAS, or rank selecting signal in response to a bank address signal.

As proposed, Dell 2 teaches remapping an address signal as a bank address signal using a logic circuit when the memory devices of memory module are configured for M banks but bank address signals inputted correspond to N bank memory devices. Dell 2, Abstract, 4:43–49, *cited in* R1 Request 162. This remapping is done, according to Requester 1, in order to save the bank address later for a CAS sequence. *See* R1 App. Br. 21. Requester 1 argues that this discussion in Dell 2 teaches that a logic element that generates a CAS signal in response to a bank address signal as recited in claim 1, because "the ASIC device will drive the stored output signal during a CAS command *depending on the bank address input.*" *Id.* (citing 3d Wang Decl. ¶ 10).

Notably, Dell 2 is silent about driving a CAS command based on a bank address signal. Rather, as understood, the bank address is stored for later use, such as "the CAS sequence and each subsequent sequence for which the ASIC 24 has to address the correct bank." Dell 2, 9:32–34. Dr. Wang similarly testifies that a A12 signal is remapped to a BA1 signal and saved for later use "for the targeted bank." 3d Wang ¶ 10. Dr. Wang further testifies "the ASIC device will drive the stored output signal during a CAS command *depending on the bank address input.*" *Id.* However, other than a mere assertion, there is no evidence to support this position. *Id.* We thus do not find this evidence probative.

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Also, some of Requester 1's discussion focuses on storing a signal for subsequent use during a column access procedure (i.e., the storing limitations). R1 App. Br. 20–21. However, the claims at issue in the non-adopted rejection based on Amidi and Dell 2 include recitations that differs from the storing limitations previously discussed, including claim 1 reciting particular input and output signals of the logic element. Requester 1 does not address sufficiently why one skilled in the art would have recognized claim 1's limitations were obvious over Amidi and Dell 2 as proposed.

Requester 1 also presents "Figure 1" through "Figure 3," which are not found in Dell 2, to show how bank address signals are outputted from a logic element to memory devices. R1 App. Br. 22–24. According to Requester 1, these figures are derived from Dr. Wang's testimony. R1 App. Br. 23–26 (citing 3d Wang. Decl. ¶¶ 11–16). Yet, this evidence is not probative due to the lack of corroborating evidence. Even so, we note that "Figure 1" and "Figure 2" do not show an input bank address signal being used to generate the CAS signal. As for Figure 3, the record has insufficient supporting evidence, other than Dr. Wang's "belief." 3d Wang Decl. ¶ 15 (further referring to Intel 452NX RAS/CAS generator device that forms no part of Grounds 3–5).

On the other hand, we note that the discussion of Amidi's CPLD receiving bank address signals (e.g., bank address limitation in claim 7) based on Dell 2's teachings as previously discussed, does provide some evidence of generating a chip select or rank select signals in response at least in part to a bank address signal. We first refer to the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach. In our discussion, we found that Dell 2 provides a teaching or suggestion to

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direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1). *See also* R2 August 14, 2013 Comments 29–30, 37–38 (discussing different memory devices or densities of memory devices known by ordinary artisan for use with Amidi). We refer above for further details.

In Requester 1's respondent brief to Patent Owner's cross appeal, Requester 1 further contends that claim 119 should be included in the rejection based on Amidi and Dell 2. R1 Resp. Br. 14–19 (citing RAN ¶ 44, 49); R1 Resp. Br. 3. Patent Owner asserts Requester 1 improperly raised this issue because the response does not address an alleged error in Appellant's argument. PO Reb. Br. 38. We determine it is unnecessary to reach the propriety of this non-adopted claim, because of above discussions related to affirming the rejection based on Grounds 4 and 6 when addressing Patent Owner's cross appeal.

We further determine that the Examiner did not err in not rejecting claims 16 and 17 for the above reasons. Requester 1 does not address how Dell 2 cures the missing features of Amidi.

Lastly, we agree with the Examiner's findings and conclusion that the secondary evidence does not outweigh the case for obviousness.

Requester 1 states claims 120–122 and 132–136 were proposed to be rejected under Ground 5 and that these claims are missing from the Examiner's list of the proposed claims. R1 App. Br. 19–20 (referring to RAN and February 13,

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2012[26] Comments). Patent Owner challenges Requester 1's contention, asserting the disputed claims form no part of the Examiner's rejection for Ground 5. PO-R1 Resp. Br. 2 (citing RAN 12).

We agree the Examiner does not list claim 120–122 and 132–136. RAN 12, 30–31. On the other hand, the Examiner refers to Requester 1's comments of February 13, 2013 (RAN 31), which do include claims 120–122 and 132–136 in the heading of the proposed rejection based on Amidi and Dell 2. R1 February 13, 2013, Comments 10. Moreover, the February 13, 2012 Comments discuss these claims in more detail. *See* R1 February 13, 2012 Comments 43–48. The Examiner thus should have considered these claims. We adopt Requester 1's position in the February 13, 2012 Comments for purposes of this Opinion. *See id.* (further referring to claim charts in R1 Request).

For the above reasons, we do not sustain the Examiner's decision not to reject (1) claims 1, 120–122, and 132–136, (2) claims 15, 28, and 39, which recite similar limitation to claim 1, and (3) the remaining claims not separately argued under § 103 based on Amidi and Dell 2. We sustain the Examiner's decision not to adopt the proposed rejection for claims 16 and 17 and do not reach the propriety of the non-adopted rejection of claim 119.

d. *Murdocca and Dell 2 (Ground 7)*

Requester 1 asserts the Examiner's decision not to adopt the proposed rejection of Murdocca and Dell 2 was in error. R1 App. Br. ii (listing claims 1–11, 14, 15, 19, 21, 23–25, 28–34, 36, and 39–42), 26–29; R1 Reb. Br. 12–13. We note

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[26] Notably, there are no comments filed on February 13, 2014 by Requester 1. R1 App. Br. 19. Also as previously noted, Requester 1 filed comments on both February 13, 2012 and 2013. We presume Requester 1 intended to refer to the comments filed on February 13, 2012.

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that the Examiner indicated that Requester 1 has failed to raise a substantial new question (SNQ) of patentability based on Murdocca and Dell 2. September 1, 2010 ACP 11 and Order Granting/Denying Request for Reexamination for Inter Partes Reexamination 7–8. Given the Examiner's determination that there is no SNQ for this proposed rejection and such a determination is final, we agree that this ground is not appropriate for appeal. *See* PO-R1 Resp. Br. 21(citing 37 C.F.R. § 1.927). Moreover, given that there was no SNQ for this ground, we determine that the additional statements made by the Examiner beyond the determination that there is no SNQ and concerning the "non-adoption of the proposed claim rejection" (R1 Reb. Br. 12 (underlining omitted)) for Ground 7 are superfluous. We will not address this proposed rejection any further.

e. *Lack of Written Description Support (Ground 14)*

Requester 1 argues that the Examiner erred in not adopting the proposed rejection under 35 U.S.C. § 112, first paragraph (pre-AIA) of claims 57, 58,[27] 60, 68, 79, 84, 89–91, and 128–131 for failing to satisfy the written description requirement. R1 App. Br. 29–32; R1 Reb. Br. 13–15. To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. *See, e.g., Moba, B.V. v. Diamond Automation, Inc.,* 325 F.3d 1306, 1319 (Fed. Cir. 2003).

Claims 57 and 128 recite in pertinent part "the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase[-]lock loop device." R1 App. Br., Claims App'x 18–19, 29. We select claim 57 as illustrative.

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[27] Claim 59 has been canceled.

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For claim 57, Requester 1 argues that Figures 1A and 1B of the '912 patent disclose logic element 40 as an empty box, failing to show how the box operates. R1 App. Br. 29–30. Additionally, Requester 1 states that one skilled in the art would not have known for certain how the signals from PLL 50 were used by logic element 40 and the corresponding disclosure provides no relationship between the output signals and the clock signals received from PLL 50. R1 App. Br. 30 (citing the '912 patent 5:25–31, 6[28]:55–63). Requester 1 and Patent Owner alike (R1 App. Br. 30; PO-R1 Resp. Br. 23) reproduce Figure 1A of the '912 patent but arrive at opposite conclusions concerning whether the '912 patent provides written description support for claim 57. R1 App. Br. 29–31, PO-R1 Resp. Br. 22–24.

Like the Examiner (RAN 53), we find Requester 1's arguments unavailing.

Referring to Figure 1A of the '912 patent reproduced earlier in this Opinion, this figure shows only chip select signals (e.g., CS_{0A-1B}) exiting PLL 40 and thus provides support for the recitation "the logic element generates a first number of chip-select signals of the set of output control signals" within claim 57. The '912 patent, Fig. 1A.

As for the remaining recitation that these signals are "in response at least in part to clock signals received from the phase[-]lock loop device," we note the figure also shows a clock signal from PLL 50, as well as other signals from the computer system (e.g., CS_{0-1}, A_{-n+1}, command signals, BA_{0-m}), enter logic element 40. The '912 patent 5:8–9, 28–36, Fig. 1A, *cited partly in* PO-R1 Resp. Br. 23. Although there is no discussion of the specific details of what happens within logic element 40 within these passages, Figure 1A shows the signals that enter logic element 40, including the clock signal of PLL 50. One skilled in the art would

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[28] Requester 1 mistakenly stated column 5 rather than column 6.

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have reasonably concluded that the signals that enter logic element 40 have some purpose and affect the output signals which are *only* chip-select signals (e.g., $CS_{0A}-CS_{1B}$).

Requester 1 further contends that column 6 does not mention the clock signal when discussing the output control signals. R1 App. Br. 30 (citing the '912 patent 6:55–63). Yet, this passage discusses output signals that "include[] address signals and command signals" (the '912 patent 6:62–63)— not chip select signals— and in *certain* embodiments (the '912 patent 6:55–56), such as those shown in Figures 2A–3B— not Figure 1A. Requester 1 even further asserts that the clock signals can be used in various ways, "including counting, synchronization, timing, phase shifting, frequency multiplication, frequency division, etc. and that the '912 patent does not disclose the specific use of the signal from the phase lock loop." R1 App. Br. 31 (citing Wang Decl. ¶ 16). Even assuming Dr. Wang is correct, this evidence does not demonstrate sufficiently that one skilled in the art would not reasonably conclude that the clock signal is not used in some manner, whether directly or indirectly, to generate the chip select signals shown in Figure 1A.

Patent Owner further notes that the '912 patent discloses an exemplary Verilog code used for memory density multiplication that includes various logic transactions that occur at a positive or negative edge of a PLL clock signal. PO-R1 Resp. Br. 23–24 (citing the '912 patent 14:5–10, 20–23, cols. 13–19). In response, Requester 1 contends that Patent Owner introduces the Verilog code for the first time in the briefs. R1 Reb. Br. 13. Requester 1 contends that there is no expert testimony to support Patent Owner's position concerning the code and that Owner relies solely on attorney argument that should be given no weight. R1 Reb. Br.

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13–14. To be sure, mere attorney argument cannot take the place of evidence in the record and is not probative. *See Estee Lauder Inc. v. L'Oreal, S.A.,* 129 F.3d 588, 595 (Fed. Cir. 1997). However, this position is not merely an argument and has support in the '912 patent.

That is, the code in Example 1 (the '912 patent, cols. 13–18) describes logic element 40 receiving one chip-select signal and generating two output chip-select signals to achieve memory density multiplication. The '912 patent 14:17–23. In this example, the code includes the phrases "always@(posedge clk_in)" and "always@(negedge clk_in)" to begin certain operations. *See, e.g.,* the '912 patent, cols. 13 and 17. As such, Patent Owner's position is supported by the '912 patent's disclosure itself. Given the code, one skilled in the art would have recognized that the certain actions of logic element 40 that translate one input chip-select signal into two output chip-select signals occur at the positive and negative edges of the input clock signal.

Lastly, Requester 1 turns to Dr. Wang in arguing that one skilled in the art "could not have known for certain how the signal from the phase locked loop was used by the logic element of the '912 Patent[.]" R1 App. Br. 30 (citing Wang Decl. ¶ 16). Dr. Wang testifies that the '912 patent discusses the PLL being operatively coupled to the logic element, which means that the PLL is electrically connected directly or indirectly to the logic element. Wang Decl. ¶ 16, *cited in* R1 App. Br. 30–31. However, Dr. Wang determines that a digital logic circuit designer "could not have known for certain how the signal from the phase locked loop was used by the logic element of the '912 Patent[.]" *Id.* Even presuming Dr. Wang's statement is correct that one skilled in the art would not have to know exactly how the signal was used, one skilled in the art would still conclude

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reasonably that the signal was used in some fashion or "in part" to generate the output signals as previously discussed.

To the extent that this argument is further asserting that there is no support in the disclosure to support the phrase "operatively coupled" in claim 57 (*see* R1 App. Br. 31 and R1 Reb. Br. 14 (citing Sechen Decl. ¶ 15)), we disagree. Figure 1A above shows the PLL coupled electrically to memory devices 30, logic element 40, and register 60 (e.g., lines connects PLL to these components).

Based on the above discussion and Figure 1A in the '912 patent, we determine at minimum that an ordinarily skilled artisan looking at this figure would have reasonably concluded that the clock signals that enter logic element 40, which include clock signals from PLL 50, have some effect on the output signals of logic element 40. We thus agree with the Examiner and Patent Owner that logic element 40 uses the input clock signal from PLL 50 *at least in part* to generate the output chip select signals in Figure 1A. *See* RAN 53; PO-R1 Resp. Br. 23. Accordingly, we further determine that the '912 patent's disclosure describes in sufficient detail of the features of claim 57 that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention.

Claims 68, 79, 84, and 89 recite "a logic element that is timed to clock signals from a [PLL]." R1 App. Br. 29. We select claim 68 as illustrative. The '912 patent describes PLL 50 transmitting clock signals to logic element 40. The '912 patent 5:28–31, Fig. 1A. Concerning whether the disclosure supports that logic element 40 "is timed to" such signals as recited, Dr. Sechen explains "[b]y providing a single, common clock from the PLL 50 to both the logic element 40 and the register 60, the memory module of claim 1 of the '912 patent is configured to provide reliable synchronous operation." Sechen Decl. ¶ 16. On the other hand,

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Dr. Wang indicates that an ordinary skilled artisan would not know for sure the clock signals are used in such a fashion. Wang Decl. ¶ 16 (stating the signals "could be used for a variety of different purposes.")

For similar reasons to those discussed above in connection with claim 57, we determine that the clock signals transmitted to logic element 40 affects various operations within the logic element at a certain time (e.g., positive and negative edge of the clock signal). The '912 disclosure 14:20–23, cols. 13–18. Moreover, the descriptor itself, a *clock* signal, describes to one skilled in the art that the signal is used for timing. Accordingly, we further determine that one skilled in the art would have reasonably concluded based on the disclosure and Figure 1A that the clock signals from PLL 50 are used for timing as recited.

Finally, both Requester 1 and Patent Owner indicate claims 90 and 91 depend from claim 89. R1 App. Br., Claims App'x 26; PO-R1 Resp. Br. 22. However, a review of the record indicates that these claims depend from claim 39 directly or indirectly and do not recite the limitations discussed previously in this section. *See* January 14, 2012 Response/Amendment 39–40 (claiming that claim 90 depends from claim 39 and claim 91 depends from claim 90). We therefore determine that these claims should not be part of the proposed rejection. However, to extent that we are mistaken, we are not persuaded by Requester 1's argument for these claims for the same reasons discussed previously.

Accordingly, we are not persuaded that the Examiner erred in not adopting the § 112 ¶ 1 rejection of claims 57 and 68 and claims 58, 60, 79, 84, 89–91, and 128–131 which are not argued separately or have similar limitations.

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2. *Requester 2's Appeal*

Requester 2's appeal concerns consideration of US 6,446,184 ("Dell 184") and a proposed rejection of Amidi and Dell 184 under 35 U.S.C. § 103 (Ground 20). R2 App. Br. 1, 10–18; R2 Reb. Br. 1–15. In particular, Dell 184 and the proposed rejection with Amidi was introduced into the reexamination proceeding subsequent to ordering granting reexamination in Requester 2's Comments dated February 13, 2012. R2 App. Br. 9. The Examiner indicated Requester 2's comments were improper. On August 30, 2012, the Office rendered a decision on a petition filed by Requester 2. R2 App. Br. 10. In its decision, the Office determined the introduction of Dell 184 and the newly-proposed rejection based on Dell 184 were improper and denied Requester 2's petition for entry. August 30, 2012 Dec. on Petition 7. Requester 2 seeks review of the Office's decision. August 30 2012 Dec. on Petition 1, 2.

Patent Owner urges us not to review the issues raised in Requester 2's appeal, because they are petitionable matters. PO-R2 Resp. Br. 12 (citing *S. Sales & Mktg. Grp., Inc. v. World Factory, Inc.*, Appeal No. 2012-008958, 2013 WL 5402207, *1 (PTAB January 10, 2013) (concerning Control No. 95/000,104)). We agree. The issues raised by Requester 2 in its appeal brief are not within the jurisdiction of the Board. *See* Manual of Patent Examining Procedure (MPEP) §§ 1002 and 1201, (9th ed. Rev. 07.2015 October 2015); *see also In re Hengehold*, 440 F.2d 1395, 1403–04 (CCPA 1971) (stating that there are many kinds of decisions made by examiners, "which have not been and are not now appealable to the board or to this court when they are not directly connected with the merits of issues involving rejections of claims, but traditionally have been settled by petition to the Commissioner.")

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In response, Requester 2 asserts that the Examiner did not perform the two-part analysis required under 35 U.S.C. § 103, and such failure is appealable. R2 Reb. Br. 5, 7. We disagree. The Examiner did not consider the proposed rejection given the Office's determination that the Examiner did not err in holding the February 2012 Comments non-compliant with Office regulations. August 30, 2012 Dec. on Petition 7–8. As such, the Examiner did not make a determination whether to adopt or not adopt the rejection proposed by Requester 2. And whether another Board panel set aside petitionable matters and addressed related appealable matter,[29] such a decision is not binding on this panel.

As an alternative, Requester 2 urges the Board to remand this proceeding for further consideration for this matter. R2 Reb. Br. 2. Office regulations state the Board *may* remand a reexamination proceeding. 37 C.F.R. § 41.77(a), *cited in* R2 Reb. Br. 2. We will not exercise our discretion to remand for further consideration of these issues in this circumstance,

There being no decision by the Examiner concerning a substantive matter to review at the Board for claims 1–43, 45–50, 57, 58, 60–63, 75, 80, 81, 85, 86, 90–93, 109–111, and 119–136,[30] we will not review this matter any further.

On the other hand, in a somewhat, apparent contradictory position, the Examiner discusses the proposed rejection of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 based on the same combination, Amidi and Dell 184 (Ground 20). RAN 56–57. Requester 2 contends that the Examiner is thus taking

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[29] *See Ex parte Taymac Corp.*, Appeal No. 2011-010682, 2012 WL 1573753 at *8–9 (BPAI April 23, 2012), *cited in* R2 Reb. Br. 7.

[30] The Examiner indicates that claims 1–43, 45–50, 57, 58, 60–63, 75, 80, 81, 85, 86, 90–93, 109–111, and 119–136 were not considered by the Examiner because they were not amended in the Patent Owner's January 14, 2013 response or depend on any such amended claims. March 21, 2014 ACP 9.

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unexplainable, inconsistent positions by discussing some claims but not others. R2 Reb. Br. 6, 8–9. Yet, as Patent Owner indicates, Requester 2 has not addressed the Examiner's full explanation to this apparent inconsistency. PO-R2 Resp. Br. 17. That is, the Examiner explained that parts of Requester 2's comments were not defective and were considered in the interest of special dispatch. March 21, 2014 ACP 9–11. As such, we assume that the Examiner, when discussing Ground 20, found that the discussion of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 was not defective. *See id.* We also determine that this decision to address some of the claims is consistent with *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1356 (Fed. Cir. 2013), *cited in* R2 Reb. Br. 8.

Turning to the merits of the proposed rejection for claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89, the Examiner states that Dell 184 does not overcome the deficiencies of Amidi when addressing the rejection of Amidi under 35 U.S.C. § 102 (Ground 3). RAN 56. Specifically, the Examiner finds that Amidi generates a chip-select signal in response to cs0, cs1, Add(n), CAS, RAS, and WE—not a bank address signal. RAN 56. Additionally, the Examiner finds that Dell 184 does not overcome these deficiencies, teaching a logic circuit receiving address and bank address signals as inputs, and remapping an address and bank address signals. RAN 56–57. Although relying on different expert testimony (i.e., Dr. Bagherzadeh's testimony), Requester 2 proposes to reject these claims for reasons similar to Requester 1 presented concerning the proposed Amidi and Dell 2 rejection. *Compare* R2 App. Br. 12–17 *with* R1 App. Br. 19–25.

The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic

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circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48–3:5, claim 1, ad Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal as recited in rendering claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 obvious.

Accordingly, we reverse the Examiner's non-adopted rejection of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89

3. Requester 3's Appeal

The Examiner did not adopt Requester 3's proposal to reject various claims based on Amidi and at least one other reference under 35 U.S.C. § 103 (Grounds 13, 19, 21, and 22). RAN 14–15. Requester 3 appeals the Examiner's decision not to adopt these proposed rejections. R3 App. Br. 2–3.

a. Micron and Amidi (Ground 13)

Requester 3 asserts that the Examiner erred by not adopting the proposed rejection of claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 as obvious over Micron and Amidi. R3 App. Br. 5–13, 19–22. Specifically, under this ground, the Examiner refers to Grounds 3 through 6 in addressing why these claims under Ground 13 were not adopted. RAN 14, 49, 52 (referring to Grounds 3–6). When addressing Grounds 3 and 4, the Examiner found that Amidi does not disclose generating a CAS or chip-select signal in response to a bank address

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signal. RAN 28–29, *cited in* R3 App. Br. 5; *see also* RAN 26–27. We select claim 1 as illustrative.

Specifically, Requester 3 argues that "obviousness does not require an explicit disclosure" (R3 App. Br. 5) or "'precise teachings . . . for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ'" (*id.* (quoting *KSR*, 550 U.S. at 418)). As discussed above, we agree. Requester 3 further asserts that, given Amidi's disclosure of rank-multiplying memory module, it would have been obvious and even necessary for a logic circuit designer to use a bank address signal in the logic that generates chip-select signals for the memory devices on the memory module. R3 App. Br. 6 (citing 2d Kozyrakis Decl. ¶ 33, 3d Kozyrakis Decl. ¶¶ 15–19, 22–25, and 4th Kozyrakis Decl. ¶¶ 22–23).

In particular, Requester 3 contends that there are two cases when "it is necessary to generate chip-select signals using input bank address signals at column address time." *Id.* The first case occurs "when the incoming row addresses have one more row address bit than the actual memory devices use (Case 1)." *Id.* (citing 2d Kozyrakis Decl. ¶ 33, 3d Kozyrakis Decl. ¶¶ 15–19). The second case occurs "when the input bank addresses have one more bank address bit than the actual memory devices use (Case 2)." *Id.* (citing 3d Kozyrakis Decl. ¶¶ 22–25).

When addressing Amidi above related to Ground 13 and other claims, we determined that Amidi, when accounting for inferences and creative steps that a person of ordinary skill in the art would have employed, at least suggests generating a chip-select signal in response in part to a bank address signal. For example, Requester 3's *second case* of using a spare bank address signal to

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generate the proper chip-select signals for rank multiplication as taught by Amidi
is similar to our previous discussion of the collective teachings suggest a CPLD
receiving a bank address signal. *See* R3 App. Br. 10–11. We refer to our previous
discussion for more details. We thus further agree with Dr. Kozyrakis that such a
chip-select signal may be generated in response to an address signal. 2d Kozyrakis
Decl. ¶ 33; *see also* Kozyrakis Decl. ¶ 26.

Regarding the Requester 3's *first case*, Requester 3 describes Amidi's
teaching of using an extra row address bit to generate a chip-select signal in place
of an address bit. R3 App. Br. 7–8 (discussing Amidi ¶¶ 43–44, 52), 10. As noted
previously, these passages in Amidi do not discuss using a *bank* address bit to
generate the chip-select signals. *See* PO-R3 Resp. Br. 12–13. We thus turn to
what Requester 3 contends an ordinarily skilled artisan would have recognized
regarding bank address signals, as well as other signals, in the context of memory
modules.

Patent Owner reasserts that bank address signals are known to be used in
memory modules in specific ways and JEDEC does not suggest them being used
any other way. PO-R3 Resp. Br. 7–10 (citing JEDEC 79-C 6, 8, 11, Figs. 4, 6).
We agree that bank address signals in JEDEC are used for the discussed
applications. Yet, as stated earlier, Amidi deviates from at least some of the
JEDEC specifications and thus suggest modification from JEDEC designs. *See* R3
Reb. Br. 1 (citing Amidi ¶¶ 10–12).

Also, as previously discussed, Amidi also teaches performing a first row
address and then a column address. Amidi ¶ 61. Amidi also states that the column
address process needs to be provided with its proper control and command signals
in order to read or write to "that" particular cell related to the row address, all

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while achieving rank multiplication. *See id.*; Amidi ¶¶ 10–12. Requester 3 further contends that, during subsequent column address time, a row address bit is not available to generate chip-select signals, and the module must store information from the row address time and match the information to a command (e.g., read). R3 App. Br. 7–8; R3 Reb. Br. 4. Requester 3 asserts some information must be carried from the row address time to the column address time and some control signals must be remapped to select the correct rank. R3 App. Br. 7–8.

> According to Requester 3,

> Input bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals at column address time. *See* Kozyrakis Decl. III, at ¶ 19. It would have been obvious to generate chip-select signals in response to input bank address signals, because the input bank address signals must be used to identify the stored row address bit required to generate the chips-elect signals.

R3 App. Br. 7. Requester asserts "the nature of standard DDR commands motivates a person of ordinary skill in the art to use bank address signals to generate chip-select signals." R3 Reb. Br. 2; *see also* 3d Kozyrakis Decl. ¶ 17, *cited in* R3 App. Br. 8 and R3 Reb. Br. 4; Amidi ¶ 61, *cited in* R3 App. Br. 7 and *quoted in* R3 App. Br. 8.

> We agree with Requester 3 that one skilled in the art would have recognized to use bank address signals for this purpose, because Amidi's rank-multiplied memory module requires more ranks and rank chip-select signals than the standard memory module for selecting the appropriate rank in the module, and some control signals must be used or remapped in order to create the needed, increased chip-select signals. R3 App. Br. 7, 9 (citing 3d Kozyrakis Decl. ¶ 18 (indicating that "[t]he incoming bank address and chip select signals from the memory controller are not sufficient for the rank-multiplying module to identify one of its 16 banks

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for the CAS command.")) We refer to our previous discussion for more details. Dr. Kozyrakis supports this position, stating, in rank-multiplying scenarios, the bank address and chip-select signals are not adequate to identify the increased number banks for a command but do identify the original pair of banks for the original specified memory devices (e.g., 8). 3d Kozyrakis Decl. ¶¶ 18–19, *cited in* R3 App. Br. 9; 4th Kozyrakis Decl. ¶ 22. As discussed in more detail above, Amidi's Figure 6A and B support this testimony.

Moreover, as discussed above, an ordinarily skilled artisan employing their background knowledge would have known that additional signals are needed to generate the expanded number of chip select signals and would turn to extra signals, including bank address signals, in order to multiply the ranks in a memory module, like Amidi's.

Without citing to Amidi or a declaration, Requester 3 even further asserts that the chip-select signals are generated in response to the input bank address signals,

> because the input bank address signals are used to select the previously stored "highest [row] address number Add(n)" needed to generate the chip-select signals matching those generated at RAS time. In other words, the CPLD 604 would generate chip-select signals based on the stored row address bit, which is selected based on the input bank address signals from the memory controller.

R3 App. Br. 10. Requester 3 further states the ability to design and implement this technique is within the skill of ordinary skilled artisans. *Id.* (citing 4th Kozyrakis Decl. ¶¶ 15–25). However, Dr. Kozyrakis's testimony seems to repeat that an address bit is used to generate a chip-select signal or that the bank address and chip-select signals are each used during CAS commands, rather than the recitation

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of a circuit, apart from the memory devices, generates chip-select signals in response to bank address signals as recited. *See* 4th Kozyrakis Decl. ¶¶ 15–25.

Turning, once again, to the second case presented by Requester 3 that occurs when the input bank addresses have one more bank address bit than the actual memory devices use (R3 App. Br. 10–11), Requester 3 cites to other portions of Dr. Kozyrakis' testimony. R3 App. Br. 6, 11 (citing 3d Kozyrakis Decl. ¶¶ 22–25, Kozyrakis Decl. ¶ 26). Requester 3 and Dr. Kozyrakis address the case of a rank-multiplication module from 512 MB devices to 1 GB DDR2 devices found in the '912 disclosure. R3 App. Br. 10–11; 3d Kozyrakis Decl. ¶ 22. Dr. Kozyrakis asserts that there are three input bank address signals (e.g., BA_{0-2}) in this scenario, and they are used to encode the number of the bank to execute a command and to determine the proper rank. 3d Kozyrakis Decl. ¶¶ 22, 25; Kozyrakis Decl. ¶ 26. As discussed, this testimony further illustrates the background knowledge of a person having ordinary skill in the art and, when combined with Amidi's teaching of using free address signals to generate the expanded chip select signals outputted a CPLD, renders claim 1 obvious.

Accordingly, we determine Requester 3 demonstrates Micron and Amidi suggest generating a chip-select signal in response at least in part to a bank address signal as recited in independent claim 1 and independent claims 15, 28, and 39, which recite commensurate limitations.

Requester 3 separately argues independent claim 52. R3 App. Br. 12. The arguments refer back to those discussed for claim 1. We are persuaded for the previously-discussed reasons.

Requester 3 also separately argues independent claims 67, 77, 82, and 87. R3 App. Br. 13. Requester 3 states that the chip-select signals in Amidi are used to

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generate rank-selecting signals. *Id.* (citing Amidi ¶¶ 43–44; Fig. 5). We agree and reverse the non-adoption of the rejection for the same reasons already discussed.

Requester even further separately argues claims 56, 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131. R3 App. Br. 19–22. Requester 3 refers to the arguments presented related to generating chip-select signals in response to input bank address signals. R3 App. Br. 19. Because these claims depend directly or indirectly from independent claims 1, 15, 28, 39, 52, and 57 discussed above and are not separately argued by Patent Owner (*see generally* PO-R3 Resp. Br.), we further determine the Examiner erred in not adopting the rejection of these claims based on Micron and Amidi.

b. *Micron, Amidi, and Olarig (Ground 21)*

This ground of rejection further illustrates known concepts to an ordinary skilled artisan. Requester 3 asserts that the Examiner erred by not adopting the proposed rejection of claims 52–54, 67–71, 77–79, 82–84, and 87–89 as obvious over Micron, Amidi, and Olarig. R3 App. Br. 17–19; R3 Reb. Br. 8–9 (citing 3d Kozyrakis Decl. ¶¶ 16–19). In not adopting the proposed rejection, the Examiner refers to Ground 13 (the rejection of Micron and Amidi) and further states "the citations of Olarig do not teach or suggest the signal response in each of these amended claims." RAN 57. The Examiner determines that the proposed combination with Olarig does not overcome the deficiencies of Micron and Amidi. RAN 57–58. For the above reasons, we disagree and refer above to our discussion of Ground 13 for more details.

Additionally, Requester 3 further relies on Olarig to teach the limitations of the claims on appeal. Requester 3 contends "the combination of Micron, Amidi, and Olarig does render obvious generating chip-select signals in response to an

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input bank address signal." R3 App. Br. 17. Specifically, Requester 3 asserts "Olarig teaches storing information received with a row access command for later use with information from a column address command" and using input bank address signals in remapping control signals. *Id.* (citing Olarig 22:49–54, Fig. 6); R3 Reb. Br. 8–9. Even further, Requester 3 asserts Olarig's Figure 6 and its accompanying description teaches translating input control signals (e.g., bank address signals) for a memory device into output control signals that can be used by another memory device. R3 App. Br. 18–19 (citing Olarig 3:39–42, 22:3–58, Fig. 6); R3 Reb. Br. 9.

Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49–51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.* Granted, there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited. *Id.* But, we agree with Requester 3 that this teaching in Olarig illustrates using bank address signals to generate other control signals was known. *See* R3 App. Br. 18–19.

Additionally, as Requester 3 notes, Olarig is used for a similar purpose to Amidi of remapping input signals into another signal so that when a new memory is introduced into the market a user can substitute the new-type memory module (e.g., a logical memory module) into a pre-existing memory array (e.g., Olarig's memory devices differ from what is expected) of the physical memory module. *See* R3 App. Br. 17–18 (citing Olarig 10:63–11:7, 11:30–40, 22:3–58); *see* Amidi ¶¶ 10–12, 47–49, 52, 55–57, 60, Figs. 6A–6B. Thus, as discussed above, when combined with Amidi's teachings, the collective teachings suggest that an

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ordinarily skilled artisan would have recognized generating a chip-select signal in response at least in part to bank address signals.

Patent Owner contends that Olarig does not disclose a bank address bit being mapped to a chip-select signal. PO-R3 Resp. Br. 23. We agree. But, as discussed above, Olarig teaches combining address signals, including a bank address signal, to generate another control signal, and artisans armed with Olarig's and Amidi's teachings and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as chip-select signals. Also, the proposed rejection does not suggest bodily incorporating Olarig's Figure 6 into Amidi. *See id.* Rather, the rejection proposes combining the teachings to generate the recited chip-select signals in response to a bank address signal as recited in claim 1.

According, we reverse the Examiner's decision not to adopt the proposed rejection of Micron, Amidi, and Olarig.

   4. *Remaining Rejections (Grounds 7, 19, 20, and 22)*

The above discussions address all the claims on appeal and are dispositive, rendering it unnecessary to reach the propriety of any remaining, non-adopted rejections. *See Beloit*, 742 F.2d at 1423, *Gleave*, 560 F.3d at 1338, and 37 C.F.R. 41.77(a).

IV. CONCLUSIONS

We affirm the Examiner's decision to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119.

We affirm the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi

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under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC under § 103, (4) claims 16 and 17 based on Amidi and Dell 2, and (5) claims 58, 60, 68, 79, 84, 89–91, 128–131 under § 112, ¶ 1 as lacking written description support.

We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. § 41.77(b).

We do not reach the propriety of the remaining adopted or proposed rejections.

V. TIME PERIOD FOR RESPONSE

Pursuant to 37 C.F.R. § 41.77(a), the above-noted reversal constitutes a new ground of rejection. Section 41.77(b) provides that "[a] new ground of rejection . . . shall not be considered final for judicial review." That section also provides that Patent Owner, WITHIN ONE MONTH FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of the appeal proceeding as to the rejected claims:

> (1) *Reopen prosecution.* The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

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> (2) *Request rehearing.* The owner may request that the proceeding be
> reheard under § 41.79 by the Board upon the same record. The request
> for rehearing must address any new ground of rejection and state with
> particularity the points believed to have been misapprehended or
> overlooked in entering the new ground of rejection and also state all other
> grounds upon which rehearing is sought.

In accordance with 37 C.F.R. § 41.79(a)(1), the "[p]arties to the appeal may
file a request for rehearing of the decision within one month of the date of: . . .
[t]he original decision of the Board under § 41.77(a)." A request for rehearing
must be in compliance with 37 C.F.R. § 41.79(b). Comments in opposition to the
request and additional requests for rehearing must be in accordance with 37 C.F.R.
§ 41.79(c)–(d), respectively. Under 37 C.F.R. § 41.79(e), "[t]he times for
requesting rehearing under paragraph (a) of this section, for requesting further
rehearing under paragraph (c) of this section, and for submitting comments under
paragraph (b) of this section may not be extended."

An appeal to the United States Court of Appeals for the Federal Circuit
under 35 U.S.C. §§ 141–144 and 315 and 37 C.F.R. § 1.983 for an *inter partes*
reexamination proceeding "commenced" on or after November 2, 2002 may not be
taken "until all parties' rights to request rehearing have been exhausted, at which
time the decision of the Board is final and appealable by any party to the appeal to
the Board." 37 C.F.R. § 41.81; *see also* MPEP §§ 2682, 2683 (8th ed., Rev. 8, July
2010).

No time period for taking any subsequent action in connection with this
appeal may be extended under 37 C.F.R. § 1.136(a).

Requests for extensions of time in this *inter partes* reexamination
proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

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In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

<u>AFFIRMED-IN-PART</u>
<u>37 C.F.R. § 41.77(b)</u>

cda

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PEIKARI, BEHZAD

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION

Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.

Requester 2, and

GOOGLE INC.
Requester 3
v.

NETLIST, INC.,
Patent Owner

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Technology Center 3900

JEFFREY B. ROBERTSON, *Administrative Patent Judge*.

DECISION ON PETITION

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This is a decision granting Patent Owner's "REQUEST FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.956," filed June 16, 2016 ("petition"). The petition requests that the Office extend the time period for filing a request to reopen prosecution by one month. The petition fee of $200 in accordance with 37 C.F.R. § 1.17(g) was charged to Patent Owner's deposit account on June 17, 2016.

FINDINGS

1.   On May 31, 2016, the Patent Trial and Appeal Board ("Board") entered a Decision on appeal in this merged *inter partes* reexamination proceeding, including new grounds of rejection. Decision 70–102.

2.   The Decision on appeal, citing 37 C.F.R. § 41.77(b), notes that appellant has one month from the date of the Decision to file a response requesting reopening of prosecution before the Examiner. *Id.* at 102.

3.   On June 16, 2016, the petition requesting an extension of time was filed.

DISCUSSION

In its petition, Patent Owner requests an extension of time to submit a request to reopen prosecution in response to the Board's Decision on appeal mailed May 31, 2016, in order to have a fair opportunity to prepare a full response for reopening prosecution. Petition 1. Patent Owner states that

> Since receipt of the Decision, the Patent Owner and its
> undersigned attorney have been working diligently on preparing
> such a response. The attorney and his colleague have reviewed
> U.S. Patent No. 7,619,912, the Decision, and references cited

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for the new grounds of rejection raised by the Decision. The
Patent Owner, the attorney and his colleague have discussed the
Decision and have begun preparing a response.

Id. at 2.

Patent Owner indicates that

The Decision reversed the Examiner on at least three new grounds of
rejection. The Decision, itself, is over 100 pages long and cites to 13
expert declarations. Adequately analyzing all the issues raised by
these new grounds of rejection requires a substantial amount of time
and preparation.

Id.

It is stated that

The Patent Owner is accordingly considering a declaration under
§ 1.132, i.e., an expert declaration presenting evidence directed to
clarifying such technical issues and to establishing the ordinary skilled
artisan's understanding of those technical issues. Sufficient time is
needed to determine and present any such evidence.

Id., at 2-3.

Patent Owner asserts that

Third, the present reexamination of the '912 Patent is co-
pending with reexaminations of patents related to the '912 Patent. One
of the related patents is U.S. Patent No. 7,864,627, which is in *inter
partes* reexamination bearing control no. 95/001,758. In the '627
Patent reexamination, the Patent Owner and the undersigned attorney
are currently preparing a response to another outstanding Decision on
Appeal. That response is also due on June 30, 2016. Thus, the
response in the '627 Patent reexamination and the response in this
present '912 Patent reexamination have overlapping periods for
response with proximate deadlines.

Id. at 3.

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Fourth, there is a discrepancy due to multiple mailing dates for the present Decision on Appeal. For the '1,339 and '578 proceedings, the Decision on Appeal was mailed on May 31, 2016. For the '579 proceeding, however, the Decision on Appeal was mailed later on June 6, 2016.
    Id.

Fifth, there is a pending Petition for Confirmation of Rejection in Decision on Appeal by Third Party Requester Under 37 C.F.R. § 41.3 dated June 13, 2016 by SMART Modular Technologies (WWH) Inc. ("Requester 2"). This Petition appears to request clarification on whether Ground 20 based on Amidi and Dell 184 is to be included as a fourth new ground of rejection, in addition to the three new grounds of rejection in the Board's listing. (Decision on Appeal at 102.)
    Id.

RELEVANT AUTHORITY

35 U.S.C. § 314(c) (pre-AIA) provides:

> SPECIAL DISPATCH.— Unless otherwise provided by the Director for good cause, all inter partes reexamination proceedings under this section, including any appeal to the Board of Patent Appeals and Interferences,[1] shall be conducted with special dispatch within the Office.

37 C.F.R. § 41.77 provides:

> (a) The Patent Trial and Appeal Board, in its decision, may affirm or reverse each decision of the examiner on all issues raised on each appealed claim, or remand the reexamination proceeding to the examiner for further consideration. The reversal of the examiner's determination not to make a rejection proposed by the third party requester constitutes a decision adverse to the patentability of the claims which are subject to that proposed rejection which will be set forth in the decision of the Patent Trial and Appeal Board as a new ground of rejection under paragraph (b) of this section. The affirmance of the rejection of a claim on any of the grounds

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[1] Now known as the Patent Trial and Appeal Board.

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specified constitutes a general affirmance of the decision of the examiner on that claim, except as to any ground specifically reversed.

(b) Should the Board reverse the examiner's determination not to make a rejection proposed by a requester, the Board shall set forth in the opinion in support of its decision a new ground of rejection; or should the Board have knowledge of any grounds not raised in the appeal for rejecting any pending claim, it may include in its opinion a statement to that effect with its reasons for so holding, which statement shall constitute a new ground of rejection of the claim. Any decision which includes a new ground of rejection pursuant to this paragraph shall not be considered final for judicial review. When the Board makes a new ground of rejection, the owner, within one month from the date of the decision, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal proceeding as to the rejected claim:

(1) Reopen prosecution. The owner may file a response requesting reopening of prosecution before the examiner. Such a response must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both.

(2) Request rehearing. The owner may request that the proceeding be reheard under § 41.79 by the Board upon the same record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

(c) Where the owner has filed a response requesting reopening of prosecution under paragraph (b)(1) of this section, any requester, within one month of the date of service of the owner's response, may once file comments on the response.

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Such written comments must be limited to the issues raised by the Board's opinion reflecting its decision and the owner's response. Any requester that had not previously filed an appeal or cross appeal and is seeking under this subsection to file comments or a reply to the comments is subject to the appeal and brief fees under § 41.20(b)(1) and (2), respectively, which must accompany the comments or reply.

(d) Following any response by the owner under paragraph (b)(1) of this section and any written comments from a requester under paragraph (c) of this section, the proceeding will be remanded to the examiner. The statement of the Board shall be binding upon the examiner unless an amendment or new evidence not previously of record is made which, in the opinion of the examiner, overcomes the new ground of rejection stated in the decision. The examiner will consider any owner response under paragraph (b)(1) of this section and any written comments by a requester under paragraph (c) of this section and issue a determination that the rejection is maintained or has been overcome.

(e) Within one month of the examiner's determination pursuant to paragraph (d) of this section, the owner or any requester may once submit comments in response to the examiner's determination. Within one month of the date of service of comments in response to the examiner's determination, the owner and any requesters may file a reply to the comments. No requester reply may address the comments of any other requester reply. Any requester that had not previously filed an appeal or cross appeal and is seeking under this subsection to file comments or a reply to the comments is subject to the appeal and brief fees under § 41.20(b)(1) and (2), respectively, which must accompany the comments or reply.

(f) After submission of any comments and any reply pursuant to paragraph (e) of this section, or after time has expired, the proceeding will be returned to the Board which shall reconsider the matter and issue a new decision. The new

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decision is deemed to incorporate the earlier decision, except for those portions specifically withdrawn.

(g) The time period set forth in paragraph (b) of this section is subject to the extension of time provisions of § 1.956 of this title when the owner is responding under paragraph (b)(1) of this section. The time period set forth in paragraph (b) of this section may not be extended when the owner is responding under paragraph (b)(2) of this section. The time periods set forth in paragraphs (c) and (e) of this section may not be extended.

37 C.F.R. § 1.956 provides:

The time for taking any action by a patent owner in an inter partes reexamination proceeding will be extended only for sufficient cause and for a reasonable time specified. Any request for such extension must be filed on or before the day on which action by the patent owner is due, but in no case will the mere filing of a request effect any extension. Any request for such extension must be accompanied by the petition fee set forth in § 1.17(g). See § 1.304(a) for extensions of time for filing a notice of appeal to the U.S. Court of Appeals for the Federal Circuit.

MPEP § 2665 provides in pertinent part:

Any request for an extension of time in a reexamination proceeding must fully state the reasons therefor. The reasons must include (A) a statement of what action the patent owner has taken to provide a response, to date as of the date the request for extension is submitted, and (B) why, in spite of the action taken thus far, the requested additional time is needed. The statement of (A) must provide a factual accounting of reasonably diligent behavior by all those responsible for preparing a response to the outstanding Office action within the statutory time period.

Prosecution will be conducted by initially setting a time period of at least 30 days or one month (whichever is longer),

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see MPEP § 2662. First requests for extensions of these time periods will be granted for sufficient cause, and for a reasonable time specified-usually one month. The reasons stated in the request will be evaluated, and the request will be favorably considered where there is a factual accounting of reasonably diligent behavior by all those responsible for preparing a response or comments within the statutory time period. Second or subsequent requests for extensions of time, or requests for more than one month, will be granted only in extraordinary situations.

ANALYSIS

Patent Owner's request for an extension of time has been considered fully. The Decision on appeal includes three new grounds of rejection for claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21) under 37 C.F.R. § 41.77(b). Decision 70–102.

In accordance with 37 C.F.R. § 41.77(g), the time period set forth in paragraph (b) of this section is subject to the extension of time provisions of § 1.956 of this title when the Patent Owner is responding under paragraph (b)(1) of this section. First requests for extensions of these time periods will be granted for sufficient cause, and for a reasonable time specified, i.e., usually one month. The reasons stated in the request will be evaluated, and the request will be favorably considered where there is a factual accounting of reasonably diligent behavior by all those responsible for preparing a response or comments within the statutory time period. Second or subsequent requests for extensions of time, or requests for more than one month, will be granted only in extraordinary situations.

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The petition includes a statement of (A) what action the Patent Owner has taken to provide a response to date, as of the date the request for extension is submitted, and (B) why, in spite of the action taken thus far, the requested additional time is needed. The statement provides a factual accounting of reasonably diligent behavior by all those responsible for preparing a response requesting reopening of prosecution within the statutory time period.

Patent Owner establishes that sufficient cause exists for extending the due date by one month for Patent Owner to request reopening of prosecution in response to the new grounds of rejection. Pursuant to 35 U.S.C. § 314(c) (pre-AIA), all *inter partes* reexamination proceedings under this section, including any appeal to the Patent Trial and Appeal Board, shall be conducted with special dispatch within the Office.

Accordingly, the present petition is **granted** for a one month extension of time.

DECISION

In view of the foregoing, the present petition is GRANTED for a one month extension of time.

The request to reopen prosecution pursuant to 37 C.F.R. § 41.77(b)(1) is due July 31, 2016.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.,
Requester 3
v.

NETLIST, INC.,
Patent Owner

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579[1]
Patent 7,619,912 B2
Technology Center 3900

JEFFREY B. ROBERTSON, *Administrative Patent Judge.*

DECISION ON PETITION

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[1] It is noted that the Decision of May 31, 2016, inadvertently included a typographical error for Control No. 95/000,579 on page 1 and in the header, however, the Decision on page 2, paragraph 1 sets forth the correct Control No.

Appeal 2015-006849
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This is a Decision granting Requester 2's "PETITION FOR CONFIRMATION OF REJECTION IN DECISION ON APPEAL BY THIRD PARTY REQUESTER UNDER 37 C.F.R. § 41.3," filed on June 13, 2016 (petition). In its petition, Requester 2 requests "review and confirmation of the rejection of claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 under 35 U.S.C. § 103 based on Amidi and Dell 184 (Ground 20), as provided in the Decision on Appeal mailed May 31, 2016." Petition 1. The petition fee of $1,940, in accordance with 37 C.F.R. § 1.20(c)(6) was charged to Requester 2's deposit account on June 24, 2016.

FINDINGS

1.   On May 31, 2016, the Patent Trial and Appeal Board ("Board") entered a Decision on appeal in this merged *inter partes* reexamination proceeding, including new grounds of rejection. Decision 70–102.

2.   The Decision on appeal, citing 37 C.F.R. § 41.77(b), notes that appellant has one month from the date of the Decision to file a response requesting reopening of prosecution before the Examiner. *Id.* at 102.

3.   On June 13, 2016, the petition was filed.

DISCUSSION

In the petition, Requester 2 requests review and confirmation of the rejection of claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 under 35 U.S.C. § 103 based on Amidi and Dell 184 (Ground 20), as provided in the Decision on Appeal mailed May 31, 2016. Petition 1.

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RELEVANT AUTHORITY

37 C.F.R. § 1.181 provides:

(a) Petition may be taken to the Director:

(1) From any action or requirement of any examiner in the ex parte prosecution of an application, or in ex parte or inter partes prosecution of a reexamination proceeding which is not subject to appeal to the Patent Trial and Appeal Board or to the court;

(2) In cases in which a statute or the rules specify that the matter is to be determined directly by or reviewed by the Director; and

(3) To invoke the supervisory authority of the Director in appropriate circumstances. For petitions involving action of the Patent Trial and Appeal Board, see § 41.3 of this title.

(b) Any such petition must contain a statement of the facts involved and the point or points to be reviewed and the action requested. Briefs or memoranda, if any, in support thereof should accompany or be embodied in the petition; and where facts are to be proven, the proof in the form of affidavits or declarations (and exhibits, if any) must accompany the petition.

(c) When a petition is taken from an action or requirement of an examiner in the ex parte prosecution of an application, or in the ex parte or inter partes prosecution of a reexamination proceeding, it may be required that there have been a proper request for reconsideration (§ 1.111) and a repeated action by the examiner. The examiner may be directed by the Director to furnish a written statement, within a specified time, setting forth the reasons for his or her decision upon the matters averred in the petition, supplying a copy to the petitioner.

(d) Where a fee is required for a petition to the Director the appropriate section of this part will so indicate. If any required

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> fee does not accompany the petition, the petition will be dismissed.
>
> (e) Oral hearing will not be granted except when considered necessary by the Director.
>
> (f) The mere filing of a petition will not stay any period for reply that may be running against the application, nor act as a stay of other proceedings. Any petition under this part not filed within two months of the mailing date of the action or notice from which relief is requested may be dismissed as untimely, except as otherwise provided. This two-month period is not extendable.
>
> (g) The Director may delegate to appropriate Patent and Trademark Office officials the determination of petitions.

37 C.F.R. § 41.3 provides:

> (a) *Deciding official.* Petitions must be addressed to the Chief Administrative Patent Judge. A panel or an administrative patent judge may certify a question of policy to the Chief Administrative Patent Judge for decision. The Chief Administrative Patent Judge may delegate authority to decide petitions.
>
> (b) *Scope.* This section covers petitions on matters pending before the Board (§§ 41.35, 41.64, 41.103, and 41.205); otherwise, see §§ 1.181 to 1.183 of this title. The following matters are not subject to petition:
>
> > (1) Issues committed by statute to a panel, and
> >
> > (2) In pending contested cases, procedural issues. See § 41.121(a)(3) and § 41.125(c).
>
> (c) *Petition fee.* The fee set in § 41.20(a) must accompany any petition under this section except no fee is required for a petition under this section seeking supervisory review.

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(d) *Effect on proceeding.* The filing of a petition does not stay
the time for any other action in a Board proceeding.

(e) *Time for action.*

(1) Except as otherwise provided in this part or as the
Board may authorize in writing, a party may:

(i) File the petition within 14 days from the date of
the action from which the party is requesting relief,
and

(ii) File any request for reconsideration of a
petition decision within 14 days of the decision on
petition or such other time as the Board may set.

(2) A party may not file an opposition or a reply to a
petition without Board authorization.

37 C.F.R. § 41.77 provides in pertinent part:

(b) Should the Board reverse the examiner's determination not
to make a rejection proposed by a requester, the Board shall set
forth in the opinion in support of its decision a new ground of
rejection; or should the Board have knowledge of any grounds
not raised in the appeal for rejecting any pending claim, it may
include in its opinion a statement to that effect with its reasons
for so holding, which statement shall constitute a new ground of
rejection of the claim. Any decision which includes a new
ground of rejection pursuant to this paragraph shall not be
considered final for judicial review. When the Board makes a
new ground of rejection, the owner, within one month from the
date of the decision, must exercise one of the following two
options with respect to the new ground of rejection to avoid
termination of the appeal proceeding as to the rejected claim:

(1) Reopen prosecution. The owner may file a response
requesting reopening of prosecution before the examiner.
Such a response must be either an amendment of the

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claims so rejected or new evidence relating to the claims
so rejected, or both.

(2) Request rehearing. The owner may request that the
proceeding be reheard under § 41.79 by the Board upon
the same record. The request for rehearing must address
any new ground of rejection and state with particularity
the points believed to have been misapprehended or
overlooked in entering the new ground of rejection and
also state all other grounds upon which rehearing is
sought.

(c) Where the owner has filed a response requesting reopening
of prosecution under paragraph (b)(1) of this section, any
requester, within one month of the date of service of the
owner's response, may once file comments on the response.
Such written comments must be limited to the issues raised by
the Board's opinion reflecting its decision and the owner's
response. Any requester that had not previously filed an appeal
or cross appeal and is seeking under this subsection to file
comments or a reply to the comments is subject to the appeal
and brief fees under § 41.20(b)(1) and (2), respectively, which
must accompany the comments or reply.

(d) Following any response by the owner under paragraph
(b)(1) of this section and any written comments from a
requester under paragraph (c) of this section, the proceeding
will be remanded to the examiner. The statement of the Board
shall be binding upon the examiner unless an amendment or
new evidence not previously of record is made which, in the
opinion of the examiner, overcomes the new ground of rejection
stated in the decision. The examiner will consider any owner
response under paragraph (b)(1) of this section and any written
comments by a requester under paragraph (c) of this section and
issue a determination that the rejection is maintained or has
been overcome.

(e) Within one month of the examiner's determination pursuant
to paragraph (d) of this section, the owner or any requester may

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once submit comments in response to the examiner's determination. Within one month of the date of service of comments in response to the examiner's determination, the owner and any requesters may file a reply to the comments. No requester reply may address the comments of any other requester reply. Any requester that had not previously filed an appeal or cross appeal and is seeking under this subsection to file comments or a reply to the comments is subject to the appeal and brief fees under § 41.20(b)(1) and (2), respectively, which must accompany the comments or reply.

(f) After submission of any comments and any reply pursuant to paragraph (e) of this section, or after time has expired, the proceeding will be returned to the Board which shall reconsider the matter and issue a new decision. The new decision is deemed to incorporate the earlier decision, except for those portions specifically withdrawn.

(g) The time period set forth in paragraph (b) of this section is subject to the extension of time provisions of § 1.956 of this title when the owner is responding under paragraph (b)(1) of this section. The time period set forth in paragraph (b) of this section may not be extended when the owner is responding under paragraph (b)(2) of this section. The time periods set forth in paragraphs (c) and (e) of this section may not be extended.

ANALYSIS

Requester 2's petition has been considered. In the petition, Requester 2 points out that

the Decision on Appeal, pages 90-93 pertain Requester 2's appeal and specific consideration of Ground 20 and a proposed rejection based on U.S. Patent Publication No. 2006/0117152 ("Amidi") and U.S. Patent No. 6,446,184 ("Dell 184") under 35 U.S.C. § 103.

Petition 1.

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Requester 2 states that

On pages 91-93, the Board discusses the Examiner's position and his
conclusion regarding the proposed rejection of claims 52-54, 56, 67-71, 77-
79, 82-84, and 87-89 based on the same combination, Amidi and Dell 184
(Ground 20). In particular, the Board notes:

On the other hand, in a somewhat, apparent contradictory position, the
Examiner discusses the proposed rejection of claims 52-54, 56, 67-71, 77-
79, 82-84, and 87- 89 based on the same combination, Amidi and Dell 184
(Ground 20). RAN 56-57.

Decision on Appeal, p. 91-92.
Id., at 2.

Requester 2 indicates that the Board further notes that:

Requester 2 proposes to reject these claims for reasons similar to
[those] Requester 1 presented concerning the proposed Amidi and Dell 2
["Dell 2" refers to U.S. Patent No. 6,209,074] rejection. Compare R2 App.
Br. 12-17 with R1 App. Br. 19-25. Decision on Appeal, p. 92.
Id.

Requester 2 states that

On pages 92-93, the Board analyzes Ground 20 and concludes:

The teachings in Dell 184 are similar to Dell 2 previously discussed.
That is, both references teach and suggest using various types of memory
devices or densities, where the memory device is configured with M banks,
but the logic circuit receives address and bank address inputs corresponding
to N bank memory devices. Compare Dell 184, Abstract, 2:48-3:5, claim 1,
ad Fig. 1 with Dell 2, Abstract, 2:40-65, claim 1, and Fig 1. Moreover, using
the same findings and reasoning as discussed above, combining Dell 184's
teaching with Amidi would have predictably yielded Amidi's CPLD
receiving various inputs, including bank address signals, to achieve both the
desired rank and bank expansion. Such a combination would also
predictably result in a logic element generating a first number of chip-select
or rank-selecting signals in response to a bank address signal as recited in
rendering claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 obvious.

Accordingly, we reverse the Examiner's non-adopted rejection of
claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89[.]

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> Decision on Appeal, pp. 92-93 (emphasis added)
> *Id.*, at 2-3.

Requester 2 points out that in contrast, in the Conclusions on page 102, the Board states:

> We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93. 109-111, and 120-136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. §41.77(b).
> Decision on Appeal, p. 102.
> *Id.*, at 3.

Requester 2 asserts that

> As the Conclusions on page 102 of the Decision on Appeal did not clearly include the reversal of the Examiner's non-adopted rejection of claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 as obvious over Amidi and Dell 184 (Ground 20) (Decision on Appeal, p. 93), Third Party Requester SMART Modular Technologies, Inc. respectfully petitions that the rejection of claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 under 35 U.S.C. § 103 based on Amidi and Dell 184 (Ground 20) be confirmed.

Id.

It is true that Requester 2's proposed rejection of Amidi and Dell 184 under 35 U.S.C. § 103 (Ground 20) is discussed on pages 90-93 of the Decision, and that the Decision states on page 93, that "we reverse the Examiner's non-adopted rejection of claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89." It is clarified that Requester 2's proposed rejection of Amidi and Dell 184 under 35 U.S.C. § 103 (Ground 20) was intended to be included as a new grounds of rejection under § 41.77(b). Therefore, page 102 of the Decision is revised to state that

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We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, (3) Amidi and Dell 148, or (4) Micron, Amidi, and Olarig (Grounds 5, 13, 20, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. § 41.77(b).

Accordingly, the petition is **granted.**

DECISION

For the foregoing reasons, the petition is GRANTED.

Patent Owner's request to reopen prosecution pursuant to 37 C.F.R. § 41.77(b)(1) is due July 31, 2016, in accordance with the decision granting an extension of time, mailed concurrently herewith, and must be responsive to the four new grounds of rejection.

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I.   REHEARING ARGUMENT

A.   Introduction

This is a request for rehearing under 37 C.F.R. § 41.79(a)(l). The Patent Trial and Appeal Board (the "Board") issued the Decision On Appeal on May 31, 2016 (the "Decision"). In the Decision, the Board affirmed the Examiner's rejection of claims 2, 5, 7, 9, 21 ,23, 26, 30, 33, 57 and 119, and issued new grounds of rejection for claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111 and 120-136, pursuant to 37 C.F.R. § 41.77(a), (b). Decision, 101, 102. As a result of this Decision, claims 16-17 addressed in this Request stand.

Claim 16 was originally dependent on independent claim 15, and was rewritten in independent form from claim 15 by Patent Owner after claim 15 was rejected under Grounds 6, 9, 11, 12, 13 and 18. Office Action of October 14, 2011, 4-7; Patent Owner Response of January 14, 2012, 8-9.

Still further, amended independent claim 15 currently stands rejected under Ground 5 (Amidi and Dell 2). Decision, 102. While amended independent claim 15 contains limitations in addition to those in the originally issued claim 15, it is apparent that the originally issued claim 15 is also invalid on these same grounds, as it contains all of the limitations of the amended independent claim 15.

Independent claim 16 differs from original claim 15 only in requiring that the command signal is transmitted to only one DDR memory device at a time. As such, currently pending claim 16 is allowable only for the portions of the claim below that are not underlined, with the underlined portions of the claim being found unpatentable by the Decision.

(Amended) [The memory module of claim 15]. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a

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4849-0723-2308.v1

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<table>
<tr><td>I hereby certify that this paper is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: July 31, 2016   Signature: /Erwin B. Palines/ (Erwin B. Palines)</td></tr>
</table>

<div align="right">
VIA EFS

Docket No.: 635162800300

(PATENT)
</div>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of: Jayesh BHAKTA et al.	Examiner: Behzad PEIKARI
Control Nos.: 95/001,339; 95/000,578; 95/000,579	Art Unit: 3992
Filed: June 8, 2010; October 20, 2010; October 21, 2010	Conf. No.: 5035; 8810; 3547

For: MEMORY MODULE DECODER

<div align="center">

PATENT OWNER'S RESPONSE
REQUESTING TO REOPEN PROSECUTION
PURSUANT TO 37 C.F.R. § 41.77(b)(1)
</div>

MS *Inter Partes* Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the Patent Trial and Appeal Board's Decision dated May 31, 2016 (the "Decision"), for which a response requesting to reopen prosecution pursuant to 37 C.F.R. § 41.77(b)(1) was due June 30, 2016, and for which a one-month request for extension of time was requested and granted to July 31, 2016, the Patent Owner respectfully submits this Response. Please consider the following:

There are no amendments to the specification or drawings.

Claim amendments begin on page 2 of this paper.

Status of all claims is provided at page 46.

Remarks/Arguments begin on page 47, and a certificate of service is provided at page 58.

la-1322110

<div align="right">
Samsung Electronics Co., Ltd.

Ex. 1010, p. 7269
</div>

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Docket No. 635162800300

CLAIM AMENDMENTS

Please **cancel** claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128-130.

Please **enter** the following amendments.

1.   (Twice amended)   A memory module connectable to a computer system, the
memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board,
the plurality of DDR memory devices having a first number of DDR memory devices arranged in a
first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a
register, the logic element receiving a set of input control signals from the computer system, the set
of input control signals comprising at least one row/column address signal, bank address signals,
and at least one chip-select signal, the set of input control signals corresponding to a second number
of DDR memory devices arranged in a second number of ranks, the second number of DDR
memory devices smaller than the first number of DDR memory devices and the second number of
ranks less than the first number of ranks, the circuit generating a set of output control signals in
response to the set of input control signals, the set of output control signals corresponding to the
first number of DDR memory devices arranged in the first number of ranks, wherein the circuit
further responds to a first command signal and the set of input control signals from the computer
system by generating and transmitting a second command signal and the set of output control
signals to the plurality of memory devices, the first command signal and the set of input control

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signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

2.   (Amended)   [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

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wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

3.   (Original)   The memory module of claim 1, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

4.   (Original)   The memory module of claim 3, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

5.   (Amended)   [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of

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ranks less than the first number of ranks, the circuit generating a set of output control signals in

response to the set of input control signals, the set of output control signals corresponding to the

first number of DDR memory devices arranged in the first number of ranks, wherein the circuit

further responds to a first command signal and the set of input control signals from the computer

system by generating and transmitting a second command signal and the set of output control

signals to the plurality of memory devices, the first command signal and the set of input control

signals corresponding to the second number of ranks and the second command signal and the set of

output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit receives and buffers a plurality of row/column address signals of the

input control signals during a row access procedure and sends the buffered plurality of row/column

address signals to the plurality of DDR memory devices during a subsequent column access

procedure.

6.   (Original)   The memory module of claim 1, wherein the logic element comprises

an application-specific integrated circuit, a field-programmable gate array, a custom-designed

semiconductor device, or a complex programmable-logic device.

7.   (Amended)   [The memory module of claim 1] A memory module connectable to a

computer system, the memory module comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

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8.   (Original)   The memory module of claim 1, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

9.   (Amended)   [The memory module of claim 1] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control

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signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the register comprises a plurality of register devices.

10.   (Original)   The memory module of claim 1, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

11.   (Original)   The memory module of claim 10, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

12.   (Original)   The memory module of claim 1, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

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13.   (Original)   The memory module of claim 12, wherein the first rank is spaced

from the second rank and the third rank is spaced from the fourth rank.

14.   (Original)   The memory module of claim 1, wherein the set of input control

signals corresponds to a first memory density, and the set of output control signals corresponds to a

second memory density, the second memory density greater than the first memory density.

15.   (Twice amended)   A memory module connectable to a computer system, the

memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,

the plurality of DDR memory devices having a first number of DDR memory devices arranged in a

first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a

register, the logic element receiving a set of input signals from the computer system, the set of input

signals comprising at least one row/column address signal, bank address signals, and at least one

chip-select signal, the set of input signals configured to control a second number of DDR memory

devices arranged in a second number of ranks, the second number of DDR memory devices smaller

than the first number of DDR memory devices and the second number of ranks less than the first

number of ranks, the circuit generating a set of output signals in response to the set of input signals,

the set of output signals configured to control the first number of DDR memory devices arranged in

the first number of ranks, wherein the circuit further responds to a command signal and the set of

input signals from the computer system by selecting one or two ranks of the first number of ranks

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and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals and (iii) the at least one chip-select signal of the set of input signals and (iv) the PLL clock signal.

16.   (Amended)   [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

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a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the command signal is transmitted to only one DDR memory device at a time.

17.   (Original)   The memory module of claim 16, wherein the command signal comprises a read command signal.

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18.   (Original)   The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

19.   (Original)   The memory module of claim 18, wherein the command signal comprises a refresh command signal.

20.   (Original)   The memory module of claim 18, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

21.   (Amended)   [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of

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input signals from the computer system by selecting one or two ranks of the first number of ranks

and transmitting the command signal to at least one DDR memory device of the selected one or two

ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a

row access procedure for subsequent use during a column access procedure.

22.   (Original)   The memory module of claim 15, wherein the command signal

comprises a read command signal or a write command signal, the set of input signals comprises a

density bit which is a row address bit, and the circuit is configured to store the row address bit

during an activate command for a selected bank.

23.   (Amended)   [The memory module of claim 15] A memory module connectable to

a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,

the plurality of DDR memory devices having a first number of DDR memory devices arranged in a

first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a

register, the logic element receiving a set of input signals from the computer system, the set of input

signals comprising at least one row/column address signal, bank address signals, and at least one

chip-select signal, the set of input signals configured to control a second number of DDR memory

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devices arranged in a second number of ranks, the second number of DDR memory devices smaller

than the first number of DDR memory devices and the second number of ranks less than the first

number of ranks, the circuit generating a set of output signals in response to the set of input signals,

the set of output signals configured to control the first number of DDR memory devices arranged in

the first number of ranks, wherein the circuit further responds to a command signal and the set of

input signals from the computer system by selecting one or two ranks of the first number of ranks

and transmitting the command signal to at least one DDR memory device of the selected one or two

ranks of the first number of ranks; and

      a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the circuit is configured to store an input signal of the set of input signals during a

row access procedure and to transmit the stored input signal as an output signal of the set of output

signals during a subsequent column access procedure.

24.   (Original)   The memory module of claim 15, wherein the logic element

comprises an application-specific integrated circuit, a field-programmable gate array, a custom-

designed semiconductor device, or a complex programmable-logic device.

25.   (Cancelled)

26.   (Amended)   [The memory module of claim 25] A memory module connectable to

a computer system, the memory module comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices, and

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wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

27.   (Original)   The memory module of claim 15, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

28.   (Twice amended)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set

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of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal.

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29.   (Original)   The memory module of claim 28, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

30.   (Amended)   [The memory module of claim 29] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number

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of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the

selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the logic element comprises an application-specific integrated circuit, a field-

programmable gate array, a custom-designed semiconductor device, or a complex programmable-

logic device, and

wherein the circuit is configured to store an input control signal of the set of input control

signals during a row access procedure and to transmit the stored input control signal as an output

control signal of the set of output control signals during a column access procedure.

31.   (Original)   The memory module of claim 28, wherein the set of input control

signals comprises fewer chip-select signals than does the set of output control signals.

32.   (Original)   The memory module of claim 31, wherein the set of input control

signals comprises two chip-select signals and the set of output control signals comprises four chip-

select signals.

33.   (Amended)   [The memory module of claim 28] A memory module connectable to

a computer system, the memory module comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein the register receives the bank address signals and the input command signal of the set of input control signals.

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34.   (Original)   The memory module of claim 28, wherein the first number of ranks is four and the second number of ranks is two.

35.   (Original)   The memory module of claim 28, wherein the first number of ranks is two and the second number of ranks is one.

36.   (Original)   The memory module of claim 28, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

37.   (Original)   The memory module of claim 28, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

38.   (Original)   The memory module of claim 28, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

39.   (Twice amended)   A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer

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system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives <u>at least one row address signal,</u> the bank address signals, <u>at least one chip-select signal,</u> and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

<u>wherein, in response to signals received from the computer system, the phase-lock loop</u> <u>(PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic</u> <u>element, and the register,</u>

<u>wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers,</u> <u>in response to the PLL clock signal, the bank address signals and a plurality of the row address</u> <u>signals, and (iii) transmits the buffered bank address signals and the buffered row address signals to</u> <u>the at least one DDR memory device of the selected at least one rank, and wherein the plurality of</u> <u>the row address signals received by the register are separate from the at least one row address signal</u> <u>received by the logic element, and</u>

<u>wherein the logic element generates gated column access strobe (CAS) signals or chip-select</u> <u>signals of the output signals in response at least in part to (i) the at least one row address signal, (ii)</u>

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the bank address signals, and (iii) the at least one chip-select signal of the plurality of input signals
and (iv) the PLL clock signal.

 40. (Original) The memory module of claim 39, wherein the plurality of output
signals corresponds to a first number of DDR memory devices arranged in the two or more ranks
which are selectable by the first number of chip-select signals and wherein the plurality of input
signals corresponds to a second number of DDR memory devices arranged in ranks which are
selectable by the second number of chip-select signals, wherein the memory module simulates a
virtual memory module having the second number of DDR memory devices.

 41. (Original) The memory module of claim 39, wherein the at least one integrated
circuit element comprises one or more integrated circuit elements selected from the group consisting
of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed
semiconductor device, and a complex programmable-logic device.

 42. (Cancelled)

 43. (Amended) The memory module of claim [42] 39, wherein the logic element
receives the second number of chip-select signals.

 44. (Cancelled)

 45. (Original) The memory module of claim 39, wherein two or more of the logic
element, the register, and the phase-lock loop device are portions of a single component.

 46. (Original) The memory module of claim 39, wherein the plurality of DDR
memory devices is arranged as the first rank of DDR memory devices on the first side of the printed
circuit board, the second rank of DDR memory devices on the first side of the printed circuit board,

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a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth

rank of DDR memory devices on the second side of the printed circuit board, the DDR memory

devices of the fourth rank spaced from the DDR memory devices of the third rank.

47.   (Original)   The memory module of claim 39, wherein the DDR memory devices

of the second rank are spaced from the DDR memory devices of the first rank in a direction along

the first side.

48.   (Original)   The memory module of claim 39, wherein the plurality of DDR

memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the

second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of

the printed circuit board.

49.   (Original)   The memory module of claim 39, wherein the plurality of input

signals corresponds to a first memory density, and the plurality of output signals corresponds to a

second memory density, the second memory density greater than the first memory density.

50.   (Original)   The memory module of claim 39, wherein the at least one integrated

circuit element is configured to respond to the plurality of input signals by selecting at least one

rank of the two or more ranks and transmitting a command signal to at least one DDR memory

device of the selected at least one rank.

51.   (Cancelled)

52.   (New) A memory module connectable to a computer system, the memory module

comprising:

a printed circuit board;

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a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

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wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and

wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

53.   (Cancelled)

54.   (New) The memory module of claim 52, wherein the row address bit and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

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55.   (Cancelled)

56.   (New) The memory module of claim 54, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

57.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number

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of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

58.   (New) The memory module of claim 57,

wherein the bank address signals of the set of input control signals are received by the logic element,

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wherein a plurality of row/column address signals and the bank address signals are received
from the computer system and buffered by the register, the register transmitting the buffered
plurality of row/column address signals and the buffered bank address signals to the plurality of
DDR memory devices, wherein the at least one row/column address signal received by the logic
element comprises at least one row address signal received by the logic element, and wherein the
plurality of row/column address signals received by the register are separate from the at least one
row address signal received by the logic element, and

wherein the generation of the first number of chip-select signals of the output control signals
by the logic element is based on the logic element responsive at least in part to (i) the at least one
row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set
of input control signals received by the logic element and (iv) the clock signals received from the
phase-lock loop device.

59.   (Cancelled)

60.   (New) The memory module of claim 58, wherein the plurality of DDR memory
devices has one or more attributes selected from a group consisting of: a number of row address bits
per DDR memory device, a number of column address bits per DDR memory device, a number of
bank address bits per DDR memory device, a number of DDR memory devices, a data width per
DDR memory device, a memory density per DDR memory device, a number of ranks of DDR
memory devices, and a memory density per rank, the memory module further comprising a read-
only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to
the computer system, wherein the data characterizes the plurality of DDR memory devices as

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having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

61.   (New) The memory module of claim 1, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices.

62.   (New) The memory module of claim 61, wherein the at least one attribute comprises the number of ranks of DDR memory devices and the memory density per rank.

63.   (New) The memory module of claim 62, wherein the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

64-66. (Cancelled)

67.   (New) A memory module connectable to a computer system, the memory module comprising:

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a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

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wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals.

68.   (Cancelled)

69.   (New) The memory module of claim 67, wherein the memory module is operable to perform successive read accesses from different ranks of DDR memory devices of the plurality of DDR memory devices.

70.   (New) The memory module of claim 67, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

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71.   (New) The memory module of claim 67, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation.

72-74. (Cancelled)

75.   (New) The memory module of claim 1, wherein each DDR memory device of the plurality of DDR memory devices is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank, wherein the memory module further comprises a read-only non-volatile memory device storing data accessible to the computer system, wherein the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has.

76.   (Cancelled)

77.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

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a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number

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of ranks, wherein the at least one row/column address signal received by the logic element

comprises at least one row address signal received by the logic element, and wherein the plurality of

row/column address signals received by the register are separate from the at least one row address

signal received by the logic element, and

wherein the logic element responds to at least the at least one row address signal, the bank

address signals, and the at least one chip-select signal of the set of input signals and the PLL clock

signal by generating a number of rank-selecting signals of the set of output signals that is greater

than double or equal to double the number of chip-select signals of the set of input signals.

78.   (New) The memory module of claim 77, wherein the memory module is operable to

perform back-to-back adjacent read commands which cross DDR memory device boundaries.

79.   (Cancelled)

80.   (New) The memory module of claim 15, wherein the plurality of DDR memory

devices has one or more attributes selected from a group consisting of: a number of row address bits

per DDR memory device, a number of column address bits per DDR memory device, a number of

bank address bits per DDR memory device, a number of DDR memory devices, a data width per

DDR memory device, a memory density per DDR memory device, a number of ranks of DDR

memory devices, and a memory density per rank, the memory module further comprising a read-

only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to

the computer system, wherein the data characterizes the plurality of DDR memory devices as

having one or more attributes that are different from the one or more attributes of the plurality of

DDR memory devices.

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81.   (New) The memory module of claim 80, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

82.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set

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of input control signals from the computer system by selecting at least one rank of the first number

of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the

selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device

operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop

(PLL) device transmits a PLL clock signal to the plurality of DDR DRAM devices, the logic

element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to

the PLL clock signal, a plurality of row/column address signals and the bank address signals, and

(iii) transmits the buffered plurality of row/column address signals and the buffered bank address

signals to the at least one DDR DRAM device of the selected at least one rank, wherein the

row/column address signal received by the logic element comprises a row address signal received

by the logic element, and wherein the plurality of row/column address signals received by the

register are separate from the row address signal received by the logic element, and

wherein the logic element responds to at least (i) the row address signal, (ii) the bank address

signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock

signal by generating a number of rank-selecting signals of the set of output control signals that is

greater than double or equal to double the number of chip-select signals of the set of input control

signals.

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83.   (New) The memory module of claim 82, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR DRAM device boundaries.

84.   (Cancelled)

85.   (New) The memory module of claim 28, wherein the plurality of DDR DRAM devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of bank address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR DRAM devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR DRAM devices.

86.   (New) The memory module of claim 85, wherein the one or more attributes comprise the number of ranks of DDR DRAM devices and the memory density per rank and the data characterizes the plurality of DDR DRAM devices as having fewer ranks of DDR DRAM devices than the plurality of DDR DRAM devices actually has, and as having a greater memory density per rank than the plurality of DDR DRAM devices actually has.

87.   (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

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a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives at least one row address signal, the bank address signals, the second number of chip-select signals, and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register,

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wherein, the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals, and (iii) transmits the buffered bank address signals and the buffered plurality of row address signals to the at least one DDR memory device of the selected at least one rank, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of the row address signals received by the register are separate from the at least one row address signal received by the logic element,

wherein the logic element responds to at least (i) the at least one row address signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals.

88.   (New) The memory module of claim 87, wherein the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries.

89.   (Cancelled)

90.   (New) The memory module of claim 39, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR

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memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

91.   (New) The memory module of claim 90, wherein the one or more attributes comprise the number of ranks of DDR memory devices and the memory density per rank and the data characterizes the plurality of DDR memory devices as having fewer ranks of DDR memory devices than the plurality of DDR memory devices actually has, and as having a greater memory density per rank than the plurality of DDR memory devices actually has.

92-108.   (Cancelled)

109.   (New) The memory module of claim 1, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

110.   (New) The memory module of claim 28, wherein the memory module comprises means for characterizing the plurality of DDR DRAM devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

111.   (New) The memory module of claim 39, wherein the memory module comprises means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from actual attributes of the plurality of DDR memory devices.

112-118.   (Cancelled)

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119.   (New) The memory module of claim 2, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

120.   (New) The memory module of claim 1, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density.

121.   (Cancelled)

122.   (New) The memory module of claim 1, wherein the register comprises a plurality of register devices.

123.   (New – amended)   The memory module of claim 1, wherein the chip-select signals generated by the logic element are a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks.

124.   (Cancelled)

125.   (New) The memory module of claim 123, wherein the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation.

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126.   (New) The memory module of claim 125, wherein the logic element is a device selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device, the logic element transmitting the generated first number of chip-select signals to the plurality of DDR memory devices and not transmitting the at least one row/column address signal, bank address signals, and the second command signal to the plurality of DDR memory devices.

127.   (New) The memory module of claim 125, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of internal banks per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of plurality of DDR memory devices.

128-130.   (Cancelled)

131.   (New) The memory module of claim 1, wherein the plurality of DDR memory devices has one or more attributes selected from a group consisting of: a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of

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bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank, the memory module further comprising a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the one or more attributes of the plurality of DDR memory devices.

132.   (New) The memory module of claim 15, wherein the command signal is transmitted to only one DDR memory device at a time.

133.   (New) The memory module of claim 132, wherein the command signal comprises a read command signal.

134.   (New) The memory module of claim 15, wherein the logic element receives the command signal from the computer system and the register receives the command signal from the computer system.

135.   (New) The memory module of claim 28, wherein the register receives the input command signal of the set of input control signals.

136.   (New) The memory module of claim 43, wherein both the register and the logic element receive at least one command signal of the plurality of input signals.

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STATUS OF CLAIMS

Pursuant to 37 C.F.R. §§ 1.530(e) and 1.941, and with entry of this Amendment, claims 1-24, 26-41, 43, 45-50, 52, 54, 56-58, 60-63, 67, 69-71, 75, 77-78, 80-83, 85-88, 90-91, 109-111, 119-120, 122-123, 125-127, and 131-136 are pending, with claims 25, 42, 44, 51, 53, 55, 59, 64-66, 68, 72-74, 76, 79, 84, 89, 92-108, 112-118, 121, 124, and 128-130 cancelled. The following sets forth in more detail the status of the claims.

A.   Original Claims

The original patent claims are claims 1-51. With entry of this Amendment, Patent Owner cancels original claims 25 and 42 and amends claims 1, 15, 28, 39, and 43. The remaining original claims are pending, except for previously cancelled claims 44 and 51.

B.   Previously Added Claims

New claims 52-136 were previously added. With entry of this amendment, Patent Owner cancels claim 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128-130 and amends claims 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134-136. Discussion and support for these amendments are provided at least in Section II of the Remarks.

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REMARKS

I.   Introduction

On May 31, 2016, the Patent Trial and Appeal Board (the "Board") issued a Decision affirming the Examiner in part. In the Decision, the Board issued a number of new grounds of rejection. (Decision at 102.) The Patent Owner responds by respectfully requesting to reopen prosecution before the Examiner pursuant to 37 C.F.R. § 41.77(b)(1). This Response includes both claim amendments and evidence – the accompanying Second Supplemental Declaration of Dr. Carl Sechen pursuant to 37 C.F.R. § 1.132 – to overcome the new grounds of rejection.

With respect to the claim amendments, the Patent Owner has made the following principle amendments to overcome the new grounds of rejection:

- Phase Lock Loop (PLL) Device

- Register

- Logic Element

The amendments are detailed in Section II. The Patent Owner respectfully submits that the claims, as amended, overcome the new grounds of rejection as detailed in Sections III-VI and in the accompanying Second Supplemental Sechen Declaration.

II.   Claim Amendments and Discussion of Support

The '912 Patent has four original independent claims: claims 1, 15, 28, and 39. Previously, claims 52, 57, 67, 77, 82, and 87 were added independent claims. The amendments to the claims are discussed below with a discussion of support pursuant to 37 C.F.R. §§ 1.530(e) and 1.941. It is also noted that Section I of the Second Supplemental Sechen Declaration ("Second Supp. Sechen Decl.") provides a detailed analysis of the support for the claim amendments.

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A.   Phase Lock Loop (PLL) Device

Claim 1 is amended to recite (exemplary support citations in curly braces):

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, in response to signals received from the computer system {5:28}, the phase-lock loop (PLL) device {50 in Figs. 1A, 1B} transmits a PLL clock signal {5:29} to the plurality of DDR memory devices, the logic element, and the register {5:29-31}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Supp. Sechen Decl. at ¶ 10.

B.   Register

Next, the Patent Owner has amended claim 1 to recite (exemplary support citations in curly braces):

> a register…
>
> wherein, the register {60 in Figs. 1A, 1B} (i) receives, from the computer system {5:31}, and (ii) buffers, in response to the PLL clock signal {Figs. 1A, 1B; 5:31}, a plurality of row/column address signals {7:43-45} and the bank address signals {7:50-51}, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices {30 in Figs. 1A, 1B; 5:34-36}, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register {A_0-A_n in Figs. 1A, 1B} are separate from the at least one row address signal received by the logic element {A_{n+1} in Figs. 1A, 1B}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 11.

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C.   Logic Element

Additionally, claim 1 is amended to recite (exemplary support citations in curly braces):

> the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, …

> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals {Figs. 1A, 1B, 3A, 3B; 17:28-19:521 22:50-63; 23:6-25} of the output control signals in response {6:55-63} at least in part to (i) the at least one row address signal {A_{u+1} in Figs. 1A, 1B; A13 in Figs. 3A, 3B; 7:46-53}, (ii) [a] the bank address signals {B_0-B_m in Figs. 1A, 1B; BA_0, BA_1 in Figs. 3A, 3B; 7:46-53}, and (iii) the at least one chip-select signal {CS_0, CS_1 in Fig. 1A; CS_0 in Fig. 1B; 7:46-53} of the set of input control signals and (iv) the PLL clock signal {Figs. 1A, 1B; 5:29-30; "clk_in" in 17:28-19:52}.

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations. *See also* Second Suppl. Sechen Decl. at ¶ 12.

D.   Other Amendments

A number of other amendments were made for conformity.

The dependency of claim 43 has been changed to claim 39 in view of the cancellation of claim 42.

The dependency of new claim 54 has been changed to new claim 52 in view of the cancellation of new claim 53. The recitation of "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" previously in new claim 54 has been deleted in view of the amendment to new claim 52.

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In new claim 123, the recitation "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating" has been replaced by "the chip-select signals generated by the logic element are" in view of the amendment to claim 1.

The dependency of new claim 125 has been changed to new claim 123 in view of the cancellation of new claim 124. The phrase "the row address bit" has been changed to "the at least one row address signal" and the recitation "wherein the transmission of the buffered bank address signals by the register is timed to the clock signals received from the phase-lock loop device, and the generation of the first number of chip-select signals by the logic element is timed to the clock signals received from the phase-lock loop device" has been deleted in view of the amendment to claim 1.

The dependency of new claim 131 has been changed to claim 1 in view of the cancellation of new claims 128-130.

The dependency of new claim 134 has been changed to claim 15 in view of the cancellation of claim 25.

The term "the bank address signals" has been deleted from claims 134-136 in view of the amendments to claims 15, 28 and 39.

III. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122, and 132-136 Are Patentable Over Amidi In View Of Dell 2 (Ground 5)

Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29 , 31, 32, 34-43, 45-50, 120-122 and 132-136 have been rejected by the Board as obvious over Amidi in view of Dell 2. These amendments distinguish the claims from the combination of Amidi and Dell 2. *See* Second Supp. Sechen Decl. at Section II.

Dell 2 is cited for teaching or suggesting "a logic element receiving and using free signals, including a bank address signal", and Amidi is cited for its "suggestion to use other types of

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memory devices." (Decision, 43.) The Decision then concludes that the combination of Amidi and Dell 2 teaches or suggests generating a chip-select, CAS, or rank selecting signal in response to a bank address signal. (Decision, 81.) To address the Board's rejection, Patent Owner narrowed the claim to include:

- "in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register"
- "the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element"
- "the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal."

As described herein, the claim amendments highlight at least two differences between the '912 invention and the prior art.

First, the claim amendments now require: in response to signals received from the computer system, the phase-lock loop (PLL) device transmit a PLL clock to the plurality of DDR memory devices, the logic element, and the register. Amidi transmits a PLL clock signal to the register and memory, but not to the CPLD. Thus, Amidi does not disclose the PLL device transmitting the PLL clock to the *logic element*; the output of PLL 606 is neither directly nor indirectly transmitted to the

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CPLD 604. *See* Second Supp. Sechen Decl. at ¶¶ 18-19. Additionally, a POSITA would not be motivated or inclined to transmit the PLL clock to CPLD 604. *Id.* at ¶ 20.

Second, the amended claims now also require that the logic element generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals. Instead, the control signals (rcs0a, rcs0b, rcs1a, rcs1b, rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select signals. Thus, Amidi does not disclose the CPLD generating the gated CAS signals or chip-select signals in response to *the bank address signals.* Second Supp. Sechen Decl. at ¶¶ 21-22. Moreover, since the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604, a POSITA would understand that the PLL clock does not control the operation of CPLD 604. Thus, Amidi is further deficient by failing to disclose the CPLD generating the gated CAS signals or chip-select signals in response to the *PLL clock signal. Id.* at ¶ 18-19.

Dell 2 does not cure the deficiencies of Amidi with respect to the amended claim. Dell 2 merely discloses a remapping or reassignment of a row address bit (A12) to be used as a bank address bit (BA1). Dell 2 does not disclose using bank address signals to generate a chip-select signal or a CAS signal. Second Supp. Sechen Decl. at ¶ 25.

Even taken in combination, Amidi and Dell 2, it would not be obvious to a POSITA to modify Amidi's system to provide the bank address signals to the CPLD device, and generate chip-select signals based on the bank address signals and a row address signal. As amended, the claims require that the *logic element receives* at least one row address signal and *bank address signals*, and require that *the register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices. The claims also require the plurality of row/column

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address signals received by the register are separate from the at least one row address signal received by the logic element. In other words, in the configuration recited by the claims, the bank address signals are received by the logic element, the register and the plurality of memory devices. Under such circumstances, Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and the at least one row address signal). The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals. Second Supp. Sechen Decl. at ¶¶ 23-24 and 26.

Based on the above, it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

While claims 132-133 are patentable over Ground 5 based on amended claim 15 from which they depend, these claims are patentable for an additional reason. Specifically, claim 132 (and its dependent claim 133) recite that "the command signal is transmitted to only one DDR memory device at a time." Claim 16 (and its dependent claim 17) have a similar recitation, and the Board found that Amidi and Dell 2 were deficient as to this recitation. (Decision, 75-77, 82-83.) Based on that reasoning, claims 132 and 133 are similarly patentable over Ground 5. It is believed that the inclusion of these claims under Ground 5 has been in error.

IV. Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 Are Patentable Over Micron In View Of Amidi (Ground 13)

Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 have been rejected by the Board as obvious over Micron in view of Amidi.

The Decision relied on two different cases proposed by Requester 3 to reject the claims. The first case refers to a memory controller that generates one row address signal more than the actual

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memory devices use (Decision, 94), and the second case refers to a memory controller that generates one bank address signal more than the actual memory devices use (Decision, 94-95.)

As discussed above, the claims, as amended, are directed to a logic element separately receiving a row address signal (i.e., similar to the first case). As claimed, the registers, and thereby the plurality of memory devices, use the bank address signals. Thus, the amended claims exclude the second case involving one more bank address signal than required by the actual memory devices. In other words, the rationale of the second case does not apply to the amended claims.

Instead, the claims require that the logic element receives at least one row address signal separate from the address signals received by the register, and as discussed above, Amidi does not suggest using a bank address signal for generating CAS signals or chip-select signals (or rank multiplication) when a row address signal is not used by the actual memory devices. Additionally, Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Second Supp. Sechen Decl. at ¶ 29.

The Decision rejects the claims under the first case based on what a POSITA "would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." (Decision, 95.) The Decision concludes, based on Requester 3's expert, Dr. Kozyrakis, that a POSITA would have recognized to use bank address signals to generate chip-select signals. (*Id.*, 96.) Additionally, the Decision concludes that a POSITA, employing their background knowledge, would have known that additional signals are needed to generate the chip-select signals and would turn to bank address signals in order to multiply ranks. (*Id.*, 97.) But, Amidi already claims to provide rank multiplication without the use of bank address signals. Second Supp. Sechen Decl. at ¶ 30.

The conclusions of Requester 3's expert at best represent how an expert, not a POSITA, would understand Amidi's disclosure. There is no question that a POSITA would recognize the conventional use of bank address signals in Amidi, but there is no suggestion of using the bank

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address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Amidi is representative evidence of what a POSITA would understand. No cited art suggests a recognition of the need for bank address signals for rank multiplication, or for generation of CAS signals or chip-select signals. Amidi was plainly not aware of any need – as the bank address signals are not used to generate the chip select signals. A POSITA reading Amidi would have recognized that Amidi claims to achieve rank multiplication without bank signals for generating chip-select signals and would not have recognized an unconventional use for the bank address signals. Second Supp. Sechen Decl. at ¶ 31.

Dr. Kozyrakis, an expert, says that bank address signals are necessary for proper generation of chip select signals, but a POSITA taking Amidi at face value would have understood otherwise. Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Second Supp. Sechen Decl. at ¶ 32.

Regardless of whether bank address signals are necessary for proper operation, this is a conclusion of fact and not an indication of what a POSITA would recognize. Amidi's complete omission of using bank address signals is formidable evidence that a POSITA looking at Amidi would not think bank address signals are necessary. Rather a POSITA would conclude that Amidi is operative without bank address signals for generating control signals. To suggest otherwise forces upon Amidi an operating principle that is not present. Namely the recognition that bank address signals are a necessary input for generating chip-select signals, when Amidi clearly does not. Second Supp. Sechen Decl. at ¶ 33.

Requester 3's expert asserts that "the nature of standard DDR commands motivates a person of ordinary skill in the art to use bank address signals to generate chip-select signals." (Decision, 96 (internal citations omitted).) While I agree that a POSITA is not an automaton and possesses common sense, understanding the nature of standard DDR commands is a skill level of an expert. A POSITA possesses far less creativity and skill than an expert, and in view of Amidi would not entertain the nature of standard DDR commands. A POSITA reading of Amidi would give some

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deference to Amidi and understand that its principle of operation does not require bank address signals for generation of chip-select signals. Second Supp. Sechen Decl. at ¶ 34.

Ultimately, regardless of how necessary bank address signals are for generation of chip-select signals, Amidi was plainly unaware of this necessity. It is precisely recognition of this necessity and solution which underlie Netlist's discovery. Second Supp. Sechen Decl. at ¶ 35.

Based on the above, it would not be obvious to a POSITA to combine Micron and Amidi to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Micron and Amidi fails to disclose the claimed invention. Therefore, even in combination, Micron in view of Amidi fails to disclose all of the claim recitations in the claims.

While claims 132-133 are patentable over Ground 13 based on amended claim 15 from which they depend, these claims are patentable for an additional reason. Requester 3 never presented a proposed rejection for claims 132 and 133 under Ground 13 during the reexamination. *See* Requester 3's February 2012 Response, 23-25. It is believed that the inclusion of these claims under Ground 13 has been in error.

V.   Claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 Are Patentable Over Amidi In View Of Dell 184 (Ground 20)

Claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Board as obvious over Amidi in view of Dell 184.

These amendments distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV.

VI.   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-11, and 120-126 Are Patentable Over Micron In View Of Amidi, Further In View Of Olarig (Ground 21)

Claims 52-54, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Board as obvious over Micron in view of Amidi and Olarig.

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These amendments distinguish the claims from the combination of Micron, Amidi and
Olarig, as discussed above. *See also* Second Supp. Sechen Decl. Section V.

VII.   Additional Points

Neither the claim amendments nor these Remarks should be in any way construed that the
Patent Owner agrees or acquiesces to any of the new grounds of rejection in the Board's Decision.
The decision to not directly address in this Response any specific points in the Board's Decision
does not indicate that Patent Owner agrees with or acquiesces to these specific points. The Patent
Owner reserves its right to seek or defend similar claims in related applications or patents, which
may be in reexamination.

Furthermore, the Patent Owner discuses above only some of the claim features of the '912
Patent for the sake of brevity and some of the reasons of patentability with respect to the new
grounds of rejection. These discussions should not be interpreted as Patent Owner asserting or
acquiescing that the patentability of the current pending claims is because of only these features or
reasons.

Additionally, where the Patent Owner has previously presented different arguments, the
Patent Owner's decision to not raise them in this Response should not be construed as the Patent
Owner abandoning or relinquishing those arguments. The Patent Owner reserves the right to re-
present those previous arguments in this reexamination or in related application or patents, which
may be in reexamination.

VIII.   Conclusion

For the above reasons, the Patent Owner respectfully requests that the pending claims be
confirmed or allowed over the new grounds of rejection.

If the Patent Office determines that relief is required, the Patent Owner petitions for any
required relief and authorizes the Commissioner to charge the cost of such petitions and/or other

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fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **635162800300.**

Dated: July 31, 2016   Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 1.903, the undersigned, on behalf of the Patent Owner, hereby certifies that a copy of the following documents:

1.   This Patent Owner's Response Requesting to Reopen Prosecution, including certificate of service (53 pages) and

2.   Second Supplemental Declaration of Dr. Carl Sechen, including Exhibit AAA.

was served on the third party requesters via first class mail on the date below. The name and address of the parties served are as follows.

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(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of: Jayesh BHAKTA et al.	Examiner: B. PEIKARI
Control Nos.: 95/001,339; 95/000,578; 95/000,579	Art Unit: 3992
Filed: October 20, 2010; October 21, 2010; June 8, 2010	Conf. No.: 5035; 8810; 3547
For: MEMORY MODULE DECODER	

SECOND SUPPLEMENTAL DECLARATION OF DR. CARL SECHEN UNDER 37 C.F.R. § 1.132

Mail Stop Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Dr. Carl Sechen, declare as follows:

1.   I have been retained by Netlist, Inc., the owner of U.S. Patent No. 7,619,912 ("the '912 patent") to provide a supplemental technical opinion concerning the '912 patent, and certain prior art references cited in the above-captioned *inter partes* reexamination proceedings, which are discussed in further detail below.

2.   In my initial declaration dated July 5, 2011, I summarized my technical background and provided my then current Curriculum Vitae. For this supplemental declaration, I am providing an updated Curriculum Vitae as Exhibit AAA.

3.   I have reviewed and am familiar with the specification of the '912 patent. I have also reviewed and am familiar with the Decision On Appeal issued by the Patent and Trial Appeal Board (the "Board") and mailed on May 31, 2016 ("the Decision").

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4.   I have also reviewed and am familiar with the prior art cited in the Decision. This prior art includes:

- U.S. Patent Publication No. 2006/0117152 to Amidi et al. ("Amidi");

- U.S. Patent No. 5,926,827 to Dell et al. ("Dell 1");

- U.S. Patent No. 6,209,074 to Dell et al. ("Dell 2");

- U.S. Patent No. 6,414,868 to Wong et al. ("Wong");

- U.S. Patent No. 5,745,914 to Connolly et al. ("Connolly");

- U.S. Patent No. u,260,127 to Olarig et al. ("Olarig");

- U.S. Patent No. 6,446,184 to Dell et al. ("Dell 184");

- Micron, DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF28672 Data Sheet, 2002 ("Micron");

- HP Printer Memory Explain 1-7 (Jan. 21, 2014), available at http://warshaft.com/hpmem/htm ("Memory Explained"); and

- JEDEC 21-C (January 2002), JEDEC JESD82-4B (May 2003) and JEDEC 79C (March 2003) referenced in the Office Action at 4 and sometimes collectively referred to as the JEDEC Standards.

5.   My understanding of the definitions and standards associated with proceedings at the Patent Office is set forth in my initial declaration, including at ¶¶ 10-11.

6.   I am being compensated by Patent Owner in connection with the preparation of this declaration. I am being paid regardless of the conclusions or opinions I reach. I have no personal or financial stake or interest in the outcome of the present reexamination proceedings.

7.   In this declaration, I explain how the disclosure of the '912 Patent supports the claim amendments in Patent Owner's Response to Decision on Appeal ("Decision Response"), accompanying this supplemental declaration. The claim amendments are directed to the following subject matter:

- Phase lock loop (PLL) circuit

- Register

- Logic element

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8.   Moreover, I explain that the prior art applied by the Decision in its new grounds of rejections at least fail to disclose or suggest the claimed inventions as amended in Patent Owner's Decision Response.

9.   I address each of these issues separately below.

I.   Claim Amendments

A.   Phase Lock Loop (PLL) Device

10.   I understand that claim 1 is amended to include claim language for a PLL clock signal. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (addition amendments underlined and support citations in curly braces):

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, in response to signals received from the computer system {5:28}, the phase-lock loop (PLL) device {50 in Figs. 1A, 1B} transmits a PLL clock signal {5:29} to the plurality of DDR memory devices, the logic element, and the register {5:29-31}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

B.   Register

11.   I understand that claim 1 is amended to include claim language for the register. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (addition amendments underlined and support citations in curly braces):

> a register…
>
> wherein, the register {60 in Figs. 1A, 1B} (i) receives, from the computer system {5:31}, and (ii) buffers, in response to the PLL clock signal {Figs. 1A, 1B; 5:31}, a plurality of row/column address signals {7:43-45} and the bank address signals {7:50-51}, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices {30 in Figs. 1A, 1B; 5:34-36}, wherein the at least one row/column address

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> signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register {A_0-A_n in Figs. 1A, 1B} are separate from the at least one row address signal received by the logic element {A_{n+1} in Figs. 1A, 1B}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

C.   Logic Element

12.   I understand that claim 1 is amended to include claim language for the logic element. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (deletion amendments bracketed, addition amendments underlined, and support citations in curly braces):

> the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, …

> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals {Figs. 1A, 1B, 3A, 3B; 17:28-19:52} 22:50-63; 23:6-25} of the output control signals in response {6:55-63} at least in part to (i) the at least one row address signal {A_{n+1} in Figs. 1A, 1B; A13 in Figs. 3A, 3B; 7:46-53}, (ii) [a] the bank address signals {B_0-B_m in Figs. 1A, 1B; BA_0, BA_1 in Figs. 3A, 3B; 7:46-53}, and (iii) the at least one chip-select signal {CS_0, CS_1 in Fig. 1A; CS_0 in Fig. 1B; 7:46-53} of the set of input control signals and (iv) the PLL clock signal {Figs. 1A, 1B; 5:29-30; "clk_in" in 17:28-19:52}.

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

D.   Other Amendments

13.   I understand that Patent Owner has made other claim amendments conform the claim language to the above main claim amendments.

II.   Amidi In View Of Dell 2 – Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 and 132-136 (Ground 5)

14.   I have been informed that claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 and 132-136 have been rejected by the Decision as obvious over

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Amidi in view of Dell 2. I confirm that the amended claim language introduced by the Decision
Response distinguishes these claims for this combination of Amidi and Dell 2, as will be
discussed below.

15.   I have been informed that the Decision concludes that the combination of Amidi
and Dell 2 teaches or suggests generating a chip-select, CAS, or rank selecting signal in response
to a bank address signal. The Decision refers to its discussion at pages 40-43 of the bank address
limitation with respect to claim 7 to support this conclusion. (Decision, 81.) I have also been
informed the Decision bases the rejection on the breadth of the claims. In particular, the
Decision states:

> The above teachings in Dell 2 teach or suggest a logic element receiving and using free
> signals, including a bank address signal, to provide the needed bank address signals based
> on the difference between the actual and expected number of banks for the memory
> devices of the memory module system. Combining this teaching with Amidi's
> suggestion to use other types of memory devices (Amidi ¶ 71) would have predictably
> yielded the recited "both the bank address signals of the set of input control signals are
> received by both the logic element and the register" in claim 7 so that the necessary rank
> chip select signals discussed in Amidi are produced. That is, Amidi and Dell 2,
> collectively, teach that ranks and banks both may be expanded; therefore, a skilled artisan
> would recognize various combinations of inputs to achieve expansion including bank
> address inputs as broadly recited. This combination also addresses the demand for
> increased memory capacity and compatibility issues. *See, e.g.,* R2 August 14, 2013
> Comments 12 (citing 3d Bagherzadeh Decl. ¶ 37), 29-30, 38 (citing Amidi ¶ 71).
> Moreover, this combination further teaches using the logic circuit or element (e.g.,
> Amidi's CPLD) to receive bank address signals for the above-discussed purpose.

(Decision, 43.)

16.   As discussed above, the claims have been amended to include language about the
PLL, register, and logic element. A POSITA would understand that the amendments narrow the
scope of the claim to a memory module in which the bank address signals are received by the
register (and thereby the plurality of DDR memory devices) and the logic element, and at least

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one row address signal – *separate* from the plurality of row/column address signals received by the register – is received by the logic element. A POSITA would understand that for such a configuration, generating a CAS signal or a chip-select signal in response at least in part to the bank address signals and the at least one row address signal is nonobvious in view of Amidi and Dell 2, as discussed in more detail below.

17.   In particular, I see that the amended claims now require in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register. I also see the amended claims now require that the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Additionally, I see that the amended claims now require that the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element.

18.   Such language, individually and in combination, distinguishes these claims from the combination of Amidi and Dell 2. First, Amidi's CPLD does not generate output control signals in response to the PLL clock signal. As amended, the claims require the PLL device transmit a PLL clock signal to the logic element, in response to signal received from the computer system, and the logic element generates gated CAS signals or chip-select signals in response at least in part to the PLL clock signal. By providing a PLL clock signal from the PLL 50 to the plurality of DDR memory devices, the logic element 40 and the register 60, the memory module of claim 1 of the '912 patent is configured to provide reliable synchronous operation. (*See* Sechen I, ¶ 16.) Such language distinguishes these claims from Amidi, which transmits the PLL clock signal to the register and memory, but not to the CPLD.

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19.   Amidi discloses PLL 606 that receives differential clock signals CLK0 and CLK0_N, generated by the memory controller, from the module connector 602. PLL 606 "relays the CLK0 and CLK0_N signals to register 608 and memory devices 306." (Amidi, ¶ [0050], Figs. 6A and 6B). Amidi's CPLD 604, however, receives differential clock signals CLK0 and CLK0_N directly from the module connector 602. The output of PLL 606 is neither directly nor indirectly (e.g., through a clock buffer) transmitted to the CPLD 604. Hence, a POSITA would understand that the output of PLL 606 does not control the operation of CPLD 604. Instead, operation of CPLD 604 is controlled by the system clock. Thus, Amidi's CPLD cannot generate output signals based on the PLL clock signal that it does not receive.

20.   A POSITA would not have been motivated or inclined to change the design of Amidi's memory module because doing so would have significantly affected the timing margins for synchronous operation of the memory modules, and likely would render the prior art memory modules inoperable or unreliable. In particular, adding a load (e.g., a logic device) to the PLL output would have greatly impacted performance, and would have required significant redesign of the memory module layout in order to achieve accurate synchronous operation and reliability. (*See* Sechen I, ¶17.)

21.   Second, Amidi's CPLD does not generate output control signals in response to the bank address signals. Amidi discloses a CPLD 410/604 that emulates a two rank memory module on a four rank memory module. As illustrated in Fig. 6A, Amidi's CPLD receives, from the module connector, two chip select signals (cs0 and cs1), an address signal (Add(n)), CAS, RAS, WE, CLK0, and CLK0_N. (Amidi, ¶ 50.) Based on these input signals, Amidi's CPLD generates control signals rcs0a, rcs0b, rcs1a, rcs1b, rcs2a, rcs2b, rcs3a, and rsc3b. (*Id.* ¶¶ 52, 60.) The control signals generated by Amidi's CPLD are based on a row address signal, not on bank address signals.

22.   Amidi never discloses that bank address signals are received by the CPLD. (*See also,* Sechen I, ¶ 23; Sechen II, ¶¶ 14-15). Therefore, because Amidi's CPLD does not receive bank address signals, Amidi does not disclose generating control signals based on bank address signals. I understand that the Decision agreed that Amidi's CPLD does not receive bank address signals. (Decision at 23.)

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23.   Even taking Amidi in combination with Dell 2, it would not be obvious to a
POSITA to modify Amidi's system to provide bank address signals to the CPLD device, and
generate control signals based thereon. The rejection of the claims relies on Amidi's use of
Add(n) to generate the control signals. Amidi, for example, provides an address signal, Add(n),
to the CPLD 604 that decodes Add(n) with inputs CS0 and CS1 to generated output signals
rCS0-rCS3. (Amidi Fig. 5.) Add(n) is not transmitted to the memory devices (and can be used
by Amidi for rank multiplication). There is no suggestion in Amidi to use a bank address signal
for generation of control signals. Amidi does not discuss any rationale for making this
modification, because Amidi's CPLD is alleged to be fully functional without receiving any bank
address signals. For example, Amidi discloses the internal circuitry of the CPLD – which does
not utilize any bank address signals. (Amidi, ¶ 64-70, Fig. 8.) Instead, Amidi discloses that the
register receives the bank address signals so that they can be passed through to the DDR memory
devices for their normal function of specifying the bank from which data is to be read or written.
Furthermore, there is no suggestion or recognition in Amidi or Dell 2 to use both the bank
address signals and a row address signal for rank multiplication or the generation of chip-select
signals or CAS signal signals.

24.   As amended, the claims are narrowed in scope such that a POSITA would
understand that at least one row address signal is received by the logic element and not received
by the register, but that the bank address signals are received and used by the plurality of
memory devices (e.g., during an activate command, a read command or a write command). In
particular, the claims require that the *logic element receives* at least one row address signal and
bank address signals, and require that *the register* (i) *receives*, from the computer system, and
(ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and
the bank address signals, and (iii) transmits the buffered plurality of row/column address signals
and the buffered bank address signals to the plurality of DDR memory devices. The claims also
require the plurality of row/column address signals received by the register are separate from the
at least one row address signal received by the logic element. In other words, in the
configuration recited by the claims, the bank address signals are received by the logic element,
the register and the plurality of memory devices. Under such circumstances, Amidi does not use
bank address signals to generate control signals (and certainly not the bank address signals and

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the at least one row address signal). The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals.

25.   Dell 2 discloses a remapping or reassignment of a row address bit (A12) to be used as a bank address bit (BA1). There is no disclosure or suggestion of using bank address to generate a control signal, such as a chip-select signal or a CAS signal. (Sechen I, ¶¶ 27, 73; Sechen II, ¶ 16.)

26.   Taking Amidi and Dell 2 together for all that they teach, it would not be obvious to a POSITA to use bank address signals to generate control signals for rank multiplication, when the bank address signals are used by the plurality of memory devices. As amended, the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers. Amidi and Dell 2 at best would suggest to a POSITA to use such a signal (i.e., one that is received separate by the logic element and not by the registers) for generating a control signal. There is no suggestion to repurpose a bank address signal for rank multiplication purposes. Certainly, there is no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

27.   Based on the above, I find that it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

III.   Micron In View Of Amidi – Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 (Ground 13)

28.   I have been informed that claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 have been rejected by the Decision as obvious over Micron in view of Amidi. I confirm that the

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amended claim language introduced by the Decision Response distinguishes these claims for this combination of Micron and Amidi.

29.   I have been informed that the Decision relied on two different cases proposed by Requester 3 to reject the claims. The first case refers to a memory controller that generates one row address signal more than the actual memory devices use (Decision, 94), and the second case refers to a memory controller that generates one bank address signal more than the actual memory devices use (Decision, 94-95.) As discussed above, the claims, as amended, are directed to a logic element separately receiving a row address signal (i.e., similar to the first case). As claimed, the registers, and thereby the plurality of memory devices, use the bank address signals. Thus, the amended claims exclude the second case involving one more bank address signal than required by the actual memory devices. In other words, the rationale of the second case does not apply to the amended claims. Instead, the claims require that the logic element receives at least one row address signal separate from the address signals received by the register, and as discussed above in Section II, Amidi does not suggest using a bank address signal for generating CAS signals or chip-select signals (or rank multiplication) when a row address signal is not used by the actual memory devices. Additionally, Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

30.   I have also been informed that the Decision rejects the claims under the first case based on what a POSITA "would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." (Decision, 95.) The Decision concludes, based on Requester 3's expert, Dr. Kozyrakis, that a POSITA would have recognized to use bank address signals to generate chip-select signals. (*Id.*, 96.) Additionally, the Decision concludes that a POSITA, employing their background knowledge, would have known that additional signals are needed to generate the chip-select signals and would turn to bank address signals in order to multiply ranks. (*Id.*, 97.) But, Amidi already claims to provide rank multiplication without the use of bank address signals.

31.   The conclusions of Requester 3's expert at best represent how an expert, not a POSITA, would understand Amidi's disclosure. There is no question that a POSITA would

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recognize the conventional use of bank address signals in Amidi, but there is no suggestion of using the bank address signal for rank multiplication or the generation of chip-select signals or CAS signal signals. Amidi is representative evidence of what a POSITA would understand. No cited art suggests a recognition of the need for bank address signals for rank multiplication, or for generation of CAS signals or chip-select signals. Amidi was plainly not aware of any need – as the bank address signals are not used to generate the chip select signals. A POSITA reading Amidi would have recognized that Amidi claims to achieve rank multiplication without bank signals for generating chip-select signals and would not have recognized an unconventional use for the bank address signals.

32.   Dr. Kozyrakis, an expert, says that bank address signals are necessary for proper generation of chip select signals, but a POSITA taking Amidi at face value would have understood otherwise. Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

33.   Regardless of whether bank address signals are necessary for proper operation, this is a conclusion of fact and not an indication of what a POSITA would recognize. Amidi's complete omission of using bank address signals is formidable evidence that a POSITA looking at Amidi would not think bank address signals are necessary. Rather a POSITA would conclude that Amidi is operative without bank address signals for generating control signals. To suggest otherwise forces upon Amidi an operating principle that is not present. Namely the recognition that bank address signals are a necessary input for generating chip-select signals, when Amidi clearly does not.

34.   Requester 3's expert asserts that "the nature of standard DDR commands motivates a person of ordinary skill in the art to use bank address signals to generate chip-select signals." (Decision, 96 (internal citations omitted).) While I agree that a POSITA is not an automaton and possesses common sense, understanding the nature of standard DDR commands is a skill level of an expert. A POSITA possesses far less creativity and skill than an expert, and in view of Amidi would not entertain the nature of standard DDR commands. A POSITA

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reading of Amidi would give some deference to Amidi and understand that its principle of operation does not require bank address signals for generation of chip-select signals.

35.   Ultimately, regardless of how necessary bank address signals are for generation of chip-select signals, Amidi was plainly unaware of this necessity. It is precisely recognition of this necessity and solution which underlie Netlist's discovery.

36.   Based on the above, I find that it would not be obvious to a POSITA to combine Micron and Amidi to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Micron and Amidi fails to disclose the claimed invention. Therefore, even in combination, Micron in view of Amidi fails to disclose all of the claim recitations the claims.

IV.   Amidi In View Of Dell 184 – Claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 (Ground 20)

37.   I have been informed that claims 52-54, 56, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Decision as obvious over Amidi in view of Dell 184. I confirm that the amended claim language introduced by the Decision Response distinguishes these claims for this combination of Amidi and Dell 184.

38.   The Decision recognizes that the teachings of Dell 184 are similar to the teaching of Dell 2. (Decision, 92.) For brevity, the discussion above with respect to the rejection under Amidi and Dell 2 applies to the rejection under Amidi and Dell 184. Accordingly, the amended claims are believed to distinguish over this rejection introduced by the Decision.

39.   The Decision goes further with respect to the combination of Amidi and Dell 184. The Decision asserts that "combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal." (Decision, 93.)

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40.   As amended, the claim cannot be said to be a predictable combination of the teachings of Amidi and Dell 184. As described above, Amidi uses the address signal received by the CPLD, and not used by the actual memory devices, to generate chip-select signals for rank multiplication. Amidi never suggests using bank address signals, which are expressly received by the register (and thereby used by the memory devices) in the claims as amended. Dell 184 discloses using bank address signals for remapping – not rank multiplication. There is no indication that a bank address signal would be used to generate CAS signals, chip-select signals, or rank selection signals.

41.   Furthermore, Dell 184's remapping function at best uses a row address input for bank address remapping. The bank address signal of Dell 184 is an output of the remapping function. The address is the input for the remapping function. (*See, e.g.*, Dell 184, Fig. 1A.) Dell 184 does not use bank address inputs for rank multiplication. There is no indication that bank address signals would be used to generate CAS signals, chip-select signals, or rank selection. Additionally, Amidi and Dell 184 provide no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

42.   Based on the above, I find that it would not be obvious to a POSITA to combine Amidi and Dell 184 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 184 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 184 fails to disclose all the claim recitations of the claims.

V.   Micron In View Of Amidi and Olarig – Claims 52-54, 67-71, 77-79, 82-84, and 87-89 (Ground 21)

43.   I have been informed that claims 52-54, 67-71, 77-79, 82-84, and 87-89 have been rejected by the Decision as obvious over Micron in view of Amidi and Olarig. I confirm that the amended claim language introduced by the Decision Response distinguishes these claims from this combination of Micron, Amidi and Olarig.

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44.   For brevity, the discussion above with respect to the rejection under Micron and Amidi applies to the rejection under Micron, Amidi and Olarig. As discussed below, the amended claims are believed to distinguish over this rejection introduced by the Decision.

45.   The Decision states that "Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49-51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.*" (Decision, 100.) Further, the Decision states that a POSITA, "armed with Olarig's and Amidi's teaching and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as a chip-select signal." (*Id.*, 101.)

46.   With the amended claim, a POSITA would not reach the same conclusion adopted in the Decision. As discussed herein, Amidi discloses using an address signal received by the CPLD, and unused by the actual memory devices, to generate chip-select signals. Amidi does not suggest, nor would a POSITA recognize and understand, to use a bank-address signal to generate the chip-select signals. As amended, the claims require at least one row address signal received by the logic element and not received by the registers. In contrast, the bank address signals are coupled to the registers (and thereby to the memory devices). As discussed above in Section III, Micron in view of Amidi is similarly deficient. Olarig is also deficient.

47.   The claims, as amended, require generating the CAS signals or chip-select signals (or rank selection signals) in response at least in part to a row address signal and the bank address signals. Olarig is essentially mapping a bank address bit to a *column* address bit during the column address time. There is no disclosure of generating a chip-select signal in response to at least a *row* address signal and bank address signals.

48.   Olarig does not teach a POSITA to use bank address signals to generate a chip-select signal. The conclusion that a POSITA would reach this understanding is purely speculative. The Decision recognizes that "there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited." (Decision, 101.) This recognition is a key to what a POSITA would understand.

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49.   Olarig teaches mapping bank address signals of an SDRAM address to address signals of an EDO memory. (Olarig, Fig. 6.) Mapping a bank address signal to an address signal has absolutely nothing to do with generating a chip-select signal (or a CAS signal or other rank multiplying signal). As described above, Amidi does not use bank addresses at all for generating chip-select signals. Thus, it is unclear to me how a POSITA would combine the two teachings and generate a chip-select signal based on bank-address signals. There is no indication in the Decision of any background knowledge that I could identify that leads me to believe a POSITA would have reached this conclusion.

50.   Furthermore, Olarig is directed to an asynchronous EDO memory. EDO memories do not use chip-select signals at all. Thus, a POSITA would not conclude based on the combination of Amidi and Olarig to generate chip select signals based on bank address signals, given that neither system suggests doing so.

51.   Furthermore, the amended claims introduce a PLL clock signal, and introduce generating CAS signals, chip-select signals, or other rank selection signals in response to at least the PLL clock signal. Olarig is an asynchronous EDO memory that does not include a chip-select signal at all, and would be incompatible with a synchronous system using a PLL. Olarig and Amidi do not suggest using a PLL clock input for generating chip-select signals, CAS signals or rank selection signals. (*See* Sechen I, ¶ 16.)

52.   Even if Olarig were not an EDO memory, but a synchronous DDR memory device, Fig. 6 indicates that Olarig merely discloses a mapping between a bank address of an SDRAM and an EDO address, A10. A POSITA would understand A10 to be an address signal, not a chip-select signal.

53.   Based on the above, I find that it would not be obvious to a POSITA to combine Micron, Amidi and Olarig to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Micron, Amidi and Olarig fails to disclose the claimed invention. Therefore, even in combination, Micron, Amidi and Olarig fail to disclose all the claim recitations of the claims.

I declare that all statements made herein of my own knowledge are true and that all

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statements made on information and belief are believed to be true; and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: July 31, 2016

Carl Sechen, Ph.D.

la-1324725

Exhibit AAA

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Research Interests

My research interests center primarily on the design and computer-aided design of digital and analog integrated circuits. Ongoing projects include: optimal gate size and threshold voltage selection for absolute leakage and/or dynamic power minimization subject to a frequency constraint; fast, accurate simulation-based timing analysis; more accurate power estimation for digital circuits; ultra low power time-to-digital conversion; resilient logic and memory for truly sub-threshold operation; for example, highly reliable, very low area overhead asynchronous logic design operating at sub-threshold voltages. Also, the design of secure ICs that cannot be reverse engineered.

Education

Ph.D., Electrical Engineering, University of California, Berkeley, 1986
     Thesis: *Placement and Global Routing of Integrated Circuits Using Simulated Annealing*
     Advisor: Prof. Alberto Sangiovanni-Vincentelli
M.S., Electrical Engineering, Massachusetts Institute of Technology, 1977
     Advisor: Prof. Stephen Senturia
B.E.E., Electrical Engineering, University of Minnesota, 1975

Employment history

Professor, University of Texas at Dallas August 15, 2005 – present
Professor, University of Washington July 1999 – August 14, 2005
Associate Professor, University of Washington July 1992 – June 1999
Associate Professor, Yale University July 1990 – June 1992
Assistant Professor, Yale University July 1986 – June 1990

University Administrative Positions

Director of ECS Tech Support Services, UTD, June 2012 – February 2014

Honors and Awards

- Received the *Distinguished Teaching Award* for the Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2014.
- Received the *Distinguished Teacher of the Year* Award, Dept. of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2008.
- Elected *IEEE Fellow* in 2002
- Received the *Outstanding Research Advisor* Award, Department of Electrical Engineering, University of Washington, 2002.
- Received the *Best Project Award*, NSF Center for the Design of Digital and Analog ICs (CDADIC), July 2002.
- Received the Semiconductor Research Corporation's 2001 *SRC Inventor's Recognition Award*
- Received the Semiconductor Research Corporation's 1994 *SRC Technical Excellence Award*
- Received the Semiconductor Research Corporation's 1988 *SRC Inventor's Recognition Award*

Graduated Ph.D. Students

1. Kai-Win Lee (Yale May 1990) "Global Routing of Row-Based Integrated Circuits".
2. Dahe Chen (Yale May 1992) "Mickey: A Graph-Based Macro-Cell Global Router".
3. Mark Chiang (Yale May 1992) "A Perturbation Approach to the Symbolic Analysis of Analog Circuits".
4. William Swartz (Yale May 1993) "Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits".
5. Ted Stanion (Yale May 1994) "Boolean Algorithms for Combinational Synthesis and Test Generation".
6. Kalapi Roy (University of Washington June 1994) "A Timing-Driven Multi-Way Partitioning System for Integrated Circuits and Multi-Chip Systems".
7. Jer-Jaw Hsu (University of Washington December 1994) "Fully Symbolic Analysis of Large Analog Integrated Circuits".
8. Wern-Jieh Sun (University of Washington December 1994) "Effective and Efficient Placement for Very Large Integrated Circuits".
9. Qicheng Yu (University of Washington March 1995) "Approximate Symbolic Analysis of Large Analog Integrated Circuits".
10. Bingzhong David Guan (University of Washington August 1996) "Automatic Layout Generation of Static CMOS Combinational Cells and Blocks".
11. Eugene Liu (University of Washington, December 1997) "Global Routing and Pin Assignment for Multi-layer Chip-level Layout".
12. Hsiao-Ping Tseng (University of Washington, December 1997) "Detailed Routing Algorithms for VLSI Circuits".
13. Gin Yee (University of Washington, June 1999) "Dynamic Logic Design and Synthesis Using Clock-Delayed Domino".
14. Tyler Thorp (University of Washington, December 1999), "Design and Synthesis of Dynamic Circuits".
15. Tatjana Serdar (University of Washington, December 2000), "Automatic Datapath Tile Placement and Routing".
16. Jovanka Ciric (University of Washington, August 2001), "Boolean Matching and Level-Based Technology Mapping".
17. Yi Han (University of Washington, December 2004), "A High-Performance CMOS Programmable Logic Core for System-on-Chip Applications".
18. Hiran Tennakoon (University of Washington, August 2005), "Efficient and Accurate Gate Sizing With Piecewise Convex Delay Models".
19. Miodrag Vujkovic (University of Washington, March 2006), "Efficient Fully-Automated, Refinement-Based Power-Delay Optimization Design Flow for Standard Cell Designs".
20. Kian Hour (Alfred) Chong (University of Washington, June 2006), "Self-Calibrating Differential Output Prediction Logic".
21. Xinyu (Sunny) Guo (University of Washington, June 2006), " A High-Throughput Divider Based on Output Prediction Logic".
22. Sheng Sun (University of Washington, August 2006), "High Performance and Energy Efficient Adder Design".
23. Mohammad Rahman (UT-Dallas, December 2011), "Power and Leakage Minimization for Digital ICs".
24. Chiu-Wei Pan (UT-Dallas, August 2012), "High Speed and Power Efficient Compression of Partial Products".
25. Zhao Wang (UT-Dallas, October 2012), "Accurate Wire Endpoint Delay Estimation".
26. Akshay Sridharan (UT-Dallas, October 2015), "STARK: Synchronous to Asynchronous Redesign Kit".
27. Anitha Yella (UT-Dallas, January 2016), "Power Optimization in ICs".

Current Ph.D. Students
1. Meisam Roshan, Ph.D. expected 08/16
2. Helen Huang, Ph.D. expected 12/16
3. Vahid Moalemi, Ph.D. expected 12/16
4. Jingsheng Tian, Ph.D. expected 06/17
5. Xiangyu Xu, Ph.D. expected 06/17
6. Jiajia Wang, Ph.D. expected 06/18
7. Lubaba Nahar, Ph.D. expected 06/19 (co-advised with JV Rajendran)
8. Thomas Broadfoot, Ph.D. expected 06/19 (co-advised with JV Rajendran)

Teaching Activities

Yr	Qtr	Course	Brief Title, Credits, #students	Stud. Opin. Survey
1992	Aut	EE538	Auto Layout, 4 credits, 20 students	4.38/4.08
1993	Win	EE356	Analog ICs, 4 credits, 55 students	3.21/3.00
1993	Spr	EE535	VLSI Design, 4 credits, 25 students	4.27/4.47
1993	Sum	EE332	Analog ICs, 5 credits, 35 students	3.57/3.48
1993	Aut	EE538	Auto Layout, 4 credits, 15 students	3.60/3.50
1993	Aut	EE332	Analog ICs, 5 credits, 40 students	3.93/3.90
1994	Win	EE433	Analog MOS ICs, 4 credits, 65 students	3.96/4.08
1994	Spr	EE476	Digital ICs, 5 credits, 55 students	3.89/3.89
1994	Aut	EE538	Auto Layout, 4 credits, 15 students	3.63/3.63
1994	Aut	EE433	Analog MOS ICs, 4 credits, 55 students	4.32/4.30
1995	Win	EE476	Digital ICs, 5 credits, 85 students	3.75/3.85
1995	Spr	EE473	Adv. Analog MOS, 5 credits, 45 students	3.53/3.59
1995	Aut	EE476	Digital ICs, 5 credits, 85 students	4.40/4.20
1996	Win	EE535	VLSI Design, 4 credits, 55 students	4.10/4.00
1996	Spr	EE538	Auto Layout, 4 credits, 15 students	4.30/4.50
1996	Aut	EE476	Digital ICs, 5 credits, 125 students	3.40/3.40
1997	Win	EE477	Custom Dig ICs, 4 credits, 45 students	4.30/4.10
1997	Win	EE541	Auto Layout, 4 credits, 20 students	4.70/4.70
1997	Spr	EE535	VLSI Design, 4 credits, 20 students	3.83/4.00
1997	Aut	EE476	Digital ICs, 5 credits, 60 students	3.88/3.89
1998	Win	EE477	Custom Dig ICs, 4 credits, 60 students	3.66/3.61
1998	Spr	EE476	Digital ICs, 5 credits, 60 students	3.39/3.50
1998	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.57/3.94
1998	Aut	EE476	Digital ICs, 5 credits, 35 students	4.15/4.50
1999	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.00/3.94
1999	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.79/4.13
1999	Aut	EE476	Digital ICs, 5 credits, 50 students	4.70/4.70
2000	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.53/4.27
2000	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	4.35/4.44
2000	Aut	EE476	Digital ICs, 5 credits, 125 students	4.20/4.19
2001	Win	EE477	VLSI II, 5 credits, 75 students	4.30/4.37
2001	Win	EE525	VLSI II, 5 credits, 25 students	4.25/4.50
2001	Spr	EE526	VLSI III, 4 credits, 50 students	4.35/4.50
2001	Aut	EE476	VLSI I, 5 credits, 150 students	4.1/4.2
2002	Win	EE477	VLSI II, 5 credits, 75 students	4.1/4.1
2002	Win	EE525	VLSI II, 5 credits, 25 students	4.1/4.1
2002	Spr	EE526	VLSI III, 4 credits, 50 students	3.6/3.3
2002	Aut	EE476	VLSI I, 5 credits, 150 students	3.7/3.6
2003	Win	EE477	VLSI II, 5 credits, 55 students	3.4/3.8

2003	Win	EE525	VLSI II, 5 credits, 25 students	3.6/3.3
2003	Spr	EE526	VLSI III, 4 credits, 32 students	3.3/3.5
2003	Aut	EE476	VLSI I, 5 credits, 30 students	4.5/4.6
2004	Win	EE477	VLSI II, 5 credits, 12 students	3.2/3.7
2004	Win	EE525	VLSI II, 5 credits, 7 students	2.2/2.2
2004	Spr	EE526	VLSI III, 4 credits, 12 students	3.2/3.2
2004	Aut	EE476	VLSI I, 5 credits, 65 students	3.8/3.9
2005	Fall	EE6325	VLSI Design, 3 units, 42 students	4.4/4.6
2006	Spr	EE7325	Advanced VLSI Design, 3 units, 20 students	4.5/4.3
2006	Fall	EE6325	VLSI Design, 3 units, 66 students	4.4/4.2
2007	Spr	EE7325	Advanced VLSI Design, 3 units, 15 students	4.5/4.2
2007	Fall	EE6325	VLSI Design, 3 units, 40 students	4.8/4.6
2008	Spr	EE4325	Introduction to VLSI Design, 40 students	3.5/3.4
2008	Spr	EE7325	Advanced VLSI Design, 3 units, 19 students	4.6/4.4
2008	Sum	EE6325	VLSI Design, 3 units, 36 students	4.0/3.7
2008	Fall	EE6325	VLSI Design, 3 units, 40 students	4.1/4.1
2009	Spr	EE4325	Introduction to VLSI Design, 22 students	4.2/3.9
2009	Spr	EE7325	Advanced VLSI Design, 3 units, 37 students	3.7/3.6
2009	Sum	EE6325	VLSI Design, 3 units, 17 students	4.1/4.0
2009	Fall	EE6325	VLSI Design, 3 units, 67 students	4.3/4.0
2010	Spr	EE4325	Introduction to VLSI Design, 25 students	4.6/4.5
2010	Spr	EE7325	Advanced VLSI Design, 3 units, 35 students	4.4/4.4
2010	Sum	EE6325	VLSI Design, 3 units, 17 students	4.7/4.5
2010	Sum	EE3320	Digital Circuits, 3 units, 17 students	4.1/3.8
2010	Fall	EE6325	VLSI Design, 3 units, 77 students	4.4/4.2
2011	Spr	EE4325	Introduction to VLSI Design, 37 students	4.0/4.1
2011	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.2/4.2
2011	Sum	EE6325	VLSI Design, 3 units, 16 students	4.14
2011	Sum	EE3320	Digital Circuits, 3 units, 26 students	4.13/4.10
2011	Fall	EE6325	VLSI Design, 3 units, 91 students	4.73/4.69
2012	Spr	EE4325	Introduction to VLSI Design, 27 students	4.25/3.83
2012	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.90/4.81
2012	Sum	EE6325	VLSI Design, 3 units, 35 students	4.31/4.46
2012	Sum	EE3311	Electronic Circuits, 3 units, 22 students	3.16/3.62
2012	Fall	EE6325	VLSI Design, 3 units, 144 students	4.74/4.76
2013	Spr	EE6325	VLSI Design, 3 units, 41 students	4.85
2013	Spr	EE4325	Introduction to VLSI Design, 7 students	4.75
2013	Sum	EE7325	Advanced VLSI Design, 3 units, 67 students	4.38
2013	Sum	EE3311	Electronic Circuits, 3 units, 46 students	4.58
2013	Fall	EE6325	VLSI Design, 3 units, 129 students	4.64
2014	Spr	EE4325	Introduction to VLSI Design, 25 students	4.69
2014	Sum	EE7325	Advanced VLSI Design, 3 units, 74 students	4.53
2014	Sum	EE3311	Electronic Circuits, 3 units, 40 students	4.75
2014	Fall	EE6325	VLSI Design, 3 units, 139 students	4.79
2015	Spr	EE4325	Introduction to VLSI Design, 25 students	4.72
2015	Sum	EE7325	Advanced VLSI Design, 3 units, 49 students	4.25
2015	Sum	EE3311	Electronic Circuits, 3 units, 25 students	4.80
2015	Fall	EE6325	VLSI Design, 3 units, 142 students	4.73
2016	Spr	EE4325	Introduction to VLSI Design, 25 students	

Course Development
  U. of Washington: EE 541 Automatic Layout of Integrated Circuits (first offering: Fall 1992)
  U. of Washington: EE 477 Custom Digital CMOS Circuit Design (first offering: Win 1997)

U. of Washington: EE 476 Digital Integrated Circuit Design (first offering: Spr 1994)

Yale University: EE 880 Automatic Layout of Integrated Circuits.
Yale University: EE 877 Introduction to VLSI CAD Tools
Yale University: EE 878 Introduction to VLSI Synthesis
Yale University: EE 988 Analog Integrated Circuits II

Journal Publications

1. Z. Wang, X. He, and C. Sechen, "A New Approach for Gate-Level Delay-Insensitive Asynchronous Logic", *Journal of Circuits, Systems & Signal Processing*, October 2014.
2. Z. Wang, C. Pan, Y. Song, and C. Sechen, "High-Throughput Digital IIR Filter Design", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 2, pp. 15-27, April 2014.
3. C. Pan, Z. Wang and C. Sechen, "High Speed and Power Efficient Compression of Partial Products and Vectors," *Journal of Algorithms and Optimization (JAO)*, Vol. 1, No. 1, pp. 39-54, October 2013.
4. Z. Wang and C. Sechen, "A New Algorithm for Accurate Wire Endpoint Delay Estimation", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 1, pp. 30-43, Jan. 2014.
5. M. Rahman, H. Tennakoon, and C. Sechen, "Library-Based Cell-Size Selection using Extended Logical Effort", *IEEE Trans. on Computer-Aided Design*, July 2013.
6. H. Tennakoon and C. Sechen, "Non-convex Gate Delay Modeling and Delay Optimization," *IEEE Trans. on Computer-Aided Design*, Vol. 27, No. 9, September 2008, pp. 1583-1594.
7. Don Bouldin, Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees, Carl Sechen, and Wayne Dai, "Automated Design of Digital Signal Processing ASICs," *IEEE Circuits and Devices*, vol. 20, n. 4, pp. 17-21, July 2004.
8. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *IEEE Trans. on Computer-Aided Design*, Vol. 22, No. 5, May 2003, pp. 535-544.
9. T. Thorp and C. Sechen, "Design and Synthesis of Dynamic Circuits," *IEEE Transactions on VLSI Systems*, Vol. 11, No. 1, February 2003, pp. 141-149.
10. G. Hoyer, G. Yee and C. Sechen, "Locally-Clocked Pipelines and Dynamic Logic," *IEEE Transactions on VLSI Systems*, Vol. 10, No. 1, February 2002, pp. 58-62.
11. H. P. Tseng, L. Scheffer and C. Sechen, "Timing- and Crosstalk-Driven Area Routing," *IEEE Transactions on Computer Aided Design*, vol. 20, no. 4, pp. 528-544, April 2001.
12. G. Yee and C. Sechen, "Clock-Delayed Domino for Dynamic Circuit Design," *IEEE Transactions on VLSI Systems*, Vol. 8, No. 4, August 2000, pp. 425-431.
13. L. Liu and C. Sechen, "Multi-layer Chip-level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
14. L. Liu and C. Sechen, "Multi-layer Pin Assignment for Macro Cell Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
15. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Router for Standard Cell Circuits using CTM Cells," *IEEE Transactions on Computer Aided Design*, Vol. 18, No. 10, October 1999.
16. W. Sun and C. Sechen, "A Parallel Standard Cell Placement Algorithm," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 11, November 1997, pp. 1342-1357.
17. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 10, October 1997, pp. 1073-1081.
18. Q. Yu and C. Sechen, "Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis," *Int. Journal of Circuit Theory and Applications*, Vol. 24, No. 5, pp. 597-603, 1996.
19. Q. Yu and C. Sechen, "A Unified Approach to the Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 8, pp. 656-669, August 1996.

20. K. Roy and C. Sechen, "A Timing-Driven Partitioning System for Multiple FPGAs," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 309-328, 1996.

21. K. Roy, D. Guan and C. Sechen, "A Sea-of-Gates Style FPGA Placement Algorithm," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 293-307, 1996.

22. T. Stanion, D. Bhattacharya, and C. Sechen, "An Efficient Method for Generating Exhaustive Test Sets," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 12, December 1995.

23. W. Sun and C. Sechen, "Efficient and Effective Placement for Very Large Circuits," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 3, pp. 349-359, March 1995.

24. J. J. Hsu and C. Sechen, "DC Small Signal Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I*, Vol. 41, No. 12, pp. 817-828, December 1994.

25. T. Stanion and C. Sechen, "Boolean Division and Factorization Using Binary Decision Diagrams," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, September 1994, pp. 1179-1184.

26. C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro Cell Integrated Circuits Using Simulated Annealing," *Int. J. Computer-Aided VLSI Design*, vol. 2, no. 2, 1990, pp. 127-158.

27. C. Sechen, D. Braun, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *IEEE J. of Solid State Circuits*, vol. 23, n. 2, pp. 410- 420, April 1988.

28. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *IEEE J. of Solid State Circuits*, vol. 20, n. 2, April 1985, pp. 510-522.

29. C. Sechen, "An Improved Lock Layer Transistor," *Solid State Electronics*, Vol. 21, No. 6, June 1978, pp. 911-913.

30. S. Senturia and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Transactions on Electron Devices*, vol.24, no.9, p.1207, September 1977.

31. S. Senturia, C. Sechen, and J. Wishneusky, "The Charge-Flow Transistor: A New MOS Device," *Applied Physics Letters*, Vol. 30, No. 2, Jan. 1977, p. 106-108.

Fully Refereed Conference Proceedings

1. Meisam Heidarpour Roshan, Kimo Joo, Rajkumar Palwai, Kamran Souri, Will Chen, Carl Arft, Sassan Tabatabaei, Samira Zaliasl, Sudhakar Pamarti, Carl Sechen, Aaron Partridge, Vinod Menon, "Dual-MEMS Resonator Temperature-to-Digital Converter with 39µK Resolution and a FoM of 0.11pJK^{2}", *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2016, San Francisco, CA.

2. M. Jain and C. Sechen, "Chip Design: Matrix Multiplier Based on Systolic Architecture", *IEEE Computer Society 6th International Conference on Computing, Communications and Networking Technologies (ICCCNT)*, July 13-15, 2015, Dallas, TX.

3. Z. Wang, X. He and C. Sechen, "TonyChopper: A Desynchronization Package", *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, Nov. 2-6, 2014, San Jose, CA. (20% accepted)

4. H. Huang and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS", *2014 Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.

5. A. Sridharan and C. Sechen, "Minimum Energy Operation using Robust Asynchronous Logic with Sleep Transistors", *Proc. Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.

6. Yashaswini Prathivadi, Carl Sechen, and Roozbeh Jafari, "A Swarm of Wearable Sensors at the Edge of the Cloud for Robust Activity Recognition", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13)*, Sept. 29, 2013, Montreal, Canada.

7. Mohammad-Mahdi Bidmeshki, Carl Sechen, and Roozbeh Jafari, "Low Power Programmable Architecture for Periodic Activity Monitoring", *Proc. SRC Techcon*, 2013, Austin, TX.

8. Thomas Broadfoot, Jingxiang Tian, HeeEun Choi, Mohammad-Mahdi Bidmeshki, Roozbeh Jafari, and Carl Sechen, "Platform Design for Swarm Wearable Computing", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13)*, Sept. 29, 2013, Montreal, Canada.

9.   A. Sridharan, C. Sechen, and R. Jafari, "Low-Voltage Low-Overhead Asynchronous Logic", accepted: *Int. Symp. on Low Power Electronics and Design (ISLPED)*, Beijing, China, Sept. 4-6, 2013. (25% accepted)

10.   M. M. Bidmeshki, C. Sechen and R. Jafari, "Low Power Programmable Architecture for Periodic Activity Monitoring," *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, 8 March 2013, Round Top, Texas.

11.   Hee-Eun Choi, C. Sechen and R. Jafari, "24kb, 11T Subthreshold SRAM for Ultra-Low Power Medical and Health Monitoring Embedded Systems," *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, 8 March 2013, Round Top, Texas.

12.   M. Rahman, and C. Sechen, "Post-Synthesis Leakage Power Minimization", *Design Automation and Test in Europe (DATE) Conference*, March 12-16, 2012, Dresden, Germany.

13.   M. Rahman, H. Tennakoon, R. Afonso and C. Sechen, "Power Reduction via Separate Synthesis and Physical Libraries", *Proc. Design Automation Conference (DAC)*, June 2011, San Diego, CA.

14.   C. Pan and C. Sechen, "Power Efficient Partial Product Compression", *Proc. Great Lakes Symposium on VLSI*, Lausanne, May 2-4, 2011, Switzerland.

15.   M. Rahman, H. Tennakoon, and C. Sechen, "Power Reduction via Near-Optimal Library-Based Cell-Size Selection", *Design Automation and Test in Europe (DATE) Conference*, March 14-18, 2011, Grenoble, France.

16.   M. Rahman, H. Tennakoon, R. Afonso, and C. Sechen, October 17-18, "Design Automation Tools and Libraries for Low Power Digital Design", *Proc. IEEE Dallas Circuits and Systems Conference (DCAS)*, Oct. 17-18, 2010, Richardson, TX.

17.   M. Rahman, H. Tennakoon, and C. Sechen, "Near Optimal Power Efficiency Through Gate Sizing", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.

18.   H. Huang and C. Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.

19.   E. Kiefer, W. Swartz, and C. Sechen, "Low Power Automated Clock Tree Generation", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.

20.   R. Afonso, M. Rahman, H. Tennakoon, and C. Sechen, "Power Efficient Standard Cell Library Design", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.

21.   C.W. Pan, Y. Song, Z. Wang, and C. Sechen, "DSP Power Reduction through Generalized Carry-Save Arithmetic", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.

22.   R. Afonso, M. Rahman, H. Tennakoon, and C. Sechen, "Power Efficient Standard Cell Library Design", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.

23.   C.W. Pan, Y. Song, Z. Wang, and C. Sechen, "DSP Power Reduction through Generalized Carry-Save Arithmetic", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.

24.   E. Kiefer, W. Swartz, and C. Sechen, "Low Power Automated Clock Tree Generation", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.

25.   H. Huang and C. Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.

26.   S. Sun and C. Sechen, "Post-Layout Comparison of High Performance 64b Static Adders in Energy-Delay Space," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, Lake Tahoe, CA, October 2007.

27.   M. Rahman, H. Tennakoon, and C. Sechen, "Optimal Area-versus-Delay Circuit Sizing Using Extended Logical Effort", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, May 14-15, 2007, Austin, TX.

28.   K. H. Chong, L. McMurchie and C. Sechen, "A 64b Adder Using Self-calibrating Differential Output Prediction Logic," *Proc. Int. Solid-State Circuits Conference (ISSCC)*, February 2006, San Francisco, CA.

29.   J. Zhang, M. Vujkovic, D. Wadkins, and C. Sechen, "Post-Layout Energy-Delay Analysis of Parallel Multipliers," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 2006, Greece.

30.   M. Vujkovic, D. Wadkins and C. Sechen, "Efficient Post-Layout Power-Delay Curve Generation," *Prof. 15th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 21-23 September 2005, Leuven, Belgium. In: *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation*, Series: Lecture Notes in Computer

Science, Vol. 3728 Paliouras, Vassilis; Vounckx, Johan; Verkest, Diederik (Eds.) 2005, XV, 753 p., Softcover ISBN: 3-540-29013-3.

31. X. Guo and C. Sechen, "High Throughput Divider Using Output Prediction Logic," *Proc. PRIME (Ph.D. Research in Microelectronics) Conf., July 25-28, 2005, Lausanne, Switzerland.*

32. X. Guo and C. Sechen, "A High Throughput Divider Implementation," *Proc. Custom Integrated Circuits Conference (CICC)*, 18-21 September 2005, San Jose, CA.

33. H. Tennakoon and C. Sechen, "Efficient and Accurate Gate Sizing with Piecewise Convex Delay Models," *Proc. Design Automation Conference (DAC)*, Anaheim, CA, June 13-17, 2005.

34. S. Sun, Y. Han, X. Guo, K. Chong, L. McMurchie and C. Sechen, "409ps 4.7 FO4 64b Adder Based on Output Prediction Logic in 0.18um CMOS," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.

35. X. Guo and C. Sechen, "High Speed Redundant Adder and Divider in Output Prediction Logic," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.

36. J. Kim, L. McMurchie and C. Sechen, "Mitigation of Single- and Multiple-Cycle-Duration SETs using Double-Mode Redundancy (DMR) in Time", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.

37. J. Lan, D. Lam, L. McMurchie, and C. Sechen, "SEE-Hardened-by-Design Area-Efficient SRAMs", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.

38. Y. Han, L. McMurchie and C. Sechen, "A High Performance CMOS Programmable Logic Core," *Proc. Custom Integrated Circuits Conference (CICC)*, October 3-6, 2004, Orlando, FL.

39. V. Tang, J. Lan, D. Lam, L. McMurchie, and C. Sechen, "High-Performance SEE-Hardened Programmable DSP Array," Proc. 2004 Military and Aerospace Programmable Logic Device (MAPLD) Conference, Washington, DC, Sept. 8-10, 2004.

40. D. Lam, J. Lan, L. McMurchie, and C. Sechen, "Radiation-Hardened-by-Design Area-Efficient SRAMs," Proc. Hardness by Design (HBD) Workshop, Albuquerque, NM, August 24-25, 2004.

41. M. Vujkovic, D. Wadkins, B. Swartz and C. Sechen, "Efficient Timing Closure Without Timing Driven Placement and Routing," *Proc. Design Automation Conference (DAC)*, San Diego, CA, June 7-11, 2004.

42. Y. Lam, L. McMurchie, and C. Sechen, "SEU Hardening of Peripheral Circuitry in Self-Scrubbing SRAMs," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.

43. V. Tang, J. Lan, D. Lam, L. McMurchie and C. Sechen, "Low-Overhead SEE-Hardened Programmable DSP Array," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.

44. L. McMurchie and C. Sechen, "RADAR -- Reconfigurable Analog and Digital Array for Radiation-Hardened Circuits", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 6-13, 2004.

45. Y. Han and C. Sechen, "A Novel High Speed FPGA Architecture, *Proc. SRC Techcon*, Dallas, TX, Aug. 25 – 28, 2003.

46. C. Sechen, "The End of Libraries as We Know Them," *Proc. 40th Design Automation Conference (DAC)*, pp. 642-643, 2003.

47. S. Kio, K. Chong, and C. Sechen, "A Low Power Delayed-Clock Generation and Distribution System," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 25-28, 2003, Bangkok, Thailand.

48. Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees Don Bouldin, Wayne Dai, and Carl Sechen, "MSP Liberator ASIC Design Flow Produces Full Custom Performance Required for Next Generation Military Electronics," *Proc. Government Microelectronics and Applications Conference (GOMAC)*, April 1-3, 2003, Tampa, FL.

49. H. Tennakoon and C. Sechen, "Gate Sizing Using Lagrangian Relaxation Combined with a Fast Gradient-Based Preprocessing Step," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.

50. M. Vujkovic and C. Sechen, "Optimized Power-Delay Curve Generation for Standard Cell ICs," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.

51. L. McMurchie and C. Sechen, "WTA -- Waveform-Based Timing Analysis for Deep Submicron Circuits," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.

52. M. Vujkovic and C. Sechen, "Optimized Power-Delay Curve Generation for Standard Cell ICs," *Proc. Int. Workshop on Logic Synthesis (IWLS)*, June 4-7, 2002, New Orleans, LA.

53.	Yi Han, Larry McMurchie, Jovanka Ciric, and Carl Sechen, "Giga hertz-Speed FPGA Architecture based on Output Prediction Logic", *Tenth ACM/SIGDA International Symposium on Field Programmable Gate Arrays* (FPGA 2002).

54.	J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *Proc. of IEEE Int. Conf. on Comp. Aided Design (ICCAD)*, San Jose, CA, November 5-7, 2001.

55.	R. Rutenbar, M. Baron, T. Daniel, R. Jayaraman, Z. Or-Bach, J. Rose and C. Sechen, "When Will FPGAs Kill ASICs?" *Proc. Design Automation Conference (DAC)*, June 18-22, 2001, Las Vegas, NV.

56.	J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *Proc. of IEEE Int. Workshop on Logic Synthesis*, Lake Tahoe, CA, June 12-15, 2001.

57.	S. Kio, L. McMurchie, and C. Sechen, "Application of Output Prediction Logic to Differential CMOS," *Proc. of IEEE Computer Society Annual Workshop on VLSI*, Orlando, FL, April 19-20, 2001.

58.	S. Sun, L. McMurchie, and C. Sechen, "A High-Performance 64-bit Adder Implemented in Output Prediction Logic," *Proc. 19th Conference on Advanced Research in VLSI*, March 14-16, 2001, Salt Lake City, UT.

59.	T. Serdar and C. Sechen, "Automatic Datapath Tile Placement and Routing," *Proc. of the Design, Automation and Test in Europe (DATE) Conference*, March 13-16, 2001, Munich, Germany.

60.	S. Kio, L. McMurchie, and C. Sechen, "Output Prediction Logic", *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.

61.	M. Vujkovic, G. Yee, and C. Sechen, "Post-Fabrication Automatically Tunable Programmable Delay Elements for Clock-Delayed Domino Logic," *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.

62.	G. Hoyer and C. Sechen, "A Locally-Clocked Dynamic Logic Serial/Parallel Multiplier," *Proc. SRC Techcon*, September 21-23, 2000, Phoenix, AZ.

63.	L. McMurchie, S. Kio, G. Yee, T. Thorp and C. Sechen, "Output Prediction Logic: A High Performance CMOS Design Technique", *Proc. Int. Conf. On Computer Design (ICCD)*, September 17-20, 2000, Austin, TX.

64.	G. Hoyer and C. Sechen, "A Locally-Clocked Dynamic Logic Serial/Parallel Multiplier", *Proc. of Custom Integrated Circuits Conference (CICC)*, May 21-25, 2000, Orlando, FL.

65.	Gin Yee, Ron Christopherson, Tyler Thorp, Ban P. Wong, and Carl Sechen, "An automated shielding algorithm and tool for dynamic circuits," *Proc. Intl. Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 20-22, 2000.

66.	J. Ciric, G. Yee, C. Sechen, "Delay Minimization and Technology Mapping of Two-Level Structures and Implementation Using Clock-Delayed Domino Logic," *Proc. Design Automation & Test in Europe (DATE2000)*, 27-30 March 2000, Paris, France.

67.	T. Serdar and C. Sechen, "AKORD: Transistor Level and Mixed Transistor/Gate Level Placement Tool for Digital Data Paths," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, San Jose, CA, November 1999.

68.	T. Thorp, G. Yee and C. Sechen, "Monotonic Static CMOS and Dual Vt Technology," *Proc. Int. Symp. on Low Power Electronics and Design (ISPLED)*, San Diego, CA, August 16-17, 1999.

69.	T. Thorp, G. Yee and C. Sechen, "Monotonic Logic and Dual Vt Technology", *Proc. of Int. Conf. on Computer Design (ICCD)*, Austin, TX, October 1999.

70.	G. Hoyer, G. Yee and C. Sechen, "SEU Tolerant Locally-Clocked Dynamic Logic, *Proc. Government Microelectronics and Applications Conference (GOMAC)*, March 1999, Monterey, CA.

71.	T. Thorp and C. Sechen, "Domino logic synthesis using complex static gates", *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 9-11, 1998, San Jose, CA.

72.	H. Tennakoon and C. Sechen, "Linear Time Heuristic for Timing Optimization", *Proc. SRC TECH-CON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.

73.	G. Hoyer, G. Yee and C. Sechen, "Locally-clocked Dynamic Logic", *Proc. Midwest Conf. On Circuits and Systems*, Aug. 10-12, 1998, Notre Dame, IN.

74.	J. Ciric and C. Sechen, "Clock-delayed Domino Synthesis Using Decomposition into Two-level Structures", *Proc. SRC TECHCON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.

75.	G. Hoyer and C. Sechen, "Locally-clocked Dynamic Logic", *Proc. SRC TECHCON Conf.*, Sept. 9-11, 1998, Las Vegas, NV.

76.	H. P. Tseng, L. Lin and C. Sechen, "Chip-level Area Routing", *Proc. International Symposium on Physical Design (ISPD)*, April 1998, Monterey, CA.

77. H. P. Tseng, L. Scheffer and C. Sechen, "Timing and Crosstalk Driven Area Routing," *Proc. IEEE Design Automation Conference (DAC)*, June 1998, San Francisco, CA.

78. T. Thorp, G. Yee and C. Sechen, "Dynamic Logic Synthesis using Alternating Dynamic and Static Gates," *Proc. Int. Workshop on Logic Synthesis*, June 1998, Lake Tahoe, CA.

79. G. Yee, R. Chandra, H. Ganesan, and C. Sechen, "Wire Delay in the Presence of Crosstalk," *ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Dec. 4-5, 1997, Austin, Texas.

80. M. Lefebvre, D. Marple and C. Sechen, "The Future of Custom Cell Generation in Physical Synthesis," *Proc. Design Automation Conference (DAC)*, Anaheim, CA, June 1997, pp. 446-451.

81. G. Yee and C. Sechen, "Dynamic Logic Synthesis," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 5-8, 1997, Santa Clara, CA, pp. 345-348.

82. H. P. Tseng and C. Sechen, "Multi-layer Over-the-Cell Routing with Obstacles," *Proc. IEEE Custom Integrated Circuits Conference*, May 5-8, 1997, Santa Clara, CA, pp. 565-568.

83. L. Liu and C. Sechen, "Multi-layer Chip-Level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *Proc. European Design and Test Conference (EDTC)*, March 18-20, 1997, Paris, France.

84. H. P. Tseng and C. Sechen, "A Gridless Multi-layer Router for Standard Cell Circuits Using Central Terminal Model Cells," *Proc. European Design and Test Conference (EDTC)*, March 18-20, 1997, Paris, France.

85. B. Guan and C. Sechen, "Large Standard Cell Libraries and Their Impact on Layout Area and Circuit Performance," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, October 7-9, 1996, Austin, TX.

86. G. Yee and C. Sechen, "Clock-delayed Domino for Adder and Random Logic Design," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, October 7-9, 1996, Austin, TX.

87. B. Guan and C. Sechen, "ASIC Automatic Layout Generation Using Large Standard Cell Libraries," *Proc. International Conference on ASIC (ASICON)*, October 21-24, 1996, Shanghai, China.

88. B. Guan and C. Sechen, "Efficient Standard Cell Generation When Diffusion Strapping Is Required," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 1996, San Diego, CA.

89. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the European Conference on Circuit Theory and Design (ECCTD)*, August 27-31, 1995, Istanbul, Turkey.

90. W. Swartz and C. Sechen, "Timing Driven Placement for Large Circuits," *Proc. 1995 Design Automation Conference (DAC)*, San Francisco, CA, June 1995.

91. T. Stanion and C. Sechen, "A Method for Finding Good Ashenhurst Decompositions and Its Application for FPGA Synthesis," *Proc. 1995 Design Automation Conference (DAC)*, San Francisco, CA, June 1995.

92. B. Guan and C. Sechen, "An Area Minimizing Layout Generator for Random Logic Blocks," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 1-4, 1995, Santa Clara, CA.

93. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *Proc. of the IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 1-3, 1995, Seattle, WA.

94. J. Hsu and C. Sechen, "Simplified Symbolic Pole and Zero Expressions from the Sifting Approach to Symbolic Analysis," *Proc. of the IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 1-3, 1995, Seattle, WA.

95. T. Stanion and C. Sechen, "Quasi-Algebraic Decomposition of Switching Functions," *Proc. 16th Conference on Advanced Research in VLSI*, March 27-29, 1995, Chapel Hill, NC, pp. 358-367.

96. K. Roy and C. Sechen, "Multiple FPGA Partitioning with Performance Optimization," *Proc. of the IEEE/ACM International Symposium on FPGAs*, March 12-14, Monterrey, CA, 1995, pp. 146-152.

97. W. Sun and C. Sechen, "A Loosely Coupled Parallel Algorithm for Standard Cell Placement," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 6-10, 1994, Santa Clara, CA, pp. 137-144.

98. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 6-10, 1994, Santa Clara, CA, pp. 664-671.

99. J. J. Hsu and C. Sechen, "Fully Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Custom Integrated Circuits Conference (CICC)*, May 2-4, 1994, San Diego, CA, pp. 457-460.

100. Q. Yu and C. Sechen, "Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis," *Fourth Great Lakes Symposium on VLSI*, March 4-5, 1994, Notre Dame, IN, pp. 252-255.

101. K. Roy and C. Sechen, "A Timing Driven N-Way Chip and Multi-Chip Partitioner," *Proc. SRC TECH-CON Conference*, September 28-30, 1993, Atlanta, GA.

102. W. Swartz and C. Sechen, "Precise Timing Driven Placement for Large Circuits," *Proc. SRC TECH-CON Conference*, September 28-30, 1993, Atlanta, GA.

103. W. Swartz and C. Sechen, "A New Generalized Row-Based Global Router," *Proc. of the SRC TECH-CON Conference*, September 28-30, 1993, Atlanta, GA.

104. T. Stanion and C. Sechen, "Maximum Projections of Don't Care Conditions in a Boolean Network," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, pp. 674-679.

105. W. Sun and C. Sechen, "Efficient and Effective Placement for Very Large Circuits," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, pp. 170-177.

106. K. Roy and C. Sechen, "A Timing Driven N-Way Chip and Multi-Chip Partitioner," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA, 240- 247.

107. W. Swartz and C. Sechen, "A New Generalized Row-Based Global Router," *IEEE Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 7-11, 1993, Santa Clara, CA. pp. 491- 498.

108. K. Roy, B. Guan and C. Sechen, "A Sea-of-Gates Style FPGA Placement Algorithm," *Int. Conf. on VLSI Design*, January 5-8, 1994, Calcutta, India.

109. J. J. Hsu and C. Sechen, "Low-Frequency Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Custom Integrated Circuits Conference (CICC)*, May 9-12, 1993, San Diego, CA, pp. 14.7.1-14.7.5.

110. T. Stanion and C. Sechen, "Boolean Division and Factorization Using Binary Decision Diagrams," *IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS '92)*, Dec. 8-11, 1992, Sydney, Australia.

111. K. W. Lee and C. Sechen, "A Global Router for Sea-of-Gates Circuits," *Proc. European Design Automation Conference*, Amsterdam, The Netherlands, February 26-28, 1991, pp. 242-247.

112. D. Chen and C. Sechen, "Mickey: A Macro Cell Global Router", *Proc. European Design Automation Conference*, Amsterdam, The Netherlands, February 26-28, 1991, pp. 248- 252.

113. W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells," *Proc. Int. Conf. on Comp. Aided Design (ICCAD)*, Santa Clara, CA, November 11-15, 1990, pp. 336-339.

114. D. Chen and C. Sechen, "Mickey: A New Macro Cell Global Router," *Proc. SRC Techcon Conference*, San Jose, CA, October 16-18, 1990, pp. 241-244.

115. W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells," *Proc. SRC Techcon Conference*, San Jose, CA, October 16-18, 1990, pp. 233-236.

116. K. W. Lee and C. Sechen, "A New Global Router for Sea-of-Gates Circuits," *Proc. 9th Australian Microelectronics Conference*, Adelaide, S. Australia, July 2-4, 1990, pp. 233-244.

117. K. W. Lee and C. Sechen, "A New Global Router for Row-Based Layout," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 7-10, 1988, Santa Clara, CA, pp. 180-183.

118. C. Sechen and D. Chen, "An Improved Objective Function for Mincut Circuit Partitioning," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 7-10, 1988, Santa Clara, CA, pp. 502-505.

119. C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro/Custom Cell Circuits Using Simulated Annealing," *Proc. of the 25th Design Automation Conference (DAC)*, June 1988, Anaheim, CA, pp. 73-80.

120. C. Sechen and K. W. Lee, "An Improved Simulated Annealing Algorithm for Row-Based Placement," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 478-481.

121. C. Sechen, "Average Interconnection Length Estimation for Random and Optimized Placements," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 190-193.

122. J. Burns, A. Casotto, M. Igusa, F. Marron, F. Romeo, A. Sangiovanni-Vincentelli, C. Sechen, H. Shin, G. Srinath, and H. Yaghutiel, "Mosaico: An Integrated Macro-Cell Layout System," in C. Sequin, editor, *Proc. of VLSI '87*, Vancouver, Canada, August, 1987.

123. C. Sechen and A. Sangiovanni-Vincentelli, "TimberWolf3.2: A New Standard Cell Placement and Global Routing Package," *Proc. 23rd Design Automation Conference (DAC)*, June 29-July 2, 1986, Las Vegas, NV, pp. 432-439.

124. D Braun, C. Sechen, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1986, Rochester, NY.

125. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Simulated Annealing Research at Berkeley," *Proc. Int. Conf. on Computer Design (ICCD)*, October 1984, Rye Brook, NY.

126. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1984, Rochester, NY.

127. M. Huberman, S. Senturia, and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Device Research Conference (DRC)*, Cornell University, June 1977.

128. S. Senturia and C. Sechen, "The Charge-Flow Transistor," *IEEE Int. Electron Devices Meeting (IEDM)*, Washington DC, Dec. 1976.

129. L. Liu and C. Sechen, "A Multi-Layer Chip-Level Global Router," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

130. L. Liu and C. Sechen, "Multi-Layer Pin Assignment for Macro Cell Circuits," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

131. G. Yee and C. Sechen, "Clock-Delayed Domino for Adder and Combinatorial Logic Design," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

132. B. Guan and C. Sechen, "Efficient Standard Cell Generation When Diffusion Strapping is Required," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

133. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Channel Router Based on a Combined Constraint Graph and Tile Expansion Approach," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

134. J. J. Hsu and C. Sechen, "The Sifting Approach to Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 211-230.

135. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 241-259.

136. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 261-277.

137. T. Stanion and C. Sechen, "Maximum Projections of Don't Care Conditions in a Boolean Network," *Proc. of the International Workshop on Logic Synthesis*, Lake Tahoe, CA, May 23-26, 1993.

138. W. Sun, K. Roy, and C. Sechen, "Fast, High-Quality Placement for Large Circuits," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.

139. K. Roy, D. Guan and C. Sechen, "FPGA MCM Partitioning and Placement," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.

140. T. Stanion and C. Sechen, "Incremental and Simultaneous Computation of Satisfiability and Observability Don't Cares," *Proc. IEEE/ACM Winter VLSI Workshop*, Jan. 25-27, 1993, Asilomar, CA.

141. R. Weier and C. Sechen, "TimberWolfAR: An Arbitrary Design Rule Multi-Layer Area Router," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.

142. W. Swartz and C. Sechen, "A Generalized Row-Based Global Router for FPGAs," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.

143. K. Roy and C. Sechen, "A Timing Driven N-Way Chip Partitioner," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.

144. K. W. Lee and C. Sechen, "A Global Router for Sea-of-Gates Circuits," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.

145. D. Chen and C. Sechen, "Mickey: A New Macro Cell Global Router", *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.

146. W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.

147. C. Sechen, "TimberWolfSG: A Sea-of-Gates Layout Package," *Proc. of SRC Workshop on Sea-of-Gates Design*, Sept. 22-23, 1988, Berkeley, CA.

148. C. Sechen, "A Global Router for the Sea-of-Gates Environment," *Proc. IFIP Workshop on Physical Design of Sea-of-Gates VLSI*, August 11-12, 1988, Lenggries, Germany.

149. J. Lam, J. M. Delosme, and C. Sechen, "A New Simulated Annealing Schedule for Row-Based Placement," *Proc. IEEE International Workshop on Placement and Routing*, May 10-13, 1988, Research Triangle Park, NC.

150. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Some Theoretical Results on Simulated Annealing and TimberWolf: A Placement and Routing Package for the Layout of Integrated Circuits,"

Proc. Workshop on Statistical Physics in Engineering and Biology, IBM T.J. Watson Research Center, Yorktown Heights, NY, April 1984.

Books Authored

Carl Sechen, **Placement and Global Routing of Integrated Circuits Using Simulated Annealing**, 278 pages, Kluwer Academic Publishers, Boston, MA, 1988.

Patents

C. Sechen, L. McMurchie, G. Yee and T. Thorp, "Output Prediction Logic", #6,549,038 issued March 2003.

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- "Optimal Gate Size and Vt Selection", Texas Instruments, Wireless Division, Jan. – Dec., 2011, $50,000, PI: Carl Sechen.

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- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Low Power HD Video Decoder Research", Texas Instruments, Wireless Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Power Optimization and Circuit Hardening", MARCO Focus Center Research Program (C2S2), $155,000, September 2005 – August 2008.

- "Ultra High Performance Digital Circuit Design and Synthesis", National Science Foundation (NSF), $80,000, (Jan. 2006 – Dec., 2008).

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $80,000, Jan. – Dec., 2008.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2008.

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- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $45,000, Jan. – Dec., 2007.

- "Three-Transistor Memory Cell Research", Carl Sechen, Texas Instruments, $35,000, Jan. – Dec., 2007.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2007.

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $30,000, Sept. – Dec., 2006.

- "DRAM-Density SRAM", Carl Sechen, Honeywell, $105,000, January 2006 – April 2007.

- "RADHARD by Design," DARPA/Boeing, Phase I, $45,000 (co-PI, my portion), November 2004 – August 2005).

- "CLASS: Clockless Logic, Analysis, Synthesis, and Systems," DARPA/Boeing, Phase II/III, $709,000 (co-PI, my portion), (Sept. 2004 – August 2006).

- "MSP Phase 2: Digital IC Optimization Techniques," DARPA/Boeing, $285,000 (co-PI, my portion). (September 2004 – August 2006).

- "Power Optimization and Circuit Hardening," MARCO FCRP C2S2 Center, $100,000, PI (Oct. 04 – Sep. 05).

- "High Speed and Low Power Digital IC Design," NSF ITR, $350,000 (my portion) co-PI, (Sept. 00 – Aug. 05).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $110,000, PI (Sep 04 – Aug 05).

- "High Speed & Low Power Digital Circuit Synthesis and Design," MARCO FCRP C2S2 Center, $100,000, PI (Oct. 03 – Sep. 04), full indirect.

- "CLASS: Clockless Logic, Analysis, Synthesis, and Systems," DARPA/Boeing, Phase I, $135,000 (co-PI, my portion), (Oct. 2003 – May 2004).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $105,000, PI (Sep 03 – Aug 04), full indirect.

- "Low Power Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 03 – Aug 04), no indirect.

- "Reconfigurable RF, Analog and Digital Array for Radiation-Hardened Wireless Communication Circuits," DARPA/SPAWAR, $150,000. PI (April 03 – May 04), full indirect.

- "Development of Pulse-Based Logic," DARPA, $100,000, PI (March 03 – May 04), full indirect.

- "High Performance and Power Efficient Digital IC Optimization Techniques," MSP Phase 1: Boeing/DARPA, $400,000, PI (April 02 – August 03), full indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (May 03 – April 04).

- "High Performance Digital IC Design," MARCO/DARPA C2S2 Center, $170,000, PI (Jan. 01 – Aug. 03), full indirect.

- "Ultra High Performance Digital Circuit Design and Synthesis," National Science Foundation, $180,000, PI, (Sep 02 – Aug 05).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $95,000, PI (Sep 02 – Aug 03), full indirect.

- "PLL Design, Clock Generation and High-Speed/Low-Power DSP-block Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 02 – Aug 03), no indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 02 – Feb 03), no indirect.

- "High Performance Digital IC Design," Semiconductor Research Corporation (SRC), June 1, 2000 – May 31, 2003, $525,000 (full indirect).

- "High Performance Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $60,000 (no indirect), PI (Sep. 00 - Aug. 01).

- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 01 – Feb 02).

- Unrestricted grant, Sun Microsystems, $30,000, PI (Feb 00 – Mar 01).

- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 99 – Sep. 00).

- Unrestricted grant, Cadabra, Inc., $20,000, PI (Feb. 00 – Mar 01).

- "Ultra High Speed Digital Circuit Synthesis and Layout NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000 (no indirect), PI (Sep. 99-Aug. 00).

- "Ultra High Speed Digital Circuit Synthesis and Layout", National Science Foundation, $255,000 (full indirect), PI (Sep 99 – Aug 02).

- "Ultra High Speed Digital Circuit Synthesis and Layout", Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).

- "Ultra High Speed Digital Circuit Synthesis and Layout", , Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).

- "Synthesis of Ultra High Speed Random Logic Blocks", Semiconductor Research Corporation, $132,000, PI (Mar 98-Feb 99).

- "Ultra High Speed Digital Circuit Synthesis and Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $65,000, PI (Sep. 98-Aug. 99).

- "Radiation-hard High Speed Digital Circuit Synthesis", Boeing, $35,000, PI (Sep. 98-Aug. 99).

- "Datapath Cell Layout", Compaq/Digital Equipment, $25,000, PI (Sep. 98 – Aug. 99).

- Unrestricted grant, Sun Microsystems, $8,000, PI (June 99 – May 00).

- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 98 – Sep. 99).

- Unrestricted grant, Sun Microsystems, $30,000, PI (Jan. 99 – Dec. 99).

- Unrestricted grant, TimberWolf Systems, Inc., $20,000, PI (Apr. 98 – Mar. 99).

- Unrestricted grant, Sun Microsystems, Inc., $8,000, PI (June 98 – May 99).

- Various industrial gifts, $65,000, PI (Sep 97-Aug 98).

- "High Speed Digital Circuit Design", NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 97-Aug. 98).

- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 97-Feb 98).

- Various industrial gifts, $112,000, PI (Sep 96-Aug 97).

- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 96-Aug. 97).

- "Symbolic Analysis of Large Analog Circuits", National Science Foundation, $90,000, PI (Sep 94-Aug 97).

- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 96-Feb 97).

- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 95-Aug. 96).

- Various industrial gifts, $117,000, PI (Sep 95-Aug 96).

- "Automatic Layout Research", Semiconductor Research Corporation, $132,000, PI (Mar 95-Feb 96).

- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 94-Aug. 95).

- Various industrial gifts, $208,000, PI (Sep 94-Aug 95).

- "Automatic Layout Research", Semiconductor Research Corporation, $144,000, PI (Mar 94-Feb 95).

- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 93-Aug. 94).

- Various industrial gifts, $343,000, PI (Sep 93-Aug 94).

- "Automatic Layout Research", Semiconductor Research Corporation, $140,000, PI (Mar 93-Feb 94).

- "High Speed Circuit Design and Mixed Signal Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 92-Aug. 93).

- Various industrial gifts, $312,000, PI (Sep 92-Aug 93).

- "Automatic Layout Research", Semiconductor Research Corporation, $140,000, PI (Mar 92-Feb 93).

- Various industrial gifts, $306,000, PI (Sep 91-Aug 92).

- Yale University, Various Industrial Gifts, $1.65 million, PI (1986-1992).

Conference Service Activities

- Elected Chairman for the Placement and Floorplanning sub-committee for the 2004 Design Automation Conference (DAC), 2004.
- Elected to the Placement and Floorplanning sub-committee for the 2003 Design Automation Conference (DAC), 2003.
- Elected Program Chair for the 2000 ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU).
- Elected chairman of the placement and floorplanning committee of the 2001 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 2000 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and routing committee of the 1999 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 1998 Int. Conf. On Computer Aided Design (ICCAD).
- Elected Program Chairman of the ACM Physical Design Workshop, Lake Arrowhead, CA, April 1993.
- Elected Chairman of the 1992 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- Elected Chairman of the 1990 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- CAD Track Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1991.
- Session Chairman for the Design Automation and Test in Europe Conference, 2012-2014.
- Session Chairman for the IEEE Design Automation Conference, 1987, 1990, 1991, 1997.
- Session Chairman for the International Symposium on Physical Design, 1997, 1998.
- Session Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1988, 89, 90, 91, 92.
- Session Chairman for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989, 1990, 1991, 1992, 1993, 1998.

Service as a Referee
- Technical Program Committee for the Design Automation Conference, 2014, 2015.
- Technical Program Committee for the Design Automation and Test in Europe Conference, 2012-2014.
- Technical Program Committee for the IEEE Int. Symposium on VLSI Design, 2010-2011.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989-93, 98.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Design (ICCD), 1987-97.
- Technical Program Committee for the European Design and Test Conference (EDTC), 1995, 96, 97, 98.
- Technical Program Committee for the Design Automation and Test in Europe (DATE) Conference, 1998, 99, 00, 01, 02, 03.
- Technical Program Committee for ACM International Physical Design Workshop, 1996.
- Technical Program committee for the International Symposium on Physical Design, 1997, 98.
- Technical Program Committee for the International Workshop on Layout Synthesis, 1988, 90, 92.
- IEEE/ACM Design Automation Conference, 1986-1998.
- National Science Foundation, 1986-present.
- IEEE Transactions on Computer Aided Design, 1986-present.
- IEEE Transactions on VLSI Systems, 1992-present.
- ACM Transactions on Design Automation of Electronic Systems, 1995-present.

University Service
UTD
Director of ECS Tech Support Services, June 2012 – February 2014

UW

Faculty Council on Research, 1994-1997
Faculty Senate, 2002-2004

Department Service
UTD
Advisory Committee to TxACE (SRC Texas Analog Center of Excellence) 2008-2009
Chair of the Computer Support Committee, EE Dept., 2007-2011
Chair of the Analog Search Sub-Committee, EE Dept., 2007-2008
Faculty Search Committee (computer engineering) 2010-11

UW
Faculty Search Committee, 2005-2006
Group Chair, VLSI and Digital Systems Group, 1997-2005
Faculty Search Committee, 98-99.
Graduate Studies and Research Committee, 1992-93, 96-97, 97-98.
Group Chair, Electronics, 94-95.
Graduate Admissions Committee, Electrical Engineering Dept., 1992-93.
Qualifying Examination Subcommittee, 1992-93.
Computer Resources Committee, 1992-93.

Outside University Service

Selected by the NSF to serve as a panelist for (invited) full proposals submitted to the CISE Expeditions in Computing (Expeditions) program, NSF 08-568, April 6-7, 2010.

Selected by the NSF to serve on the 2008 proposal review panel (April 14-15, 2008) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2009 funding.

Selected by the NSF to serve on the 2007 proposal review panel (January 8-9, 2007) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2008 funding.

Selected by the NSF to serve on the 2005 proposal review panel (October 20-21, 2005) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2006 funding.

Selected by the NSF to serve on the 2004 proposal review panel (May 5-6, 2004) to review a number of proposals that have been submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2004 funding.

Selected by the NSF to serve on the 2002 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Selected by the NSF to serve on the 1999 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Co-Director of the NSF Center for the Design of Analog and Digital ICs (CDADIC), 1997-2005; this center provides about $450,000 annually to the University of Washington.

Professional Society Memberships

Eta Kappa Nu
Tau Beta Pi
Sigma Xi
IEEE Fellow
ACM

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Attorney Docket No.: 635162800300

Certificate of Electronic Filing Under 37 CFR 1.8

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with 37 CFR 1.6(a)(4):

Mail Stop Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on _____July 31, 2016_____
                          Date

_____/Erwin B. Palines/_____
                          Signature

_____Erwin B. Palines_____
Typed or printed name of person signing Certificate

_____   _____
Registration Number, if applicable   (213) 892-5200
                                            Telephone Number

Second Supplemental Declaration of Dr. Carl Sechen
(and accompanying Exhibit AAA)

la-1324993

Electronic Acknowledgement Receipt

EFS ID:	26503425
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	Mehran Arjomand/Erwin Palines
Filer Authorized By:	Mehran Arjomand
Attorney Docket Number:	17730-3
Receipt Date:	01-AUG-2016
Filing Date:	20-OCT-2010
Time Stamp:	02:51:15
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		63516-28003_00_PO_Response _Requesting_to_Reopen_Prose cution_.pdf	168131 4fcfa75919f30f3254cf36f29c52a39c90a566 9b	yes	59

	Multipart Description/PDF files in .zip description			
	Document Description		Start	End
	Patent Owner Response after Board Decision		1	58
	Reexam Certificate of Service		59	59

Warnings:

Information:

			536613		
2	Reexam - Affidavit/Decl/Exhibit Filed by 3rd Party	63516-28003_00_2nd_Supp_Sechen_Dec.pdf	7c50f44d15ce2f887003ea09965eb58518bc72e9	no	38

Warnings:

Information:

Total Files Size (in bytes):	704744

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

I hereby certify that this paper is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: August 1, 2016   Signature: _____/Erwin B. Palines/_____ (Erwin B. Palines)

Via EFS Web
Patent
Docket No. 635162800301

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:	Examiner: Behzad PEIKARI
Jayesh BHAKTA et al.	Group Art Unit: 3992
Control Nos.: 95/001,339; 95/000,578; 95/000,579	Confirmation No.: 5035; 8810; 3547
Appeal No.: 2015-006849	
Filed: June 8, 2010; October 20, 2010; October 21, 2010	
For: MEMORY MODULE DECODER	

RESPONDENT'S COMMENTS TO REQUESTER 1'S REQUEST FOR REHEARING UNDER 37 C.F.R. § 41.79(c)

MS *Inter Partes* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

These Respondent's Comments relate to the May 31, 2016 Decision ("Decision") by the Patent Trial and Appeal Board (the "Board"). In the Decision, the Board affirmed the Examiner's decision to not reject claims 16 and 17 of U.S. Patent No. 7,619,912 (the "'912 Patent") under Grounds 4 and 5 raised by Requester 1 (Inphi for control no. 95/001,339). Requester 1, as Appellant, filed a Request for Rehearing on June 30, 2016 based on alleged errors by the Board.

Pursuant to 37 C.F.R. § 41.79(c), Respondent hereby submits these Comments by August 1, 2016 (the next business day following July 30, 2016) and respectfully submits that the Board did not commit the alleged errors in its Decision. Thus, the Rehearing Request should be denied.

Control No. 95/001,339   Docket No. 635162800301

I.   APPELLANT'S ATTEMPTS TO INTRODUCE NEW ARGUMENTS ARE IMPROPER

Appellant candidly admits that its very "basis for this Request for Rehearing" is to set forth reasoning regarding claims 16 and 17 that it had not previously "elaborated upon" during the reexamination. (Request at 4.) These arguments are improper and foreclosed at this late stage. *See* 37 C.F.R. § 41.79(b)(1) ("Arguments not raised in the briefs before the Board and evidence not previously relied upon in the briefs are not permitted in the request for rehearing . . ."). Moreover, the events of the underlying reexamination make clear that Appellant had multiple opportunities to previously "elaborate upon" this reasoning, but either chose not do so or failed to do so.

In Appellant's request for reexamination, Appellant argued that the claimed feature "wherein the command signal is transmitted to only one DDR memory device at a time" in claim 16 (and its dependent claim 17) should be rejected under § 103 based on Amidi alone or Amidi in combination with Dell 2. (May 7, 2010 Corrected Reexamination Request at 139-140, 173.) Appellant, for example, alleged that Amidi's command signal "could have been transmitted to the DDR memory devices serially in a sequential fashion." (*See, e.g., id.* at 139-140.) After merger, the Examiner labeled the respective § 103 grounds as Grounds 4 and 5, and dismissed Appellant's mere conclusory assertion because it lacked support or any reasoned explanation. (April 4, 2011 Office Action at ¶¶ 61 and 71.) Appellant had the opportunity to respond to the Examiner by supporting its assertions, but chose not to do so. Its follow-on comments did not even mention claims 16 and 17 under these grounds. (August 29, 2011 Requester 1 Comments).

Appellant had a *second* opportunity to respond, after the Examiner issued a second Office Action again rejecting Appellant's "mere conclusory statement." (October 14, 2011 Office Action at ¶¶ 23 and 26.) In response, Appellant argued that Amidi's row and column accesses are "for the purpose of accessing a single memory cell." (February 13, 2012 Requester 1 Comments at 19-20.) Despite requesting (and subsequently being granted) a waiver of the fifty-page limit for response, Appellant devoted essentially one page of arguments that it now seeks to "elaborate upon."

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Control No. 95/001,339   Docket No. 635162800301

Appellant had even a *third* opportunity to present the arguments that it now presents. After the Examiner found in a third Office Action that Appellant's February 2012 analysis still lacked a reasonable explanation, Appellant simply chose not to present any arguments with regards to claims 16 and 17 in its subsequent response. (November 13, 2012 Office Action at ¶ 54; February 13, 2013 Requester 1 Comments).

On Appeal, Appellant just restated its conclusory arguments during the reexamination. (App. Br. at 18-19.) Affirming the Examiner, the Board found that Appellant's analysis was conclusory under Grounds 4 and 5 and sustained the Examiner's decision as to claims 16 and 17. (Decision at 75-77 and 83.)

Now, Appellant attempts to essentially reopen the reexamination on the basis of arguments that have never been presented during the reexamination or on appeal. Appellant claims that it is setting forth reasoning regarding claims 16 and 17 that it had not "elaborated upon" during the reexamination. (Rehearing Req. at 3-4.) But that claim rings hollow given the multiple opportunities afforded to Appellant during the reexamination to elaborate upon its reasoning. At this late stage, Appellant should not be allowed to introduce arguments in a rehearing request under the guise of rectifying a Board mistake.

Moreover, the arguments that Appellant now presents are mere attorney argument that newly proposes a speculative example in which "a RAS signal can be provided to all of the memory devices at the same time, but the CAS signal be provided to only one of the memory devices." (Rehearing Req. at 4-5.) Appellant alleges that this is "further clarification" of the Second Wang Declaration (*id.* at 4), but is unable to cite to any portion of that declaration or anywhere in the record to support its allegation.

Appellant also misstates the record, claiming that the "contentions in the Second Wang Declaration" are "unrebutted." (Rehearing Req. at 5.) Yet, as the Board explained, the very art that Appellant relies upon contravenes the Second Wang Declaration. At least Figures 6A and 6B of Amidi establish "countering evidence in Amidi" against Appellant according to the Board. (Decision at 76.)

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Control No. 95/001,339   Docket No. 635162800301

Appellant further misstates its own expert's testimony in asserting that "Amidi provides RAS and CAS signals to isolate a particular memory <u>device</u> in an array of memory <u>cells</u>." (Rehearing Req. at 4 (emphasis added).) Where Appellant stated "device" then "cells," the expert testimony actually stated "cell" then "devices": "DDR memory devices generally provide some type of RAS and CAS signals to isolate a particular memory <u>cell</u> in an array of memory <u>devices</u>." (2d Wang Decl. at ¶ 13 (emphasis added).) Memory cells are not the same as memory devices, but Appellant confuses the two terms in its Rehearing Request.

Finally, Appellant attempts to argue that "[w]ait time is known to be inserted in order to avoid multiple read commands causing contention." (Rehearing Req. at 6.) This argument is also new and impermissible at this stage.

II.   CONCLUSION

Appellant had ample opportunity to present the arguments that it is now attempting to introduce. Appellant chose not to do so or failed to do so. Therefore, Respondent respectfully submits that Appellant's new arguments should be rejected as improper for failing to "state with particularity the points believed to have been misapprehended or overlooked in rendering the Board's opinion reflecting its decision," as required by § 41.79(b)(1). Indeed, the Board cannot misapprehend or overlook points that it has never previously heard. Accordingly, Appellant's Rehearing Request should be denied, and the Board should continue to maintain its affirmance of the Examiner's decision to not reject claims 16 and 17 under Grounds 4 and 5.

The Respondent authorizes the Commissioner to charge the cost of any petitions or fees due in connection with this filing to **Deposit Account No. 03-1952** referencing docket no. **635162800301**.

Dated: August 1, 2016   Respectfully submitted,

By__/Mehran Arjomand/_____
Mehran Arjomand
    Registration No.: 48,231
MORRISON & FOERSTER LLP
707 Wilshire Boulevard
Los Angeles, California 90017-3543
(213) 892-5630

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la-1324880

Control No. 95/001,339   Docket No. 635162800301

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 1.903, the undersigned, on behalf of Respondent/Patent Owner, hereby certifies that a copy of the following documents:

1.   Respondent's Comments to Requester 1's Request for Rehearing Under 37 C.F.R. § 41.79(c)

was served on the third party requesters via first class mail on the date below. The name and address of the parties served are as follows.

For Requester 95/000,578:

Michael Heafey
King & Spalding, LLP
601 South California Avenue
Palo Alto, CA 94304

For Requester 95/000,579:

Michael Heafey
King & Spalding, LLP
601 South California Avenue
Palo Alto, CA 94304

For Requester 95/001,339:

David A. Jakopin
Pillsbury Winthrop Shaw Pittman LLP
P.O. Box 10500 – Intellectual Property Group
McLean, VA 22102

Date: August 1, 2016   /Mehran Arjomand/
                                           Mehran Arjomand

5

la-1324880

Electronic Acknowledgement Receipt

EFS ID:	26515552
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	Mehran Arjomand/Erwin Palines
Filer Authorized By:	Mehran Arjomand
Attorney Docket Number:	17730-3
Receipt Date:	02-AUG-2016
Filing Date:	20-OCT-2010
Time Stamp:	01:50:57
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		63516-28003_01_Comments_to_Request_for_Rehearing_912_Patent.pdf	34925 ac07040762904319a1b7ddadf4dd0c566072ab85	yes	5

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Patent Owner Comments on Req for Rehearing timely	1	4
Reexam Certificate of Service	5	5

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Information:

Total Files Size (in bytes):	34925

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Control No.: 95/000,578

Filing Date: October 20, 2010

U.S. Patent No.: 7,619,912

Inventor: Jayesh Bhakta, *et al.*

Issued: November 17, 2009

Title: MEMORY MODULE DECODER

Confirmation No.: 8810

Group Art Unit: 3992

Examiner: PEIKARI, BEHZAD

REQUESTER 2'S COMMENTS PURSUANT TO 37 C.F.R. 41.77(c)

Mail Stop Inter Partes Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pursuant to 37 C.F.R. § 41.77(c), Third Party Requester SMART Modular Technologies, Inc. ("Requester 2") timely files this response addressing Patent Owner's Response Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(l) ("Reopen Request") within one month from Patent Owner's service.

TABLE OF CONTENTS

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I.   INTRODUCTION

Claims 1-136 of U.S. Patent No. 7,619,912 were subject to reexamination, and Claims 1-43, 45-50, 52-54, 56-58, 60-63, 67-71, 75, 77-93, 109-111, & 119-136 were pending on appeal. *See* Patent Owner Response/Amendment, Jan. 14, 2013 ("RAN Claims"). On June 18, 2014, the Examiner issued a Right of Appeal Notice ("RAN") rejecting Claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, & 119 and indicated the remaining pending claims as patentable. RAN 1.

The Parties appealed to the PTAB and on June 6, 2016, the PTAB rendered its decision that, in part:

(1)   affirmed the Examiner's rejection of Claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, & 119, Decision 101; and

(2)   reversed the Examiner's decision not to adopt proposed rejections of Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, & 120-136.

Decision 102.

On July 31, 2016, Patent Owner filed a request to reopen examination for the claims rejected under new grounds. In its Reopen Request, Patent Owner amended Claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, & 134-136 ("Reopen Claims"). Patent Owner also submitted a second supplemental declaration of Dr. Carl Sechen, dated July 31, 2016 ("Sechen Decl. III").

Patent Owner's Reopen Request does not overcome the PTAB's conclusions of obviousness. First, Patent Owner's amendments include limitations that were previously submitted and the PTAB, the Examiner, or both, determined that they do not render claims nonobvious. Second, Patent Owner fails to establish how these amendments, alone or in combination, overcome the PTAB's rejections.

II.   THE EXAMINER SHOULD REJECT ALL CLAIMS AS AMENDED

The PTAB's decision is "binding upon the examiner" unless Patent Owner submits new evidence or an amendment "not previously of record" which overcomes the rejection. 37 C.F.R. § 41.77(d); MPEP § 2681. Thus, it is Patent Owner's burden to overcome the PTAB's rejection. Here, Patent Owner's amendments and arguments do not overcome the PTAB's rejections because Patent Owner relies on amendments that were previously determined to not render claims nonobvious, on evidence that is already of record, and on arguments that are unpersuasive.

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A.   The "Amendments" Are Not New

Patent Owner's amendments consist of combinations of up to four additional limitations. These limitations, however, are not new and do not render the claims nonobvious because either the Examiner, the PTAB, or both have already determined that they are obvious. This is true whether the limitations are taken individually or in combination.

1.   PLL Clock Amendment

Patent Owner amended Claims 1, 15, 28 39, 52, 67, 77, 82, & 87 to add the following language, referred to here as the "PLL Clock Amendment":

> wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register.

Reopen Request 48.

The PLL Clock Amendment does not render any of the claims nonobvious in view of Micron and Amidi, which are present in each ground of rejection, because it has already been considered and determined not to confer patentability. Further, Dr. Sechen's new declaration provides no new evidence and the claims would still be obvious.

a.   The PLL Clock Amendment Has Already Been Considered And Found Not To Render The Claims Nonobvious

The PTAB and the Examiner already rejected claims that include the PLL Clock Amendment as obvious in view of Micron and Amidi. For example, the Examiner rejected Claim 57 in view of Micron and Amidi which had the same elements of the PLL Clock Amendment. RAN ¶ 98-99. Specifically, Claim 57 included a limitation that the PLL transmits clock signals to the memory devices, logic element, and the register:

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device and the logic element generates a first number of chip-select signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device.

RAN Claims 27-28.

The PTAB also rejected, and Patent Owner cancelled, Claims 53 and 124 that, although worded differently, expressed the PLL Clock Amendment. Decision 102; Reopen Request 2-3; RAN Claims 25-26, 42. Specifically, the limitation recited, "the phase-lock loop device

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transmitting clock signals **to the plurality of DDR memory devices** and to both **the logic element** and **the register**." RAN Claims 25-26, 42 (emphasis added).

Additionally, with respect to Claims 52, 67, 77, 82, & 87, in view of Amidi and JEDEC, the Examiner agreed with the statement submitted by Requester 2 that "it would have been obvious to use the PLL to synchronize all components of the memory module **including logic devices**." RAN ¶ 166 (emphasis added).

Further, with regard to Claim 54, the Examiner stated that:

> it would have been obvious to one of ordinary skill in the art, having the teachings of Amidi before him at the time the invention was made, to receive buffered clock signals from PLL 606 instead of unbuffered clock signals from the system.

Non-Final Office Action, Nov. 13, 2012, ¶ 40.

Moreover, the PTAB also affirmed the rejection of Claim 7, which recites "a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device **operatively coupled to the plurality of DDR memory devices, the logic element, and the register**." RAN Claims 5-6 (emphasis added); Decision 66. The PTAB elaborated that "we do not find error in the mapping of register 418 in Amidi to the recited 'register' and register 408 to the separately recited 'logic element.'" Decision 18.[1]

b.   Sechen Decl. III Does Not Present New Evidence

The PTAB has already determined that the PLL Clock Amendment did not render claims nonobvious despite having considered the same testimony from Dr. Sechen. Sechen Decl. III ¶¶18-20; Decl. of Dr. Sechen, July 5, 2011 ("Sechen Decl. I"), ¶¶ 51, 55. Specifically, Sechen Decl. III states:

> Such language distinguishes these claims from Amidi, which transmits the PLL clock signal to the register and memory, but not to the CPLD.

Sechen Decl. III ¶ 18. In comparison, Dr. Sechen previously stated:

> [T]he output clock signals from the PLL device are transmitted to the register and to the memory devices, but not to the CPLD.

Sechen Decl. I ¶ 51; *also compare* Sechen Decl. III ¶¶ 19, 20 *with* Sechen Decl. I ¶¶ 51, 55.

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[1] The PTAB and Examiner have already determined that a POSITA would not find a required one-to-one identity between the claimed logic element and Amidi's CPLD or a one-to-one identity between the claimed register and one or more of Amidi's register. Decision 18.

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Further, Dr. Sechen's analysis of Amidi does not reflect proper obviousness analysis because it does not factor in the knowledge of a POSITA. For example, referring to Amidi, Dr. Sechen states:

> The output of PLL 606 is neither directly nor indirectly (e.g., through a clock buffer) transmitted to the CPLD 604. Hence, a POSITA would understand that the output of PLL 606 does not control the operation of CPLD 604.

Sechen Decl. III ¶20. Dr. Sechen's statements only address Amidi's explicit teachings and includes conclusory statements about a POSITA, but Dr. Sechen does not provide any analysis concerning the understanding or knowledge of a POSITA. MPEP § 2141(I), (II)(C), (III) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007)).

c.   Amidi Teaches Providing PLL Clock Signal To The Logic Element

Even if Patent Owner's amendments were new or Patent Owner provided new evidence, the amendments fail to render the claims nonobvious because Amidi discloses a PLL that receives clock signals and relays the clock signals to a register, which includes a logic element, and memory devices. Decl. of Nader Bagherzadeh, Aug. 31, 2016 ("Bagherzadeh Decl. V"), ¶ 5 (citing Amidi ¶ 39, 50, Fig. 6A). Amidi states:

> The PLL 412 is used to generate a zero-delay buffer off of system side input differential clock signals 208 (clk and clk_n). By using a PLL, the system side will not see the loading effect of either 18 differential clock loads or 36 differentials clock loads in the case of stacking memory devices.

Amidi ¶ 39.

In Amidi, the PLL input clock is logically identical to the PLL output clock, with the PLL output clock having improved electrical qualities. Bagherzadeh Decl. V ¶ 5. A POSITA would have known that using the PLL clock for all components of a memory module can provide improved performance because providing the PLL output clock, which is buffered, to all components of the memory module of Amidi's Fig. 6A results in improved synchronization. *Id.* Specifically, a POSITA would know from her studies, for example in UCI EECS Courses 119 (VLSI Design), 112 (Organization of Digital Computers), or 31L (Introduction To Digital Logic Laboratory), that a buffered clock will result in improved synchronization. *Id.* Thus, it would have been obvious to a POSITA having the teachings of Amidi to use PLL output clock signals from PLL instead of the input clock signals from a memory controller to provide clock signals to the CPLD, the memory devices, and the registers to improve synchronization. *Id.*

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2.   **The Register Amendment**

Patent Owner amended Claims 1, 15, 28 39, 52, 67, 77, 82, & 87 to add the following
language, referred to here as the "Register Amendment":

> wherein, the register (i) receives, from the computer system, and (ii) buffers, in
> response to the PLL clock signal, a plurality of row/column address signals and
> the bank address signals, and (iii) transmits the buffered plurality of row/column
> address signals and the buffered bank address signals to the plurality of DDR
> memory devices.

Reopen Request 48.

The Register Amendment does not render any of the claims nonobvious because it has
already been considered and the PTAB and the Examiner have found that this limitation is not
capable of rendering the claims nonobvious.

a.   **The Broadest Reasonable Interpretation Includes Transmission Of
Any Portion Of The Row/Column Address Signal Or Buffered Bank
Address Signal**

In reexaminations, claims should be construed to their broadest reasonable interpretation
in view of the specification. MPEP § 2111. The Register Amendment requires the transmission
of "the buffered plurality of row/column address signals and the buffered bank address signals to
the plurality of DDR memory devices." Reopen Request 48. The broadest reasonable
interpretation of that phrase is that the transmission must include any portion of the row/column
address signals and the buffered bank address signals. Bagherzadeh Decl. V ¶ 6.

b.   **The Register Amendment Is A Combination Of Limitations From
Previously Rejected Claims**

The PTAB and the Examiner have already determined that the Register Amendment does
not render claims nonobvious. RAN 98; Decision 101. For example, the Examiner and the
PTAB rejected Claim 26, which although worded differently, recites elements of the Register
Amendment:

> a phase-lock loop device coupled to the printed circuit board, **the phase-lock loop
> device operatively coupled to** the plurality of DDR memory devices, the logic
> element, and **the register**, wherein the set of input signals comprises **a plurality
> of row/column address signals received and buffered by the register** and **sent
> from the register** to the plurality of DDR memory devices.

RAN Claims 13-14 (emphasis added); Decision 101.

Similarly, the PTAB rejected Claim 25, now cancelled, which recites:

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wherein the set of input signals comprises a plurality of row/column address signals **received and buffered by the register and sent from the register** to the plurality of DDR memory devices."

RAN Claims 13-14 (emphasis added); Decision 102.

Further, the PTAB rejected Claim 129 that recited in part, "wherein **the bank address signals** of the set of input control signals are received by the logic element and **received and buffered by the register, the register transmitting the buffered bank address signals** to the plurality of DDR memory." RAN Claims 43-44 (emphasis added); Decision 102.

c.   Micron And Amidi Teach The Register Amendment

The Register Amendment does not render the claims nonobvious because the references teach this limitation. Micron states that the "DDR SDRAM modules operate in registered mode, where the control, command, and address **input signals are latched in the registers** on the rising clock edge and **sent to the DDR SDRAM devices** on the following rising clock edge (data access is delayed by one clock cycle)." Micron 9 (emphasis added). Micron also discloses that bank address signals (BA0, BA1) and row/column address signals (A0-A12) are provided to the registers (U37, U38) of a memory module, and that an output of a PLL (e.g., U40) is coupled to the registers. Micron Fig. 4, at 6.

Further, Amidi teaches a "register 608" that receives row/column address signals and bank address signal and transmits buffered row/column address signals and bank address signal. Bagherzadeh Decl. V ¶ 7 (citing Amidi ¶ 38, Fig. 6A). Amidi states:

> The register 408 is used to **synchronize the incoming address and control signals with respect to differential clock signals** 208 (clk and clk_n). Also, the register 408 may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out.

Id. (quoting Amidi ¶ 38) (emphasis added). A POSITA would understand that the register's synchronization requires receiving and then transmitting the address and control signals. *Id.*

Amidi also teaches that register 608 receives PLL clock signals (CLK0 and CLK0_N), row/column address signals (Add[n-1:0]), and bank address signals (BA[1:0]), and transmits rAdd[n-1:0] and rBA[1:0] to the memory devices. *Id.* (citing Amidi ¶ 50, Fig. 6A).

3.   The Separate Address Limitation Amendment

Patent Owner amended Claims 1, 15, 28 39, 52, 67, 77, 82, & 87 to add the following language, referred to here as the "Separate Address Amendment":

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> wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element.

Reopen Request, 48.

The Separate Address Amendment fails to render any claims nonobvious because it has already been considered and the PTAB found that this limitation is not capable of rendering the claims nonobvious.

a.   The PTAB Already Considered The Separate Address Amendment

The Separate Address Amendment merely incorporates a limitation from a dependent claim that the PTAB has already rejected. Specifically, the PTAB rejected Claims 92 and 93, which depended from Claims 1 and 39, respectively. Decision 102. Although worded differently, Claims 92 and 93 already disclosed the limitation of the Separate Address Amendment now included in Claims 1 and 39. RAN Claims 40. In the Reopen Request, Patent Owner canceled Claims 92 and 93. Reopen Request 42.

b.   Amidi Teaches The Separate Address Amendment

Amidi discloses at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and that the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element. Specifically, a POSITA would understand from reviewing Fig. 6 and the disclosure of Amidi that it discloses that address signals Add(n), which is separate from Add(n-1:0), and Add(n-1:0) serve as row/column address signals/bits and that address signal Add(n) is provided to the CPLD 604, while address signals Add(n-1:0) are provided to the register 608. Bagherzadeh Decl. V ¶ 8 (citing Amidi ¶ 50, Fig. 6A).

4.   Logic Amendment

Patent Owner amended Claims 1, 15, 28 39, 52, 67, 77, 82, & 87 to add the following language, referred to here as the "Logic Amendment":

> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Reopen Request 49.

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The Logic Amendment fails to render any claims nonobvious because it has already been considered and the PTAB and the Examiner have found that this limitation is not capable of rendering claims nonobvious.

a.   The Broadest Reasonable Interpretation of The Logic Amendment Is Disjunctive

The Logic Amendment requires the generation of CAS or chip select signals in response "at least in part to" four enumerated signals. Reopen Request 49. The broadest reasonable interpretation of that phrase is that the CAS and chip select signals are produced in response to "at least one of" the four enumerated signals. Bagherzadeh Decl. V ¶ 9; MPEP § 2111. Accordingly, the claim is disjunctive and therefore rendered obvious if the CAS or chip select signals are generated in response to **any** of the four enumerated signals.

b.   The PTAB Has Considered The Elements Of The Logic Amendment

In the Reopen Request, Patent Owner added the Logic Amendment which is substantially the same as the rejected limitations of Claim 123 except for the "PLL clock signal element." Claim 123 recited:

> wherein the logic element is responsive at least in part to **a row address bit of the at least one row/column address signal**, **the bank address signals**, and **the at least one chip-select signal** by generating a first number of chip-select signals of the set of output control signals.

RAN Claims 42 (emphasis added). Similarly, the PTAB rejected independent Claim 52, which had nearly identical limitations as rejected Claim 123. Decision 102; RAN Claims 42. Thus, the PTAB has already determined that the first three elements of the Logic Amendment do not render claims nonobvious.

With regard to the "PLL clock signal," the PTAB determined that this limitation does not confer patentability because it rejected Claim 128. Decision 102. Patent Owner cancelled Claim 128, which depended from Claim 1 and recited in part, "the **logic element generates** a first number of chip-select signals of the set of output control signals **in response** at least in part **to clock signals received from the phase-lock loop device**." RAN Claims 43 (emphasis added); Reopen Request 44. Although worded differently, the emphasized language is equivalent to the fourth element, the PLL clock signal, of the enumerated elements of the Logic Amendment. RAN Claims 43; Reopen Claims 2-3.

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The PTAB has also determined that the individual elements of the Logic Amendment do not confer patentability. For example, the PTAB rejected Claim 129, now cancelled. Decision 102; Reopen Request 44. Claim 129 depended from Claim 1 through canceled Claim 128, and recited "the generation of the first number of chip-select signals of the output control signals **by the logic element** is **responsive at least in part to the bank address signals**." RAN Claims 43-44 (emphasis added).

B.   Combinations Of Known Elements With Predictable Results

Patent Owner is attempting to show nonobviousness by adding known elements to its rejected claims. Reopen Request 50-57. As explained above, however, all of the amendments submitted by Patent Owner add limitations that do not individually render the claims nonobvious because either the PTAB or the Examiner, or both, have already considered the limitations to be obvious in view of the prior art and because the prior art references disclose these limitations. *Supra* Section II(A).

Claims consisting of a combination of known prior art elements are obvious if the improvements are no more than the predictable use of prior art elements according to their established functions. MPEP § 2141(I)-(III). Combinations of known elements can be nonobvious in certain circumstances, for example when the combination produces unexpected results. *Id.* Here, the elements were not only known, but have been determined to not individually confer nonobviousness, and Patent Owner has not provided any evidence showing that the combination is unique. In fact, Patent Owner does not argue that the combination of the four new elements establishes nonobviousness, but rather argues that the references do not disclose the individual elements. For the reasons discussed above, however, the PTAB and the Examiner have already determined that the prior art discloses these elements.

C.   The Reopen Claims Are Rendered Obvious Amidi In View Of Dell 2 Under 35 U.S.C. § 103

Patent Owner has not shown that Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 & 132-136 are nonobvious.

As explained above, Patent Owner's amendment have already been determined to not render claims nonobvious and overcome the PTAB's determination of obviousness. *Supra* Sections II(A)-(B). Moreover, Dell 2 also discloses the bank address signals element of the Logic Amendment. A POSITA would understand that Dell's disclosure of "ensuring the correct

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bank is addressed" would require generating the CAS or chip-select argument in response to at least the bank address signal because the logic element would need the bank address signal to ensure the correct bank is addressed. Bagherzadeh Decl. V ¶ (citing Dell 2, 8:29-44).

Nonetheless, Patent Owner argues that its amendments overcome the PTAB's rejection because Amidi does not show that the PLL clock signal is transmitted to the logic element, Amidi's CPLD never receives the bank address signal so Amidi's control signals cannot be generated in response to bank address signals, and it would not be obvious to a POSITA to amend Amidi to satisfy that limitation. Patent Owner's arguments fail because, as explained in Sections II(A)-(B), the prior art discloses all of these limitations and further that they would have been obvious to a POSITA. *Supra* Sections II(A)-(B).

D.   Patent Owner Has Not Shown That The Reopen Claims Are Nonobvious In View of Amidi And Dell 184

Although Claims 52-54, 56, 67-71, 77-79, 82-84 & 87-89 of the '912 Patent stand rejected in view of Amidi and Dell 184, Patent Owner did not provide any individual analysis concerning the patentability of those claims in view of this rejection, but rather relied on its analysis for the rejections under Micron and Amidi. Reopen Request 56. Thus, Patent Owner concedes any arguments it had relating to Dell 184.[2]

Moreover, Patent Owner has failed to show that those claims are nonobvious in view of Micron and Amidi. As explained in Sections II(A)-(B), Patent Owner's arguments fail because the prior art discloses all of these limitations and further that they would have been obvious to a POSITA. *Supra* Sections II(A)-(B).

III.   FEE AUTHORIZATION

Please charge any fees associated with these comments to Deposit Account No. 503732, order number 21584-105002.

IV.   CONCLUSION

For the foregoing reasons, Requester 2 requests that the Examiner reject all pending claims.

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[2] To the extent any of these arguments apply to Dell 184, Requester 3 addressed these arguments in its response filed August 31, 2016, in Reexam Control No. 95/000,579.

Dated: August 31, 2016

                                        Respectfully Submitted,

                                         /s Michael F. Heafey
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PEIKARI, BEHZAD

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

_____

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

_____

DENISE M. POTHIER, *Administrative Patent Judge.*

Order Remanding *Inter Partes* Reexamination
Under 37 C.F.R. § 41.77(d) to the Examiner

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

A.   FINDINGS

1.   On May 31, 2016, the Patent Trial and Appeal Board ("the Board") issued an Opinion ("Opinion" and "Op.") affirming the Examiner's decision to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119 of U.S. Patent 7,619,912 ("the '912 patent") and not to reject claims 16 and 17. The Board reversed the Examiner's decision not to adopt the proposed rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–11, and 120–36 based on (1) Amidi and Dell 2 (Ground 5), (2) Micron and Amidi (Ground 13), (3) Amidi and Dell 184 (Ground 20),[1] and (4) Micron, Amidi, and Olarig (Ground 21). Op. 91–93, 101–02.

2.   The reversal of the Examiner's decision not to adopt the noted proposed rejections of 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–11, and 120–36 resulted in new grounds of rejection of these claims. *See id.* at 78–83, 91–104.

3.   In the Decision, Patent Owner was given two options set forth in 37 C.F.R. § 41.77(b) with respect to the new grounds of rejection: (1) to file a response requesting to reopen prosecution before the Examiner or (2) to request that the proceeding be reheard before the Board upon the same record. *Id.* at 102–03.

4.   On June 27, 2016, the Office granted Patent Owner's petition for an extension of time until July 31, 2016, to request to reopen prosecution pursuant to

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[1] Although not summarized explicitly at the conclusion of the decision (Op. 102), the decision by the Examiner not to adopt the rejection of claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 (Ground 20) was reversed (Op. 91–93). Patent Owner recognized this determination in its Response and has presented arguments related to the reversal. PO Request 56.

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Rule 41.77(b)(1).

    5. Patent Owner filed a response requesting that prosecution be reopened before the Examiner. *See* "PATENT OWNER'S RESPONSE REQUESTING TO REOPEN PROSECUTION PURSUANT TO 37 C.F.R. § 41.77(b)(1)" ("PO Request").

    6. On August 31, 2016, Requesters 1 and 2 filed comments to Patent Owner's Response. *See* "THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) COMMENTS ON PATENT OWNER'S RESPONSE REQUESTING TO REOPEN PROSECUTION PURSUANT TO 37 C.F.R. §41.77(b)(1)" ("Requester 1's Comments") and "REQUESTER'S COMMENTS PURSUANT TO 37 C.F.R. 41.77(c)" ("Requester 2's Comments.")

B.   DISCUSSION

    Pursuant to 37 C.F.R. § 41.77(d), after any patent owner response properly filed under § 41.77(b)(1) and any requester comments properly filed under § 41. 77(c), the proceeding is to be remanded to the Examiner. In its response, Patent Owner submits claim amendments and additional evidence in the form of a Second Supplemental Declaration from Carl Sechen, Ph.D ("2d Supp. Sechen Decl.") PO Request 47. The Patent Owner's Request has been reviewed for compliance with 37 C.F.R. § 41.77(b)(1).

    The Request is **granted** for the following reasons.

    Any patent owner response arising under 37 C.F.R. § 41.77(b)(1) "must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both." Patent Owner requests amending claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and canceling claims 25,

<center>3</center>

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42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30. PO Request 46. Patent Owner's Request with respect to amended claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 is considered compliant with 37 C.F.R. § 41.77(b)(1), as the amendments relate to the claims so rejected.

Patent Owner identifies where the Specification of the '912 patent provides support for the amendments to claims and further asserts that claims are patentable as a result of the amendment. PO Request 47–57. The second supplemental declaration of Dr. Sechen also testifies concerning how the disclosure of the '912 patent supports the amendments and how the amended claims are patentable as the result of the amendments. 2d Supp. Sechen Decl., *cited in* PO Request 48–56.

Accordingly, the proposed amendments to claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and Patent Owner's arguments related these claims are entered for the Examiner's consideration.

Patent Owner's Request with respect to cancelling claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30 is also considered compliant with 37 C.F.R. § 41.77(b)(1). Patent Owner has also amended the dependency of various claims (e.g., claims 43 amended to depend from claim 39 and claim 54 amended to depend from claim 52) that previously depended from one of the claims requested to be canceled (e.g., claims 42 and 53 respectively). PO Request 49–50. As such, the cancellation of these claims does not affect the scope of any pending claim in this proceeding and is consistent with 37 C.F.R. § 41.63.

The amendments to cancel claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30 are entered for the Examiner's consideration.

The proceeding will be remanded to the Examiner for consideration of Patent Owner's Request and Requester 1's and 2's Comments in connection with

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claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–11, 120, 122, 123, 125–27, and 131–36. As set forth in 37 C.F.R. § 41.77(d), after due consideration of those submissions, the Examiner is to issue a determination as to whether the Board's new grounds of rejection as designated in the Opinion have been overcome. Following the Examiner's determination, the proceeding will be returned to the Board together with any comments and reply submitted by Patent Owner or Requester under 37 C.F.R. § 41.77(e) for reconsideration and issuance of a new decision by the Board as provided by 37 C.F.R. § 41.77(f).

C. ORDER

It is

ORDERED that Patent Owner's Request requesting reopening of prosecution before the Examiner is **granted** and the proceeding is hereby remanded to the Examiner to consider claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–11, 120, 122, 123, 125–27, and 131–36 in view of the Patent Owner's Request, Requester 1's and 2's Comments, and the newly-submitted evidence pertaining to the new grounds of rejection presented in the May 31, 2016 Opinion.

GRANTED

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Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

FOR PATENT OWNER:
MEHRAN ARJOMAND
MORRISON & FOERSTER LLP
707 Wilshire Boulevard
Los Angeles, CA 90017-3543

FOR THIRD-PARTY REQUESTER 1 (95/001,339):
DAVID A. JAKOPIN
PILSBURY WINTHROP SHAW PITTMAN LLP
P.O. BOX 10500 – INTELLECTUAL PROPERTY GROUP
MCLEAN, VA 22102

FOR THIRD-PARTY REQUESTER 2 (95/000,578):
MICHAEL HEAFEY
KING & SPAULDING, LLP
601 SOUTH CALIFORNIA AVENUE
PALO ALTO, CA 94304

FOR THIRD-PARTY REQUESTER 3 (95/000,579):
MICHAEL HEAFEY
KING & SPAULDING, LLP
601 SOUTH CALIFORNIA AVENUE
PALO ALTO, CA 94304

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224   7590   05/02/2017
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
05/02/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

_____

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/001,579
Patent No. 7,619,912 B2
Technology Center 3900

_____

DENISE M. POTHIER, *Administrative Patent Judges.*

Order Remanding *Inter Partes* Reexamination
Under 37 C.F.R. § 41.77(d) to the Examiner

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

A.   FINDINGS

1.   On May 31, 2016, the Patent Trial and Appeal Board ("the Board") issued an Opinion ("Opinion" and "Op.") affirming the Examiner's decision to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119 of U.S. Patent 7,619,579 ("the '579 patent") and not to reject claims 16 and 17. The Board reversed the Examiner' decision not to adopt the proposed rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, and (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21). Op. 101–02.

2.   The reversal of the Examiner's decision not to adopt the noted proposed rejections of 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 resulted in new grounds of rejection for these claims. *See id.* at 78–83, 91—104.

3.   In the Decision, Patent Owner was given two options set forth in 37 C.F.R. § 41.77(b) with respect to the new grounds of rejection: (1) to file a response requesting to reopen prosecution before the Examiner or (2) to request that the proceeding be reheard before the Board upon the same record. *Id.* at 102–03.

4.   On June 27, 2016, the Office granted Patent Owner's petition for an extension of time until July 31, 2016 to request to reopen prosecution pursuant to Rule 41.77(b)(1).

5.   On August 1, 2016, Patent Owner filed a response requesting that prosecution be reopened before the Examiner. See "PATENT OWNER'S RESPONSE REQUESTING TO REOPEN PROSECUTION PURSUANT TO 37

2

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

C.F.R. § 41.77(b)(1)"

("PO Request").

    6. On August 31, 2016, Requesters 1– 3 filed comments to Patent Owner's Request. See "THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) COMMENTS ON PATENT OWNER'S RESPONSE REQUESTING TO REOPEN PROSECUTION PURSUANT TO 37 C.F.R. §41.77(b)(1)"[1] ("3PR1 Comments"), "REQUESTER 2'S COMMENTS PURSUANT TO 37 C.F.R. 41.77(c)" ("3PR2 Comments"), and "REQUESTER 3'S COMMENTS PURSUANT TO 37 C.F.R. 41.77(c)" ("3PR3 Comments").

    7. On February 9, 2017, the Office issued an Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner ("Order") granting Patent Owner's Request. The Order remanded the proceeding to:

> the Examiner to consider claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-11, 120, 122, 123, 125-27, and 131-36 in view of the Patent Owner's Request, *Requester 1's and 2's Comments*, and the newly-submitted evidence pertaining to the new grounds of rejection presented in the May 31, 2016 Opinion.

Order 5 (emphasis added).

    8. Requester 3 filed a petition on February 20, 2017, requesting that its timely comments of August 31, 2016 be entered and considered.

    9. On April 7, 2017, the petition was granted.

---

[1] On September 12, 2016, the Office of Patent Legal Administration granted Requester 1's petition to waive the 50-page limit for response under Rule 1.943(b).

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

B.   DISCUSSION

Pursuant to 37 C.F.R. § 41.77(d), after any patent owner response properly filed under § 41.77(b)(1) and any requester comments properly filed under § 41. 77(c), the proceeding is to be remanded to the Examiner. In its response, Patent Owner submits additional evidence in the form of claim amendments and a Second Supplemental Declaration from Carl Sechen, Ph.D. ("2d Supp. Sechen Decl.") PO Request 2. We have reviewed Patent Owner's Request for compliance with 37 C.F.R. § 41.77(b)(1).

The Request is **granted** for the following reasons.

Any patent owner response arising under 37 C.F.R. § 41.77(b)(1) "must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both." Patent Owner requests amending claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and canceling claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–130. PO Request 46. Patent Owner's Request with respect to amended claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 is considered compliant with 37 C.F.R. § 41.77(b)(1), as the amendments relate to the claims so rejected.

Patent Owner identifies where the Specification of the '579 patent provides support for the amendments to claims and further asserts that claims are patentable as a result of the amendment. PO Request 47–57. The second supplemental declaration of Dr. Sechen also testifies concerning how the disclosure of the '579 patent supports the amendments and how the amended claims are patentable as the result of the amendments. 2d Supp. Sechen Decl, *cited in* PO Request 48–56.

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Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

Accordingly, the proposed amendments to claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and Patent Owner's arguments related these claims are entered for the Examiner's consideration.

Patent Owner's Request with respect to cancelling claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30 is also considered compliant with 37 C.F.R. § 41.77(b)(1). Patent Owner has also amended the dependency of various claims (e.g., claims 43 amended to depend from claim 39 and claim 54 amended to depend from claim 52) that previously depended from one of these claims requested to be canceled (e.g., claims 42 and 53). PO Request 49–50. As such, the cancellation of these claims does not affect the scope of any pending claim in this proceeding consistent with 37 C.F.R. § 41.63.

As such, the amendments to cancel claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30 are entered for the Examiner's consideration.

The proceeding will be remanded to the Examiner for consideration of Patent Owner's Request and Requester 1's–3's Comments in connection with claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36. As set forth in 37 C.F.R. § 41.77(d), after due consideration of those submissions, the Examiner is to issue a determination as to whether the Board's new grounds of rejection as designated in the Opinion have been overcome. Following the Examiner's determination, the proceeding will be returned to the Board together with any comments and reply submitted by Patent Owner or Requester under 37 C.F.R. § 41.77(e) for reconsideration and issuance of a new decision by the Board as provided by 37 C.F.R. § 41.77(f).

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

C. ORDER

It is

ORDERED that Patent Owner's Request requesting reopening of
prosecution before the Examiner is **granted** and the proceeding is hereby
remanded to the Examiner to consider claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77,
82, 87, 123, 125, 131, and 134–36 in view of the Patent Owner's Request,
Requester 1's–3's Comments, and the newly-submitted evidence pertaining to the
new grounds of rejection presented in the May 31, 2016 Opinion.

<u>GRANTED</u>

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

FOR PATENT OWNER:

MEHRAN ARJOMAND
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MCLEAN, VA 22102

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PALO ALTO, CA 94304

FOR THIRD-PARTY REQUESTER 3 (95/000,579):

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EXAMINER
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PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
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Patent of NETLIST, INC.
Patent Owner

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Technology Center 3900

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Appeal 2015-006849
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C.F.R. § 41.77(b)(1)"

("PO Request").

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Order 5 (emphasis added).

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3

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

B.   DISCUSSION

Pursuant to 37 C.F.R. § 41.77(d), after any patent owner response properly filed under § 41.77(b)(1) and any requester comments properly filed under § 41. 77(c), the proceeding is to be remanded to the Examiner. In its response, Patent Owner submits additional evidence in the form of claim amendments and a Second Supplemental Declaration from Carl Sechen, Ph.D. ("2d Supp. Sechen Decl.") PO Request 2. We have reviewed Patent Owner's Request for compliance with 37 C.F.R. § 41.77(b)(1).

The Request is **granted** for the following reasons.

Any patent owner response arising under 37 C.F.R. § 41.77(b)(1) "must be either an amendment of the claims so rejected or new evidence relating to the claims so rejected, or both." Patent Owner requests amending claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and canceling claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–130. PO Request 46. Patent Owner's Request with respect to amended claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 is considered compliant with 37 C.F.R. § 41.77(b)(1), as the amendments relate to the claims so rejected.

Patent Owner identifies where the Specification of the '579 patent provides support for the amendments to claims and further asserts that claims are patentable as a result of the amendment. PO Request 47–57. The second supplemental declaration of Dr. Sechen also testifies concerning how the disclosure of the '579 patent supports the amendments and how the amended claims are patentable as the result of the amendments. 2d Supp. Sechen Decl, *cited in* PO Request 48–56.

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Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

Accordingly, the proposed amendments to claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 and Patent Owner's arguments related these claims are entered for the Examiner's consideration.

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As such, the amendments to cancel claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–30 are entered for the Examiner's consideration.

The proceeding will be remanded to the Examiner for consideration of Patent Owner's Request and Requester 1's–3's Comments in connection with claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36. As set forth in 37 C.F.R. § 41.77(d), after due consideration of those submissions, the Examiner is to issue a determination as to whether the Board's new grounds of rejection as designated in the Opinion have been overcome. Following the Examiner's determination, the proceeding will be returned to the Board together with any comments and reply submitted by Patent Owner or Requester under 37 C.F.R. § 41.77(e) for reconsideration and issuance of a new decision by the Board as provided by 37 C.F.R. § 41.77(f).

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Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

C. ORDER

It is

ORDERED that Patent Owner's Request requesting reopening of prosecution before the Examiner is **granted** and the proceeding is hereby remanded to the Examiner to consider claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–36 in view of the Patent Owner's Request, Requester 1's–3's Comments, and the newly-submitted evidence pertaining to the new grounds of rejection presented in the May 31, 2016 Opinion.

<u>GRANTED</u>

Appeal 2015-006849
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,579

FOR PATENT OWNER:

MEHRAN ARJOMAND
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LOS ANGELES, CA 90017-3543

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DAVID A. JAKOPIN
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PALO ALTO, CA 94304

FOR THIRD-PARTY REQUESTER 3 (95/000,579):

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FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440

7

Docket No.: 635162800300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:
Jayesh R. BHAKTA

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Confirmation Nos.: 5035; 8810; 3547

Filed: October 20, 2010; October 21, 2010;   Art Unit: 3992
June 8, 2010

For: MEMORY MODULE DECODER   Examiner: B. Peikari

PATENT OWNER'S PETITION PURSUANT TO 37 C.F.R. § 41.3
TO CORRECT REMAND ORDER

Mail Stop Chief Administrative Patent Judge
Patent Trial and Appeal Board
US Patent and Trademark Office
PO Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Patent Owner Netlist, Inc. ("Patent Owner") respectfully petitions the Chief

Administrative Patent Judge under 37 C.F.R. § 41.3 to have a discrepancy corrected in the

updated Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the

Examiner dated May 2, 2017 ("Updated Remand Order"). This Updated Remand Order instructs

"the Examiner to consider claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and

134-36[.]" (*See* at 6.) This listing of claims, however, is incomplete as the listed claims

correspond only to expressly amended claims. (*Id.* at 4.) Thus, the Examiner is ordered to

consider an incomplete listing of claims. In short, this listing of claims in the Updated Remand

Order appears to be a typographical error.

la-1349769

95/001,339; 95/000,578; 95/000,579   Docket No.: 635162800300

For comparison, the original Order Remanding *Inter Partes* Reexamination Under 37

C.F.R. § 41.77(d) to the Examiner dated February 9, 2017 ("Original Remand Order") instructed

"the Examiner to consider claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-

50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-11, 120, 122, 123, 125-

27, and 131-36[.]" (*See* at 5.) This original listing of claims includes, not only the above

incomplete listing of (only expressly amended) claims, but also other pending claims.

Thus, Patent Owner respectfully requests correction of the above discrepancy in the

listing of claims for the Examiner to consider, such as issuance of a corrected remand order or an

erratum paper by the Patent Trial and Appeal Board.

If the Patent and Trademark Office determines that a fee or any other relief is required,

Patent Owner petitions for any required relief and authorizes the Commissioner to charge the

cost of such petition and/or other fees due in connection with the filing of this document to

Deposit Account No. **03-1952** referencing **635162800300**.

Dated: May 17, 2017   Respectfully submitted,

                                              By   /David S. Kim/
                                              David S. Kim
                                                  Registration No.: 57,143
                                              MORRISON & FOERSTER LLP
                                              707 Wilshire Boulevard
                                              Los Angeles, California 90017
                                              (213) 892-5479

2

95/001,339; 95/000,578; 95/000,579   Docket No.: 635162800300

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 1.903, the undersigned, on behalf of the Patent Owner, hereby certifies that a copy of the following documents:

1.   Patent Owner's Petition Pursuant To 37 C.F.R. § 41.3 To Correct Remand Order was served on the Third Party Requesters via first class mail on the date below. The names and addresses of the parties served are as follows.

For Requester 95/000,578:

Michael Heafey
King & Spalding, LLP
601 South California Avenue
Palo Alto, CA 94304

For Requester 95/000,579:

Michael Heafey
King & Spalding, LLP
601 South California Avenue
Palo Alto, CA 94304

For Requester 95/001,339:

David A. Jakopin
Pillsbury Winthrop Shaw Pittman LLP
P.O. Box 10500 – Intellectual Property Group
McLean, VA 22102

Date: May 17, 2017   /David S. Kim/
                                                 David S. Kim

3

la-1349769

Electronic Patent Application Fee Transmittal

Application Number:	95000578
Filing Date:	20-Oct-2010
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Filer:	David S. Kim/Kristine Obrenovic
Attorney Docket Number:	17730-3

Filed as Large Entity

Filing Fees for   inter partes reexam

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Petitions to the Chief	1405	1	400	400
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		400

Electronic Acknowledgement Receipt

EFS ID:	29242563
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	David S. Kim/Kristine Obrenovic
Filer Authorized By:	David S. Kim
Attorney Docket Number:	17730-3
Receipt Date:	17-MAY-2017
Filing Date:	20-OCT-2010
Time Stamp:	21:51:46
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$400
RAM confirmation Number	051817INTEFSW00007600031952
Deposit Account	031952
Authorized User	Kristine Obrenovic
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	
37 CFR 1.16 (National application filing, search, and examination fees)	
37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		635162800300_Petition.pdf	28702 df35b3219572915703873121b1ecf18b6d5dea2	yes	3

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Petition under Rule 41.3 to Chief Admin Patent Judge		1	2
Reexam Certificate of Service		3	3

Warnings:

Information:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
2	Fee Worksheet (SB06)	fee-info.pdf	29950 15a157572e0875b901775144e0e756e89de240a65	no	2

Warnings:

Information:

Total Files Size (in bytes):	58652

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224 7590 06/05/2017	EXAMINER
MORRISON & FOERSTER, LLP 707 Wilshire Boulevard LOS ANGELES, CA 90017	PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
06/05/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

———————————

BEFORE THE
PATENT TRIAL & APPEAL BOARD

———————————

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.,
Requester 3
v.

NETLIST, INC.,
Patent Owner

———————————

Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and
95/000,579
Patent 7,619,912 B2
Technology Center 3900

———————————

JEFFREY B. ROBERTSON, *Administrative Patent Judge.*

DECISION ON PETITION

Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

This is a Decision granting-in-part "Patent Owner's Petition Pursuant to 37 C.F.R. § 41.3 to Correct Remand Order," filed on May 17, 2017 (present petition). In its petition, Patent Owner requests revision of the "Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner," on May 2, 2017, to correct a discrepancy in the listing of the claim numbers. Petition 1.

FINDINGS

1. On May 31, 2016, the Patent Trial and Appeal Board ("Board") entered a Decision on appeal in this merged *inter partes* reexamination proceeding, which included new grounds of rejection pursuant to 37 C.F.R. § 41.77(b). Decision 78–83, 90–102.

2. Patent Owner filed a request to reopen prosecution pursuant to 37 C.F.R. § 41.77(b)(1) on August 1, 2016, in response to the new grounds of rejection.

3. All three Requesters filed comments pursuant to 37 C.F.R. § 41.77(c) separately on August 31, 2016, in reply to Patent Owner's request to reopen prosecution.

4. On February 9, 2017, an "Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner" was mailed ("Order"), which entered Patent Owner's request to reopen prosecution, and the comments of Requester 1 and Requester 2. Order 3–5.

Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

5. Requester 3 filed a petition to enter its comments on February 20, 2017.

6. A Decision granting the petition was mailed on April 7, 2017.

7. An updated "Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner" was mailed on May 2, 2017, which entered Requester 3's comments.

8. Patent Owner filed the present petition on May 17, 2017.

RELEVANT AUTHORITY

37 C.F.R. § 41.3 states:

(a) Deciding official. Petitions must be addressed to the Chief Administrative Patent Judge. A panel or an administrative patent judge may certify a question of policy to the Chief Administrative Patent Judge for decision. The Chief Administrative Patent Judge may delegate authority to decide petitions.

(b) Scope. This section covers petitions on matters pending before the Board (§§ 41.35, 41.64, 41.103, and 41.205); otherwise, see §§ 1.181 to 1.183 of this title. The following matters are not subject to petition:

(1) Issues committed by statute to a panel, and

(2) In pending contested cases, procedural issues. *See* § 41.121(a)(3) and § 41.125(c).

(c) Petition fee. The fee set in § 41.20(a) must accompany any petition under this section except no fee is required for a petition under this section seeking supervisory review.

(d) Effect on proceeding. The filing of a petition does not stay the time for any other action in a Board proceeding.

(e) Time for action.

(1) Except as otherwise provided in this part or as the Board may authorize in writing, a party may:

(i) File the petition within 14 days from the date of the action from which the party is requesting relief, and

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Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

> (ii) File any request for reconsideration of a petition decision within 14 days of the decision on petition or such other time as the Board may set.
> (2) A party may not file an opposition or a reply to a petition without Board authorization.

37 C.F.R. § 41.77(d) states:

> Following any response by the owner under paragraph (b)(1) of this section and any written comments from a requester under paragraph (c) of this section, the proceeding will be remanded to the examiner. The statement of the Board shall be binding upon the examiner unless an amendment or new evidence not previously of record is made which, in the opinion of the examiner, overcomes the new ground of rejection stated in the decision. The examiner will consider any owner response under paragraph (b)(1) of this section and any written comments by a requester under paragraph (c) of this section and issue a determination that the rejection is maintained or has been overcome.

ANALYSIS

In its petition, Patent Owner requests revision of the "Order Remanding *Inter Partes* Reexamination Under 37 C.F.R. § 41.77(d) to the Examiner," of May 2, 2017, to correct a discrepancy in the listing of the claim numbers. Petition 1. Patent Owner asserts that the Board's Order only instructs the examiner to consider the expressly amended claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–136, which is an incomplete listing of claims. *Id.* Patent Owner indicates that the previous Order had instructed the examiner to consider claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67,

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Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and
95/000,579
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69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127,
and 131–136. *Id.* at 2.

In the Decision of May 31, 2016, the Board reversed the Examiner's
decision not to adopt the proposed rejections of claims 1, 3, 4, 6, 8, 10–15,
18–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–
71, 75, 77–93, 109–111, and 120–136 based on (1) Amidi and Dell 2, (2)
Micron and Amidi, and (3) Micron, Amidi, and Olarig (Grounds 5, 13, and
21). Dec. 101–02. The reversal of the Examiner's decision not to adopt the
proposed rejections of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 25, 27–29,
31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111,
and 120–136 resulted in new grounds of rejection for these claims. *Id.* at
78–83, 91–104. To the extent that clarification of the record may be
necessary, it is hereby clarified that the Board's new grounds of rejection of
these claims are before the examiner for consideration under 37 C.F.R.
§ 41.77(d) in view of:

(1) "PATENT OWNER'S RESPONSE REQUESTING TO
REOPEN PROSECUTION PURSUANT TO 37 C.F.R.
§ 41.77(b)(1)," of August 1, 2016, which includes a proposed
amendment;

(2) "THIRD PARTY REQUESTER INPHI CORP.'S
(REQUESTER 1'S) COMMENTS ON PATENT OWNER'S
REPSPONSE REQUESTING TO REOPEN PROSECUTION
PURSUANT TO 37 C.F.R. § 41.77(b)(1)," filed on August 31, 2016;

(3) "REQUESTER 2'S COMMENTS PURSUANT TO
37 C.F.R. § 41.77(c)," filed on August 31, 2016; and

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Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and
95/000,579
Patent 7,619,912 B2

(4) "REQUESTER 3'S COMMENTS PURSUANT TO

37 C.F.R. § 41.77(c)," filed on August 31, 2016.

The petition is granted to the extent that the record is clarified, but the

request for a new Order remanding to the examiner or *erratum* is denied.

Accordingly, the petition is **granted-in-part**.

DECISION

In view of the foregoing, the petition is GRANTED-IN-PART.

FOR PATENT OWNER:
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David S. Kim
Morrison & Foerster, LLP
707 Wilshire Boulevard
Los Angeles, CA 90017

FOR THIRD-PARTY REQUESTERS:

For Requester 95/000,578
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601 South California Avenue
Palo Alto, CA 94304

For Requester 95/000,579
Michael F. Heafey
King & Spalding, LLP
601 South California Avenue
Palo Alto, CA 94304

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Appeal No. 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and
95/000,579
Patent 7,619,912 B2

<u>For Requester 95/001,339</u>
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P.O. Box 10500- Intellectual Property Group
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95|000,578 + 95/001,339

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,579	10/21/2010	7619912	19473-0099RX1	3547

25224   7590   10/03/2017
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
10/03/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Transmittal of Communication to Third Party Requester *Inter Partes* Reexamination	Control No. ~~95/000,579~~ *t95/001,339 t95/000,578*	Patent Under Reexamination 7619912	
	Examiner B. JAMES PEIKARI	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

┌─── (THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS) ───┐

OCT 0 3 2017

TROUTMAN/GOOGLE
ATTN: PATENTS
600 PEACHTREE STREET
SUITE 5200
ATLANTA, GA 30308

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination prceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it <u>cannot</u> be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

U.S. Patent and Trademark Office
PTOL-2070 (Rev. 07-04)

Paper No. 20170926

Application/Control Numbers:
95/000,578 *95/000,579* +*95/001,339*   Page 2
Art Unit: 3992

DETERMINATION UNDER 37 CFR §41.77(d)

This is an inter partes reexamination of U.S. Patent No. 7,619,912 ('912 patent),

issued November 17, 2009.

Three reexamination proceedings, 95/000,578 (*inter partes*), 95/000,579 (*inter

partes*) and 95/001,339 (*inter partes*), each directed to the '912 patent, were merged

into a single reexamination proceeding (see Decision Merging Proceedings, mailed

February 28, 2011).

Claims 1-43, 45-50, 52-54, 56-58, 60-63, 67-71, 75, 77-93, 109-111 and 119-136

remain pending in this reopened, merged reexamination proceeding.

Timeline

The following is a brief timeline of this *inter partes* reexamination proceeding:

- On June 8, 2010, a third party requester ("Requester 1") filed a request for
  inter partes reexamination of claims 1-51 of the '912 patent. The request
  was assigned the serial number 95/001,339 ('1339 Request).

- On September 1, 2010, the Examiner issued an Order granting the
  reexamination of claims 1-51. On the same day, the Examiner also issued
  an Action Closing Prosecution ("ACP"), in which the Examiner did not
  adopt any of the proposed rejections and confirmed all claims over the
  prior art references applied in the proposed rejections.

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95/000,578   Page 3
Art Unit: 3992

- On October 20, 2010, a second third party requester ("Requester 2") filed a request for reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45 and 50. The request was assigned the control number 95/000,578 ('578 Request).

- On October 21, 2010, yet another third party requester ("Requester 3") filed a request for reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45 and 50. The request was assigned the control number 95/000,579 ('579 Request).

- On January 14, 2011, an Order was mailed, granting the reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45 and 50, requested by Requester 3.

- On January 18, 2011, an Order was mailed, granting the reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45 and 50, requested by Requester 2.

- On February 28, 2011, the three *inter partes* reexamination proceedings ('1339, '578, and '579 proceedings) were merged.

- On April 4, 2011, the Examiner issued a non-final Office Action, rejecting claims 1-20 and 22-51, in the merged proceeding. Claim 21 was confirmed.

- On July 5, 2011, Patent Owner timely filed a response adding new claims 52-118.

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- On August 29, 2011, Requesters 1, 2 and 3 filed comments proposing new rejections of newly added claims.

- On October 14, 2011, the Examiner issued a non-final Office Action confirming claims 2, 5, 8, 9, 16, 17, 21, 23, 30, 50, 51, 54-60, 66 and 72-74 and rejecting claims 1, 3, 4, 6, 7, 10-15, 18-20, 22, 24-29, 31-49, 52, 53, 61-65, 67-71 and 75-118. The Office Action was made non-final because it contained new rejections (under Grounds 6, 12 and 13) of unamended claims.

- On January 14, 2012, Patent Owner filed a response amending claims 1, 2, 5, 7, 9, 15, 16, 21, 23, 26, 28, 30, 33, 39, 44, 51, 52, 57, 67, 72, 77, 82, 87, 92 and 93, cancelling claims 64-66, 94-108 and 112-118 and adding claims 119-136. Original independent claims were amended to recite the subject matter of claim 66, which had been previously confirmed.

- On February 13, 2012, Requester 1 filed comments.

- On February 23, 2012, Requester 3 filed comments.

- On March 30, 2012, Requester 2 filed comments.

- On November 13, 2012, the Examiner issued a non-final Office Action, rejecting claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 44, 51-55, 57, 59, 67-74, 77-79, 82-84, 87-89 and 119, in the merged proceeding. Claims 1, 3, 4, 6, 8,10-20, 22, 24, 25, 27-29, 31, 32, 34- 43, 45-50, 56, 58, 60-63, 75-76, 80, 81, 85, 86, 90-93,109-111 and 120-136 were confirmed.

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- On January 14, 2013, Patent Owner filed a response amending claims 52,
  67, 77, 82 and 87 and cancelling claims 44, 51, 55, 59, 72-74 and 76.

- On February 13, 2013, Requesters 1 and 3 filed comments.

- On August 14, 2013, Requester 2 filed comments.

- On March 21, 2014, the Examiner issued an Action Closing Prosecution
  (ACP) rejecting claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119, in the
  merged proceeding. Claims 1, 3, 4, 6, 8, 10-20, 22, 24, 25, 27-29, 31, 32,
  34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111 and 120-
  136 were confirmed.

- On June 18, 2014, the Examiner issued a Right of Appeal Notice (RAN)
  rejecting claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119, in the merged
  proceeding. Claims 1, 3, 4, 6, 8, 10-20, 22, 24, 25, 27-29, 31, 32, 34-43,
  45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111 and 120-136 were
  confirmed.

- On September 16, 2014, Requester 2 filed an appeal brief.

- On September 30, 2014, Requester 1 filed an appeal brief.

- On September 30, 2014, Requester 3 filed an appeal brief.

- On October 1, 2014, Patent Owner filed a cross appeal brief.

- On October 17, 2014, Patent owner filed a respondent brief to the appeal
  brief filed by requester 2.

- On October 30, 2014, Requester 1 filed a respondent brief to patent
  owner's cross appeal brief.

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- On October 30, 2014, Requester 2 filed a respondent brief to patent owner's cross appeal brief.

- On October 30, 2014, Requester 3 filed a respondent brief to patent owner's cross appeal brief.

- On October 31, 2014, Patent owner filed a respondent brief to the appeal brief filed by requester 1.

- On October 31, 2014, Patent owner filed a respondent brief to the appeal brief filed by requester 3.

- On January 14, 2015, the Examiner issued an Examiner's Answer, rejecting claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119, in the merged proceeding. Claims 1, 3, 4, 6, 8, 10-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111 and 120-136 were confirmed.

- On February 9, 2015, Requester 2 filed a rebuttal brief.

- On February 17, 2015, Requester 1 filed a rebuttal brief.

- On February 17, 2015, Requester 3 filed a rebuttal brief.

- On February 18, 2015, Patent Owner filed a rebuttal brief.

- On May 31, 2016, the Patent Trial and Appeal Board ("PTAB" or "Board") issued a decision as follows:

  "We affirm the Examiner's decision to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119.
  We affirm the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18-20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39-43, and 46 based on Amidi under § 102, (2) claims 1, 3, 4, 6, 10-20, 24, 25, 27-29,

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31, 32, 34, 36-43, 45^18, 50, 52-54, 56, 58, 67-71, 75, 77-89, 92, 93, 120-126, 128-130, 132, 133, and 135 based on Amidi under § 103,(3) claims 56, 60-63,90,91, 109-111, 127, and 131 based on Amidi and JEDEC under § 103, (4) claims 16 and 17 based on Amidi and Dell 2, and (5) claims 58, 60, 68, 79, 84, 89-91, 128-131 under § 112,11 as lacking written description support.

We reverse the Examiner's decision not to adopt the rejections of claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 3A43, 45-50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 based on (1) Amidi and Dell 2, (2) Micron and Amidi, or (3) Micron, Amidi, and Olarig (Grounds 5, 13, and 21), designating our reversal as new grounds of rejection under 37 C.F.R. § 41.77(b).

We do not reach the propriety of the remaining adopted or proposed rejections."

The decision by the Examiner not to adopt the rejection of claims

52-54, 56, 67-71, 77-79, 82-84, and 87-89 (Ground 20) was also reversed

(Opinion, pages 91-93).

- On August 1, 2016, Patent Owner filed a request to reopen prosecution,

  amending independent claims 1, 15, 28, 39, 52, 67, 77, 82 and 87 and

  dependent claims 43, 54, 58, 123, 125,131 and 134-136 and canceling

  claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124 and 128-130.

- On August 31, 2016, Requesters 1, 2 and 3 filed comments directed to

  patent owner's request to reopen prosecution.

- On February 9, 2017, the Office issued an Order remanding the

  proceeding to the examiner ("Remand 1").

- On May 2, 2017, the Office issued a second Order remanding the

  proceeding to the examiner ("Remand 2").

Application/Control Numbers:
95/000,578
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- On June 5, 2017, the Office issued a decision on a petition, clarifying the

  second Order remanding the proceeding to the examiner ("Clarified

  Remand").

Considerations

References

The references discussed herein are as follows:

(1)   U.S. Patent Application Publication No. 2006.0117152 ("Amidi")

(2)   U.S. Patent No. 6,209,074 ("Dell 2")

(3)   Micron, *DDR SDRAM RDIMM*, MT36VDDF12872 & MT36VDDF28672 Data Sheet © 2002, ("Micron")

(4)   U.S. Patent No. 6,446,184 ("Dell 184")

(5)   U.S. Patent No. 6,260,127 ("Olarig")

(6)   *Design Specification for PC2100 and PC1600 DDR SDRAM Registered DIMM*, JEDEC Standard No. 21-C, Revision 1.3, Release 11b, January 2002, ("JEDEC 21C");

Parties filing Comments

- Patent Owner of U.S. Patent No. 7,619,912

- Requester 1 – Inphi Corporation (95/001,339)

- Requester 2 – SMART Modular Technologies Inc. (95/000,578)

- Requester 3 – Google Inc. (95/000,579)

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On May 31, 2016, the PTAB issued an Opinion affirming the Examiner's decision

to reject claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119 of U.S. Patent 7,619,912 ("the

'912 patent") and not to reject claims 16 and 17.

The Board reversed the Examiner's decision not to adopt the proposed rejections

of claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 52-54, 56,

58, 60-63, 67-71, 75, 77-93, 109-111 and 120-136 based on (1) Amidi and Dell 2

(Ground 5), (2) Micron and Amidi (Ground 13), (3) Amidi and Dell 184 (Ground 20),

and (4) Micron, Amidi and Olarig (Ground 21). See Remand 1, page 2.

The Board's new grounds of rejection of these claims are before the examiner for

consideration under 37 C.F.R. § 41.77(d) in view of:

(1)   "PATENT OWNER'S RESPONSE REQUESTING TO REOPEN

PROSECUTION PURSUANT TO 37 C.F.R. § 41.77(b)(1)," of August 1, 2016,

which includes a proposed amendment;

(2)   "THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S)

COMMENTS ON PATENT OWNER'S REPSPONSE REQUESTING TO

REOPEN PROSECUTION PURSUANT TO 37 C.F.R. § 41.77(b)(1)," filed on

August 31, 2016;

(3)   "REQUESTER 2'S COMMENTS PURSUANT TO 37 C.F.R. §

41.77(c)," filed on August 31, 2016; and

(4) "REQUESTER 3'S COMMENTS PURSUANT TO 37 C.F.R. §

41.77(c)," filed on August 31, 2016.

See Clarified Remand, pages 5-6.

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New evidence to be considered further includes the Second Supplemental

Declaration of Dr. Carl Sechen, submitted by patent owner on August 1, 2016 ("Sechen

declaration"), the Fourth Declaration of David Wang Ph.D., submitted by Requester 1 on

August 31, 2016 ("Wang declaration") and the Declaration of Nader Bagherzadeh

submitted by Requester 2 on August 31, 2016 ("Bagherzadeh declaration"). The

comments also include direct or indirect reference to earlier declarations by Sechen,

Bagherzadeh, Wang and Kozyrakis. These earlier declarations have been considered

by the examiner and were referenced as necessary in preparing this determination.

The amendment of August 1, 2016 cancelled claims 25, 42, 53, 68, 79, 84, 89,

92, 93, 121, 124, 128-130.

Thus, the remaining claims to be considered in view of the new grounds of

rejection are 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-

127 and 131-136.

Consequently, the specific rejections to be considered are as follows:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 2 (Ground 5).

(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45,

50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120,

122, 123, 125-127 and 131-136 in view of Micron and Amidi (Ground 13).

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell

184 (Ground 20).

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(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Micron, Amidi and

Olarig (Ground 21).

It is the examiner's determination that the following rejections set forth by the

PTAB should be maintained:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 2.

(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45,

50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120,

122, 123, 125-127 and 131-136 in view of Micron and Amidi.

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell

184.

(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Micron, Amidi and

Olarig.

Further, it is the examiner's determination that the PTAB's decision to reject the

claims should be maintained because the prior art cited by Requester 1 renders the

claims unpatentable as set forth in the proposed rejections by Requester 1 in comments

under 41.77(c):

(5)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-

127 and 131-136 in view of Amidi, Dell 2 and JEDEC 21-C.

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Evaluation of Amendments and Evidence

The PTAB has asked the examiner to consider the new grounds of rejection in

view of the amendment and in view of the evidence provided by patent owner and the

third party requesters.

Patent owner's comments are directed amendments that have been made to the

claims for the purpose of overcoming the new grounds of rejection. Patent owner notes,

in particular the "Phase-Lock Loop (PLL) Device" limitation, the "Register" limitation and

the "Logic Element" limitation. Note page 47 of patent owner's comments submitted

August 1, 2016.

The following analysis will first take into account the comments from patent

owner and the third party requesters with respect to each of these limitations:

(1)   The "Phase-lock loop (PLL) circuit" limitation

Patent owner has added the following language to the independent claims:

"wherein, in response to signals received from the computer system, the phase-
lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory
devices, the logic element, and the register"

Patent owner argues that Amidi's design lacks the claimed connectivity,

specifically the PLL device transmitting to the CPLD:

"First, the claim amendments now require: in response to signals received from
the computer system, the phase-lock loop (PLL) device transmit a PLL clock to the
plurality of DDR memory devices, the logic element, and the register. Amidi transmits a
PLL clock signal to the register and memory, but not to the CPLD. Thus, Amidi does not
disclose the PLL device transmitting the PLL clock to the *logic element*, the output of

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PLL 606 is neither directly nor indirectly transmitted to the CPLD 604." (*Patent owner's comments, pages 51-52*)

Note also the Sechen declaration, ¶¶ 18-20.

It appears, however, that much of patent owner's arguments are framed as if addressing an anticipation rejection, rather than a question of obviousness. For reasons discussed below, the examiner does not agree that such connectivity in Amidi is unobvious.

Requester 1 makes the case that in Amidi, Figures 6A and 6B, the phase-lock loop (PLL) 606 receives clock signals CLK0 and CLK0_N from the module connector 602. Furthermore, those same clock signals are provided to the CPLD 604 (which teaches the claimed logic element, as discussed below). Because of this, it would have been obvious to one of ordinary skill in the art at the time the invention was made to either provide the CLK0 and CLK0_N signals from the module connector directly to the CPLD 604 (as described in Amidi) or to provide the CLK0 and CLK0_N signals from the PLL 606 to the CPLD 604 (as in the amended claims), depending on the needs and specific requirements of the circuit in which the Amidi system is being used. This argument is convincing.

Requesters 2 and 3 also present technical arguments, relying on support from the Bagherzadeh declaration and Kozyrakis declarations, arguing that it would have been obvious to send clock signals from the PLL of Amidi instead of from the memory controller. For example, Requester 2 states:

"it would have been obvious to POSITA having the teachings of Amidi to use PLL output clock signals from the PLL instead of the input clock signals from a memory

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controller to provide clock signals to the CPLD, the memory devices, and the registers
to improve synchronization." (*Requester 2's comments, page 4*)

For the reasons given above from Requester 1, and supported by the arguments of

Requesters 2 and 3, the examiner agrees with this statement.

Perhaps even more convincingly, Requesters 2 and 3 note that in the present

reexamination proceeding, the PTAB has already decided that the combination of

Micron and Amidi demonstrated the obviousness of "in response to signals received

from the computer system, the phase-lock loop (PLL) device transmits a PLL clock

signal to the plurality of DDR memory devices, the logic element, and the register" in

claims that were designated as obvious in the Opinion of May 31, 2016.

For example:

Claim 57 - a phase-lock loop device mounted to the printed circuit board, the
phase-lock loop device operatively coupled to the plurality of DDR memory devices, the
logic element, and the register, wherein operation of the register is responsive at least in
part to clock signals received from the phase-lock loop device and the logic element
generates a first number of chip-select signals of the set of output control signals in
response at least in part to clock signals received from the phase-lock loop device.

Claim 53 – the phase-lock loop device transmitting clock signals to the plurality of
DDR memory devices and to both the logic element and the register.

Consequently, the phase-lock loop (PLL) device limitation is not deemed to

distinguish the amended claims, especially since it would have been obvious to one of

ordinary skill in the art to modify Amidi to transmit buffered clock signals from PLL 606

instead of unbuffered clock signals from the system.

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(2)   The "Register" limitation

Patent owner has added the following language to the independent claims:

"wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices."

Patent owner argues:

"As amended, the claims require that ... *the register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices ... Amidi does not use bank address signals to generate control signals" (*Patent owner's comments, pages 52-53*)

Note the Sechen declaration, ¶¶ 23-26. Further, Patent owner takes the position that

the register limitation has functionality not taught by Amidi, Dell2 or Micron. The

examiner does not find this persuasive, for the reasons described below.

Requester 1's arguments are convincing and technically accurate, significantly

with regard to the use of bank address signals in Amidi:

"In Amidi's Fig. 6A (reproduced above), the register 608 (i.e., the claimed 'register') receives from the module connector (i.e., the claimed 'computer system') Add[n-1:0] and BA[1:0] (i.e., the claimed 'row/column address signals' and the 'bank address signals'). Fourth Wang Decl., ¶ 21, citing Amidi, Fig. 6A, ¶ [0050]. In response to the CLK0 and CLK0_N signals (i.e., the claimed 'PLL clock signals') from the PLL 606, the register 608 buffers those signals and transmits rAdd[n-1:0] and rBA[1:0] (i.e., the claimed 'buffered plurality of row/column address signals' and 'buffered bank address signals') to the memory devices 306 (i.e., the claimed 'plurality of DDR memory devices'). *Id.*, citing Amidi, Fig. 6A, ¶¶ [0050]-[0051]; [0058]-[0059]. Thus, the first part of the register amendment is met by Amidi. *Id.*

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     Further, in Amidi's Fig. 6A, the CPLD 604 (corresponding to the claimed 'logic element') receives Add(n) (corresponding to the claimed 'at least one row/column address signal received by the logic element'). Fourth Wang Deck, ¶ 22, citing Amidi, Fig. 6A, ¶ [0050]. In the Row Address Decoding scheme of Amidi, the address Add(n) is row address bit A12 corresponding to the 'at least one row address signal', specified in the claim. *Id.*, citing Amidi, ¶ [0045]-[0049]. Fig. 6A shows that the Add[n-1:0] signals received by the register 608 are separate from the Add(n) signal received by the CPLD 604, thus meeting the last limitation in the second wherein clause that the 'plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element.' *Id.*, citing Amidi, Fig. 6A, ¶¶ [0045-0051]. Thus, the second part of the register amendment is also met by Amidi. *Id.*" (*Requester 1's comments, pages 8-9*)

Note also the Wang declaration, ¶¶ 21-22.

     Requesters 2 and 3, in addition to technical arguments about the obviousness of

the register feature, point out that the PTAB has already determined that the register

amendment does not render the claims nonobvious since the limitations of the register

amendment were previously in claims that were designated as obvious in the Opinion of

May 31, 2016.

     For example:

     Claim 26 – a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

     Claim 25 (now canceled) - wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

     Claim 129 - wherein the bank address signals of the set of input control signals are received by the logic element and received and buffered by the register, the register transmitting the buffered bank address signals to the plurality of DDR memory.

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Thus, is clear that the claimed register limitation is made up entirely of limitations

lifted from claims that the PTAB has previously deemed obvious.

(3)   The "Logic element" limitation

Patent owner has added the following language to the independent claims:

"wherein the logic element generates gated column access strobe (CAS) signals
or chip-select signals of the output control signals in response at least in part to (i) the at
least one row address signal (ii) the bank address signals, and (hi) the at least one chip-
select signal of the set of input control signals and (iv) the PLL clock signal."

Patent owner argues:

"Second, the amended claims now also require that the logic element generates
certain output control signals (e.g., gated column access strobe (CAS) signals or chip-
select signals recited in claim 1) in response at least in part to (i) the at least one row
address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal
of the set of input control signals and (iv) the PLL clock signal. Amidi's CPLD 604 never
receives bank address signals and hence Amidi's control signals cannot be generated
based on bank address signals. Instead, the control signals (rcs0a, rcs0b, rcs1a, rcs1b,
rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select
signals. Thus, Amidi does not disclose the CPLD generating the gated CAS signals or
chip-select signals in response to *the bank address signals.* Second Supp. Sechen
Deck at ¶¶ 21-22. Moreover, since the output of PLL 606 is neither directly nor indirectly
transmitted to the CPLD 604, a POSITA would understand that the PLL clock does not
control the operation of CPLD 604. Thus, Amidi is further deficient by failing to disclose
the CPLD generating the gated CAS signals or chip-select signals in response to the
PLL clock signal. Id. at ¶ 18-19." (*Patent owner's comments, page 52*)

Patent owner takes the position that the claimed logic element has functionality not

taught by Amidi. Note the Sechen declaration, ¶¶ 20-22 and 25.

It appears, however, that much of patent owner's arguments are framed as if

addressing an anticipation rejection, rather than a question of obviousness. As such,

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patent owner has not adequately addressed the question of obviousness with regard to

the functionality of the CPLD in Amidi.

Requester 1 argues:

"Amidi's Fig. 6A, the CPLD 604 (corresponding to the claimed 'logic element')
generates rcs0a, rcs0b, res1a, res1b, rcs2a, rcs2b, rcs3a, rcs3b (corresponding to the
claimed 'chip-select signals') in response to Add(n) (corresponding to the claimed 'at
least one row address signal') and in response to cs0, cs1 (corresponding to the
claimed 'at least one chip-select signal of the set of input signals'). Fourth Wang Decl.,
123, citing Amidi, Fig. 6A, ¶¶ [0045]-[0052]." (*Requester 1's comments, page 9*)

Requesters 2 and 3, in addition to technical arguments about the obviousness of

the logic element, point out that the PTAB has already determined that the logic element

amendment does not render the claims nonobvious since the limitations of the logic

element amendment were previously in claims that were designated as obvious in the

Opinion of May 31, 2016.

For example:

Claim 123 – wherein the logic element is responsive at least in part to a row
address bit of the at least one row/column address signal, the bank address signals,
and the at least one chip-select signal by generating a first number of chip-select
signals of the set of output control signals.

Claim 128 – the logic element generates a first number of chip-select signals of
the set of output control signals in response at least in part to clock signals received
from the phase-lock loop device.

Claim 129 – the generation of the first number of chip-select signals of the output
control signals by the logic element is responsive at least in part to the bank address
signals.

Thus, is clear that the claimed logic element limitation is made up entirely of

limitations lifted from claims that the PTAB has previously deemed obvious.

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Rejections

As stated above, the remaining rejections to be considered are:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 2.

(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45,

50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120,

122, 123, 125-127 and 131-136 in view of Micron and Amidi.

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell

184.

(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Micron, Amidi and

Olarig.

In the discussion of these rejections by patent owner and by the third party

requesters, the arguments hinge, either directly or indirectly, on the "Phase-lock loop

(PLL) circuit" limitation, the "Register" limitation and the "Logic element" limitation, which

were added to the claims in an amendment that was intended to overcome the new

grounds of rejection by the Board.

However, despite these amendments, none of the claims subject to the new

grounds of rejection are able to overcome those rejections. For the reasons set forth

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above in reference to requester's arguments, and because every feature of these

amendments was already considered and designated as obvious in view of the same

prior art cited by the Board in the Opinion of May 31, 2016, the rejections should be

maintained.

Consequently, claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43,

45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120,

122, 123, 125-127 and 131-136 are deemed obvious in view of the art of record.

New Grounds of Rejection Proposed by Requester 1

In addition to the new grounds of rejection made by the PTAB, discussed above,

Requester 1 proposes new grounds of rejection in the comments filed August 31, 2016.

Requester 1 relies on prior art that has already been cited and considered in this

reexamination proceeding. Requester 1 asserts that claims 1, 3, 4, 6, 8, 10-15, 18-20,

22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-

83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 are obvious in view of

Amidi, Dell 2 and JEDEC 21-C.

The description of the proposed rejection, including claim charts, covers pages

12-77 of Requester 1's comments filed August 31, 2016.

After due consideration of the new grounds of rejection proposed by Requester

1, the examiner is convinced that these rejections are appropriate and tenable.

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Determination Under 37 C.F.R. 41.77(d)

It is the examiner's determination that the following rejections set forth by the

PTAB should be maintained:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 2.

(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45,

50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120,

122, 123, 125-127 and 131-136 in view of Micron and Amidi.

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell

184.

(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Micron, Amidi and

Olarig.

Additionally, it is the examiner's determination that the PTAB's decision to reject

the claims should be maintained because the prior art cited by Requester 1 renders the

claims unpatentable as set forth in the proposed rejections by Requester 1 in comments

under 41.77(c):

(5)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54,

56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-

127 and 131-136 in view of Amidi, Dell 2 and JEDEC 21-C.

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All correspondence relating to this *inter partes* reexamination proceeding should be

directed:

By EFS: Registered users may submit via the electronic filing system EFS-web, at

           https://efs.uspto.gov/efile/myportal/efs-registered

By Mail to: Mail Stop *Inter Partes* Reexam

           Attn: Central Reexamination Unit
           Commissioner of Patents
           United States Patent & Trademark Office
           P.O. Box 1450
           Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
           Central Reexamination Unit

By hand to: Customer Service Window
            Randolph Building
            401 Dulany Street
            Alexandria, VA 22314

For EFS-Web transmissions, 37 CFR 1.8(a)(1)(i) (C) and (ii) states that correspondence
(except for a request for reexamination and a corrected or replacement request for
reexamination) will be considered timely filed if (a) it is transmitted via the Office's
electronic filing system in accordance with 37 CFR 1.6(a)(4), and (b) includes a
certificate of transmission for each piece of correspondence stating the date of
transmission, which is prior to the expiration of the set period of time in the Office action.

Any inquiry concerning this communication or earlier communications from the
examiner, or as to the status of this proceeding, should be directed to the Central
Reexamination Unit at telephone number (571) 272-7705.

Signed: Conferees:
                                         /J. W./
/B. James Peikari/   Primary Examiner, Art Unit 3992
Primary Examiner
Art Unit 3992   /WHC/
                                         SPRS, Art Unit 3992

VIA EFS
Docket No.: 635162800300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:
Jayesh BHAKTA et al.

Examiner: Behzad PEIKARI

Control Nos.: 95/001,339; 95/000,578; 95/000,579

Art Unit: 3992

Filed: June 8, 2010; October 20, 2010; October 21, 2010

Conf. No.: 5035; 8810; 3547

For: MEMORY MODULE DECODER

PATENT OWNER'S COMMENTS
IN RESPONSE TO EXAMINER'S DETERMINATION
PURSUANT TO 37 C.F.R. § 41.77(e)

MS *Inter Partes* Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is in response to the Examiner's Determination Under 37 C.F.R. § 41.77(d) (the "Determination" or "Det.") dated October 3, 2017, for which a Comments submission is due on November 3, 2017 under 37 C.F.R § 41.77(e). Pursuant to § 41.77(e), the Patent Owner respectfully submits its Comments within one month of the Examiner's Determination in the present reexamination of U.S. Patent No. 7,619,912 ("the '912 Patent").

la-1364652

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Docket No. 635162800300

I.   Introduction

On July 31, 2016, Netlist, Inc. (the "Patent Owner") submitted its Patent Owner's Response Requesting To Reopen Prosecution Pursuant To 37 C.F.R. § 41.77(b)(1) ("Reopen Response" or "Reopen Resp."), including both claim amendments and evidence—a Second Supplemental Declaration of Dr. Carl Sechen Under 37 C.F.R. § 1.132 ("2nd Supp. Sechen")—to overcome the new grounds of rejection issued by the Patent and Trial Appeal Board (the "Board") in its Decision On Appeal mailed on May 31, 2016 (the "Decision").

On August 31, 2016, the Inphi Corporation ("Requester 1"), SMART Modular Technologies (WWH) Inc. ("Requester 2") and Google Inc. ("Requester 3" and now "Google LLC") each filed its respective Requester's Comments submission under 37 C.F.R. § 41.77(c) ("R1 Comments," "R2 Comments," "R3 Comments," respectively). The R1 Comments were accompanied by a Fourth Declaration of David Wang, Ph.D. dated August 30, 2016. The R2 Comments were accompanied by a Declaration of Nader Bagherzadeh, Ph.D. dated August 31, 2016.

Of particular note, the R1 Comments included a "Proposed New Rejection Of Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 Based On Amidi, Dell 2 and JEDEC 21-C." (R1 Comments at 12-77.)

The Examiner subsequently determined in his Determination that four grounds of rejections set forth by the Board's Decision should be maintained, as follows.

> (1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29 , 31, 32, 34-41, 43, 45-50, 120, 122 and 134-136 obvious over Amidi in view of Dell 2 (Ground 5)[1]

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[1] For Ground 5 (Amidi in view of Dell 2), the Examiner's claim listing appears to be incorrect for including claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 and omitting claims 120-122 and 134-136. (Decision, 68, 83.) (The Board's Decision also included claims 132 and 133 under Ground 5, but the Patent Owner believes that the inclusion of claims 132 and 133 was in error. (Reopen Resp., 53.))

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(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45, 50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 obvious over Micron in view of Amidi (Ground 13)

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 obvious over Amidi in view of Dell 184 (Ground 20)

(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 obvious over Micron in view of Amidi and Olarig (Ground 21)

(Det. at 10-11, 21.)

II.   Examiner's Determination – New Ground Of Rejection Proposed By Requester 1

With respect to Requester 1's "Proposed New Rejection . . . Based on Amidi, Dell 2 and JEDEC21-C," the Examiner's comments in their entirety are presented below from his Determination:

> In addition to the new grounds of rejection made by the PTAB, discussed above, Requester 1 proposes new grounds of rejection in the comments filed August 31, 2016.
> Requester 1 relies on prior art that has already been cited and considered in this reexamination proceeding. Requester 1 asserts that claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52,54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 are obvious in view of Amidi, Dell 2 and JEDEC 21-C.
> The description of the proposed rejection, including claim charts, covers pages 12-77 of Requester 1's comments filed August 31, 2016.
> After due consideration of the new grounds of rejection proposed by Requester 1, the examiner is convinced that these rejections are appropriate and tenable.

(Det. at 20.)

> Additionally, it is the examiner's determination that the PTAB's decision to reject the claims should be maintained because the prior art cited by Requester 1 renders the claims unpatentable as set forth in the proposed rejections by Requester 1 in comments under 41.77(c):

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la-1364652

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Docket No. 635162800300

> (5) Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 in view of Amidi, Dell 2 and JEDEC 21-C.

(*Id.* at 21.)

The Patent Owner points out that its Reopen Response already includes substantive arguments for the currently pending claims against the combination of Amidi and Dell 2 in Ground 5. (Reopen Resp. at 50-53.) Requester 1 merely adds JEDEC21-C for "meeting the limitations of the PLL amendment." (R1 Comments at 16.) Thus, even assuming, *arguendo*, that Requester 1's incorporation of teachings from JEDEC 21-C were properly combined with Amidi and Dell 2, such JEDEC 21-C teachings would be limited to Requester 1's purpose of "meeting the limitations of the PLL amendment." (*Id.*)

Moreover, analyzing different claim recitations individually would indicate an improper piecemeal approach to reviewing the obviousness of the Patent Owner's amended claims. Instead, the amended claims should be analyzed under the "as a whole" approach statutorily required by the express language of 35 U.S.C. § 103(a) for proper obviousness analysis.

Therefore, even if incorporating these JEDEC 21-C teachings were determined to meet the (i) Phase Lock Loop (PLL) Device claim amendments, this incorporation would still fail to cure the deficiencies of the combination of Amidi and Dell 2 with respect to the (ii) Register claim amendments and the (iii) Logic Element claim amendments, as the Patent Owner already argued. (Reopen Resp. at 51-53.) When considered "as a whole," the amended claims would not be obvious to a POSITA over the combination of Amidi, Dell 2 and JEDEC 21-C.

III.   Additional Points

These Remarks should be in any way construed that the Patent Owner agrees or acquiesces to any of the Examiner's rejections or rationales in his Examiner's Determination. The decision to not directly address in this Comments submission any specific points in the Examiner's Determination does not indicate that Patent Owner agrees with or acquiesces to these specific

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Control Nos.: 95/001,339; 95/000,578; 95/000,579   Docket No. 635162800300

points. The Patent Owner reserves its right to seek or defend similar claims in related applications or patents, which may be in reexamination.

Furthermore, the Patent Owner discusses above only some of the claim features of the '912 Patent and some portions of the Examiner's Determination for the sake of brevity. These discussions should not be interpreted as Patent Owner asserting or acquiescing that the patentability of the current pending claims is because of only these discussed claim features or that the Examiner's Determination is erroneous in only the discussed portions.

Additionally, where the Patent Owner has previously presented different arguments, the Patent Owner's decision to not raise them in this Response should not be construed as the Patent Owner abandoning or relinquishing those arguments. The Patent Owner reserves the right to re-present those previous arguments in this reexamination or in related application or patents, which may be in reexamination.

IV. Conclusion

The Patent Owner respectfully requests that the pending claims be confirmed or allowed.

If the Patent Office determines that relief is required, the Patent Owner petitions for any required relief and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **635162800300.**

Dated: November 3, 2017   Respectfully submitted,

By: /David S. Kim/
David S. Kim
   Registration No.: 57,143
MORRISON & FOERSTER LLP
707 Wilshire Boulevard
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(213) 892-5479

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la-1364652

Control Nos.: 95/001,339; 95/000,578; 95/000,579   Docket No. 635162800300

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 1.903, the undersigned, on behalf of the Patent Owner, hereby certifies that a copy of the following documents:

1.   Patent Owner's Comments In Response To Examiner's Determination Pursuant To 37 C.F.R. § 41.77(e)

was served on the third party requesters via first class mail on the date below. The name and address of the parties served are as follows.

For Requester 95/000,578:

Michael Heafey
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600 Peachtree, N.E., Suite 5200
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For Requester 95/000,579:

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For Requester 95/001,339:

David A. Jakopin
Pillsbury Winthrop Shaw Pittman LLP
P.O. Box 10500 – Intellectual Property Group
McLean, VA 22102

Date: November 3, 2017   /David S. Kim/
                                           David S. Kim

6

la-1364652

Electronic Acknowledgement Receipt

EFS ID:	30855854
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	David S. Kim/Erwin Palines
Filer Authorized By:	David S. Kim
Attorney Docket Number:	17730-3
Receipt Date:	03-NOV-2017
Filing Date:	20-OCT-2010
Time Stamp:	20:02:54
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		63516-28003_PO_Comments.pdf	38029 66697fcc36f36abe9a4ed9422220a4f7eb4fa a16	yes	6

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Patent Owner Comments on Examiner's Determination after Board Decision	1	5
Reexam Certificate of Service	6	6

Warnings:	
Information:	
Total Files Size (in bytes):	38029

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

<div align="right">

Reexamination Control No.: 95/001,339; 95/000,578; 95/000,579

U.S. Patent No. 7,619,912

</div>

CERTIFICATE OF SERVICE UNDER 37 C.F.R. §§ 1.33(c), 1.248, AND 1.915 (b)(6)

I hereby certify that true copies of the foregoing documents:

1) **Transmittal letter;**

2) **THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) REPLY TO PATENT OWNER'S COMMENTS IN RESPONSE TO EXAMINER'S DETERMINATION PURSUANT TO 37 C.F.R. § 41.77(e)**

3) **Certificate of Service.**

were electronically filed with the US Patent Office and were served in their entirety by First Class Mail on the date indicated below to the attorneys of record for the Assignee/Owner of the subject patent, **Netlist Inc.,** as well as sent to attorneys of record for Google Inc. and Smart Modular Technologies Inc., at/to addresses indicated below:

For Patent Owner:
> Mehran Arjomand
> Morrison & Foerster, LLP
> 707 Wilshire Boulevard
> Los Angeles, CA 90017-3543

For Third Party Requester 95/000,578:
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For Third Party Requester 95/000,579:
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> Palo Alto, CA 94304

Date Mailed December 1, 2017   By: _____
Desiree Ortiz

4825-8236-0151.v1

<div align="right">

Samsung Electronics Co., Ltd.
Ex. 1010, p. 7671

</div>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE REEXAMINATION OF	:	U.S. Patent No. 7,619,912
CONTROL NOS.:		95/001,339; 95/000,578; 95/000,579
REEXAM FILING DATE	:	June 8, 2010
CONFIRMATION NOS.	;	5035; 8810; 3547
ART UNIT	:	3992
EXAMINER	:	Behzad Peikari
ATTORNEY DOCKET	:	043326-0000021

FOR: MEMORY MODULE DECODER

Mail Stop *Inter Partes* Reexamination
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) REPLY TO PATENT OWNER'S COMMENTS IN RESPONSE TO EXAMINER'S DETERMINATION PURSUANT TO 37 C.F.R. § 41.77(e)

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I.   Introduction And Procedural Background

This Reply is in response to Patent Owner's Comments In Response To Examiner's Determination Pursuant To 37 C.F.R. § 41.77(e) ("Patent Owner's Comments"), filed November 3, 2017. This Reply is being timely filed within the one month period following the Patent Owner's Comments, as specified by 37 C.F.R. § 41.77(e).

On October 3, 2017, the Examiner issued a Determination under 37 C.F.R. § 41.77(d) (the "Determination"). On pages 2-8, the Determination sets forth a "Timeline" reviewing the procedural background of the present merged *inter partes* reexamination proceeding. Requester 1 believes that the timeline provided by the Examiner is correct except that it omits reference to the following: i) Petition For Clarification Of Rejection In Decision On Appeal By Third Party Requester Under 37 C.F.R. § 41.3, filed by SMART Modular Technologies, Inc. (Requester 2) on June 13, 2016; ii) June 27, 2016 Decision On Petition, granting Requester 2's June 13, 2016 petition; iii) Appellant Inphi's Request for Rehearing, filed June 30, 2016; and iv) Respondent's (Patent Owner's) Comments To Requester 1's Request For Rehearing Under 37 C.F.R. § 41.79(c), filed August 1, 2016.

Notwithstanding that the Examiner did not explicitly refer to Requester 2's June 13, 2016 petition and the Office's June 27, 2016 decision granting such petition, the Examiner recognized the clarification provided by the June 27, 2016 decision. Specifically, the Examiner noted that his pre-appeal decision not to reject claims 52-54, 56, 67-71, 77-79, 82-84 and 87-89 under 35 U.S.C. § 103 based on Amidi and Dell 184 (Ground 20) was reversed by the Board. October 3, 2017 Determination at 7, citing the Board's May 31, 2016 Decision on Appeal at 91-93.

The Examiner had no reason to refer to Requester 1's June 30, 2016 Request For Rehearing or the Patent Owner's August 1, 2016 Comments thereon, as they are exclusively within the purview of the Board. The Request for Rehearing is mentioned here because, as

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explained below, it is related to Patent Owner's assertion that inclusion of claims 132 and 133 in the Ground 5 rejection made by the Board in the May 31, 2016 Decision was in error. Patent Owner's Comments at 2, note 1, citing Reopen Resp. at 53.

II.   The Rejections Considered In The Examiner's 37 C.F.R. § 41.77(d) Determination

On pages 10-11, the October 3, 2017 Determination lists the specific rejections from the Board's May 31, 2016 Decision to be considered, in view of Patent Owner's August 1, 2016 Request To Reopen Prosecution, as follows:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 2 (Ground 5).

(2)   Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 27-29, 31, 32, 36-39, 41, 43, 45, 50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 in view of Micron and Amidi (Ground 13).

(3)   Claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Amidi and Dell 184 (Ground 20).

(4)   Claims 52, 54, 67, 69-71, 77, 78, 82, 83, 87 and 88 in view of Micron, Amidi and Olarig (Ground 21).

In its November 3, 2017 Comments, Patent Owner likewise lists the grounds of rejection set forth by the Board's Decision. Patent Owner's Comments at 2, 3. With respect to Grounds 13, 20 and 21, the Patent Owner identifies the same claims and references as respectively identified by the Examiner. *Id.* at 3. However, with respect to Ground 5, the Patent Owner's claim listing differs from the Examiner's claim listing in that for Ground 5, the Patent Owner lists claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 120, 122 and 134-136. *Id.* According to Patent Owner, "[f]or Ground 5 (Amidi in view of Dell 2), the Examiner's claim listing appears to be incorrect by including claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 and omitting claims 120 [,] 122 and 134-136." Patent Owner's Comments at 2, note 1, citing Decision at 68, 83. Patent Owner further states, "[t]he Board's Decision also included

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claims 132 and 133 under Ground 5, but the Patent Owner believes that the inclusion of claims 132 and 133 was in error." *Id.,* citing its July 31, 2016 Reopen Resp. at 53.

Requester 1 believes that the listing in the October 3, 2017 Determination for the Ground 5 claims is incorrect by including claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 and omitting claims 120, 122 and 132-136. *See* May 31, 2016 Decision at 68 (listing the claims within the non-adopted rejection under Ground 5); *Id.* at 78 ("Requester 1 disputes the Examiner['s] non-adoption of the proposed rejection of claims 1, 3, 4, 6, 8, 10-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 and 132-136 based on Amidi and Dell 2."); *Id.* at 83 ("For the above reasons, we do not sustain the Examiner's decision not to reject (1) claims 1, 120-122, and 132-136, (2) claims 15, 28 and 39, which recite similar limitations to claim 1, and (3) the remaining claims not separately argued under § 103 based on Amidi and Dell 2. We sustain the Examiner's decision not to adopt the proposed rejection for claims 16 and 17 and do not reach the propriety of the non-adopted rejection of claim 119").

In view of the Board's May 31, 2016 Decision, and after Patent Owner's July 31, 2016 cancellation of claims 25, 42, 121 and 128-130, Requester 1 believes that the claims rejected under Ground 5 based on Amidi and Dell 2 are claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 120, 122 and 132-136. Thus, Requester 1 believes that the Examiner's October 3, 2017 listing of the Ground 5 claims was incorrect by including claims 52, 54, 56, 67, 69-71, 77, 78, 82, 83, 87 and 88 and by omitting claims 120, 122 and 132-136.

As the Board's May 31, 2016 Decision specifically identified claims 132-136 in reversing the Examiner's non-adoption of the Ground 5 rejection, Requester 1 believes that the Board's inclusion of claims 132 and 133 in the Ground 5 rejection was not in error, as alleged by Patent Owner. However, Requester 1 notes that there is an apparent inconsistency in the Board

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reversing the Examiner's decision not to reject claims 132 and 133 under Ground 5, yet

sustaining the Examiner's decision not to reject claims 16 and 17 under Ground 5. At the time of

the Board's May 31, 2016 Decision, claims 16 and 132 had nearly the same scope, and claims 17

and 133 had nearly the same scope.[1]

Requester 1 respectfully submits that claims 16 and 17 are unpatentable (at least based on

Amidi and Dell 2 under Ground 5) for the reasons set forth in Requester 1's June 30, 2016

Request for Rehearing. Consideration of that request and granting of the relief specified therein

are respectfully requested.

III.   The Examiner Correctly Determined That The Board's Rejection Under Ground 5 Should
        Be Maintained Notwithstanding Patent Owner's Amendments.

On pages 12-18 of the Determination, the Examiner analyzes in detail each of the "Phase-

Lock Loop (PLL) Device", "Register" and "Logic Element" limitations added to the independent

claims with respect to the cited references. Based on such analysis, the Examiner concludes that

the Ground 5 references (in particular, Amidi) meet or render obvious each of the added claim

limitations. *See* Determination at 12-14 with respect to the "Phase-Lock Loop (PLL) Device"

limitation; *Id.* at 15-16 with respect to the "Register" limitation; *Id.* at 17-18 with respect to the

"Logic Element" limitation.

In its Comments, Patent Owner notes that its Reopen Response includes arguments for

the currently pending claims against the combination of Amidi and Dell 2 under Ground 5.

Patent Owner's Comments at 4, citing Reopen Resp. at 50-53. In evaluating the patentability of

---

[1] Rejected claims 132 and 133 were actually narrower than claims 16 and 17, respectively, since
claims 132 and 133 depended from claim 15 as amended by the inclusion of a wherein clause
which did not appear in original claim 15 as incorporated into claim 16. Claims 132 and 133
are now substantially narrower than claims 16 and 17, respectively, due to Patent Owner's
further amendment of claim 15 in its August 1, 2016 Reopen Response.

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the amended claims, the Examiner took into account the Patent Owner's Reopen Response

arguments. *See* Determination at 12-13, 15 and 17. The Examiner nevertheless determined that

the Ground 5 references render the amended claims obvious. Notwithstanding the Examiner's

analysis, Patent Owner does not address in its Comments "any specific points in the Examiner's

Determination." Patent Owner's Comments at 4.

Based on the Examiner's analysis, and in view of Patent Owner's silence as to how the

Examiner made any improper findings or conclusions, Requester 1 respectfully requests the

Board to affirm the Examiner's determination that the Ground 5 rejection should be maintained.

For the reasons explained in the prior section, Requester 1 believes that the claims rejected by

the Board under Ground 5 (i.e., obviousness based on Amidi in combination with Dell 2) are

claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 120, 122 and 132-136.

For the reasons explained in its June 30, 2016 Request For Rehearing, Requester 1 respectfully

requests that claims 9 and 16 also be rejected under Ground 5.

IV.   The Examiner Correctly Determined That All Of The Claims For Which Prosecution
       Was Reopened Are Rendered Obvious By The Combination Of Amidi, Dell 2 and
       JEDEC-21C

In its August 31, 2016 Comments On Patent Owner's Response Requesting To Reopen

Prosecution, Requester 1 proposed a new ground of rejection for all of the claims for which

prosecution was reopened based on the combination of Amidi, Dell 2 and JEDEC-21C, all of

which were of record and considered by the Board in its May 31, 2016 Decision. *See* Requester

1 Comments at 12-15. The relevance of Amidi, Dell 2 and JEDEC-21C to the newly added

claim limitations and the motivations to combine Amidi with Dell 2, and Amidi with JEDEC-

21C are set forth in Requester 1's Comments. *Id.* at 15-17.

In its November 3, 2017 Comments In Response To Examiner's Determination, Patent

Owner states that Requester 1 adds JEDEC-21C to the prior Ground 5 combination of Amidi and

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Dell 2 merely for meeting the limitations of the PLL amendment. Patent Owner Comments at 4, citing Requester 1's Comments at 16. Patent Owner argues that JEDEC-21C's teachings are therefore limited to the purpose of meeting the limitations of the PLL amendment. *Id.* Patent Owner mischaracterizes Requester 1's use of JEDEC-21C. As stated in Requester 1's Comments, "Amidi in combination with JEDEC-21C are used to meet the limitations in the PLL amendment (first wherein clause)", and "Amidi in combination with JEDEC-21C further in combination with Dell 2 are used to meet the limitations in the logic element amendment (third wherein clause)." Requester 1 Comments at 15, 16. With regard to the other newly added limitation, i.e., the "Register" limitation, as previously noted by Requester 1, "Patent Owner does not expressly argue that the amended claims distinguish over the references utilized in the Board's new ground of rejection on account of the register amendment *per se.*" Requester 1 Comments at 16; *See also* Patent Owner's Reopen Resp. at 51-55.

In any event, Requester 1's Comments set forth detailed reasons, including claim charts, explaining how the combination of Amidi, Dell 2 and JEDEC-21C meet not only the newly added claim limitations, but also each and every limitation of all the claims for which prosecution was reopened, as the basis for a new ground of rejection. *See* Requester 1 Comments at 17-77. "After due consideration of the new grounds of rejection proposed by Requester 1, the examiner is convinced that these rejections are appropriate and tenable." Determination at 20.

Requester 1 respectfully requests the Board to affirm the Examiner's rejection of all the claims for which prosecution was reopened as being obvious under § 103 in view of Amidi, Dell 2 and JEDEC-21C. Requester 1 further requests the Board, utilizing its discretionary authority under 37 C.F.R. § 41.77(b), to include claims 16 and 17 within the § 103 rejection based on

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Amidi, Dell 2 and JEDEC-21C, as claims 16 and 17 are broader in scope than amended claims 132 and 133 which were rejected by the Examiner. *See* Note 1 at 5 hereof and Determination at 21, paragraphs (2) and (5); *see also* Requester 1 Comments at 75-76, 26-31; *and c.f.* claims 16 and 17 as set forth in Requester 1's June 30, 2016 Request for Rehearing.

V.   Conclusion

For any and all reasons set forth above, Requester 1 respectfully requests the Board to make the following rejections:

(1)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 120, 122 and 132-136 are unpatentable under § 103 over Amidi in view of Dell 2.

(2)   Claims 16 and 17 are unpatentable under § 103 over Amidi in view of Dell 2.

(3)   Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 are unpatentable under § 103 over Amidi in view of Dell 2 further in view of JEDEC-21C.

(4)   Claims 16 and 17 are unpatentable under § 103 over Amidi in view of Dell 2 further in view of JEDEC-21C.

Date: December 1, 2017

Respectfully submitted,

__/David A. Jakopin, #32995/_____
David A. Jakopin
Reg. No. 32,995
Customer No. 27,498

8

4834-4736-5462.v1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE RE-EXAMINATION OF	:	U.S. Patent No. 7,619,912	Art Unit: 3992
CONTROL NOS.	:	95/001,339; 95/000,578; 95/000,579	Conf. Nos: 5035, 8810, 3547
FILING DATE	:	June 8, 2010	
ASSIGNEE	:	NETLIST INC., IRVINE CA	
EXAMINER	:	Behzad Peikari	
FOR:		MEMORY MODULE DECODER	

Mail Stop *Inter Partes* Reexamination
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER

Applicant herewith submits the following:

1. THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) REPLY TO PATENT OWNER'S COMMENTS IN RESPONSE TO EXAMINER'S DETERMINATION PURSUANT TO 37 C.F.R. § 41.77(e)

2. Certificate of Service

Requester does not believe a fee is due for this submission. However, should the Commissioner determine a fee is necessary, he is authorized to charge the appropriate fee to deposit account no. 033975 (ref: 043326-0000021).

Date: December 1, 2017

Respectfully submitted,
PILLSBURY WINTHROP SHAW PITMAN LLP

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David A. Jakopin
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Customer No. 27,498

ADDRESS:
IP Docketing
P.O. Box 10500
McLean, VA 22102

4830-1673-2759.v1

Electronic Acknowledgement Receipt

EFS ID:	31091198
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	David A. Jakopin
Filer Authorized By:	
Attorney Docket Number:	17730-3
Receipt Date:	01-DEC-2017
Filing Date:	20-OCT-2010
Time Stamp:	12:36:13
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Inphi_Reply_to_Patent_Owner_Comments_In_Response_Examiners_Determination_1DEC2017.PDF	127117 c582ff4d5f806b72d3828b7621f00a5804c368df	yes	10

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Reexam Certificate of Service	10	10
Requester Comments on Patent Owner Response after Board Decision	2	9
Trans Letter filing of a response in a reexam	1	1

Warnings:

Information:

Total Files Size (in bytes):	127117

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

<u>Reexamination Control No.: 95/001,339; 95/000,578; 95/000,579</u>

<u>U.S. Patent No. 7,619,912</u>

<u>CORRECTED CERTIFICATE OF SERVICE UNDER 37 C.F.R. §§ 1.33(c), 1.248, AND 1.915 (b)(6)</u>

I hereby certify that true copies of the foregoing documents:

1) **Transmittal letter;**

2) **THIRD PARTY REQUESTER INPHI CORP.'S (REQUESTER 1'S) REPLY TO PATENT OWNER'S COMMENTS IN RESPONSE TO EXAMINER'S DETERMINATION PURSUANT TO 37 C.F.R. § 41.77(e)**

3) **Certificate of Service.**

were electronically filed with the US Patent Office and were served in their entirety by First Class Mail on the date indicated below to the attorneys of record for the Assignee/Owner of the subject patent, **Netlist Inc.**, as well as sent to attorneys of record for Google Inc. and Smart Modular Technologies Inc., at/to addresses indicated below:

> For Patent Owner:
> Mehran Arjomand
> Morrison & Foerster, LLP
> 707 Wilshire Boulevard
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> For Third Party Requester 95/000,578:
> Michael F. Heafey
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> Atlanta, Georgia 30308-2216

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> Bank of America Plaza
> 600 Peachtree, N.E., Suite 5200
> Atlanta, Georgia 30308-2216

Date Mailed   <u>December 1, 2017</u>   By: _____
                                            Desiree Ortiz

Electronic Acknowledgement Receipt

EFS ID:	31103395
Application Number:	95000578
International Application Number:	
Confirmation Number:	8810
Title of Invention:	MEMORY MODULE DECODER
First Named Inventor/Applicant Name:	7619912
Customer Number:	25224
Filer:	David A. Jakopin
Filer Authorized By:	
Attorney Docket Number:	17730-3
Receipt Date:	01-DEC-2017
Filing Date:	20-OCT-2010
Time Stamp:	13:50:40
Application Type:	inter partes reexam

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reexam Certificate of Service	Corrected_Cert_Service.PDF	17015 ede38fc313a4b257f5eb526ae161e5d5ec424fcb	no	1

Warnings:

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Total Files Size (in bytes):	17015

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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95|00133A
95|000579

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224   7590   02/12/2018
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
02/12/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Transmittal of Communication to Third Party Requester *Inter Partes* Reexamination	Control No. 95/000,579; 95/000,578; 95/001339	Patent Under Reexamination 7619912
	Examiner B. JAMES PEIKARI	Art Unit 3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

┌──── (THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS) ────┐

MICHAEL F. HEAFEY
TROUTMAN/GOOGLE LLC
ATTN: PATENTS
600 PEACHTREE STREET
SUITE 5200
ATLANTA, GA 30308

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination prceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it <u>cannot</u> be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

U.S. Patent and Trademark Office
PTOL-2070 (Rev. 07-04)

Paper No. 20180202

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
95/000,578; 95/000,579 95/001,339	20 October, 2010	7619912	17730-3

		EXAMINER	
MORRISON & FOERSTER, LLP 707 Wilshire Boulevard LOS ANGELES, CA 90017		B. JAMES PEIKARI	
		ART UNIT	PAPER
		3992	20180201

DATE MAILED:

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Commissioner for Patents

See Attached.

/MF/	B. JAMES PEIKARI Primary Examiner Art Unit: 3992

PTO-90C (Rev.04-03)

Application/Control Numbers:
95/000,578; 95/000,579; 95/001,339   Page 2
Art Unit: 3992

ATTACHMENT TO INTER PARTES REEXAMINATION COMMUNICATION

The USPTO mailed the examiner's determination under 37 CFR 41.77(d) on

October 3, 2017.

The following comments in response to the Examiner's Determination were filed

pursuant to 37 CFR 41.77(e):

- Patent Owner's comments received November 3, 2017.

The following replies were received in response to comments submitted pursuant to

37 CFR 41.77(e):

- Third Party Requester's [Requester 1; 95/000,578] reply to Patent Owner's

  comments received December 1, 2017.

MPEP 2682 states:

"Patent owner and third party requester(s) have one month from the mailing date of the
determination under 37 CFR 41.77(d) to once file comments on the determination. If
any comments are filed, each opposing party may then file a single reply to the
comments from an opposing party. No amendments or further evidence may be
submitted as part of these comments."

"Comments and/or replies that do not comply with 37 CFR 41.77(e) will not be entered
but will remain in the record for the proceeding. The examiner will notify the parties and
the Board of the compliance with 37 CFR 41.77(e) and will forward the proceeding to
the Board."

Application/Control Numbers:
95/000,578; 95/000,579; 95/001,339   Page 3
Art Unit: 3992

The comments filed November 3, 2017 and the response filed December 1, 2017 satisfy

the requirements of 37 CFR 41.77(e) and will be entered.

This proceeding will be forwarded to the Patent Trial and Appeal Board (PTAB) for

consideration under 37 CFR 41.77(f).

Application/Control Numbers:
95/000,578; 95/000,579; 95/001,339   Page 4
Art Unit: 3992

   All correspondence relating to this *Inter Partes* reexamination proceeding should

be directed:

  By EFS: Registered users may submit via the electronic filing system EFS-web, at

      https://efs.uspto.gov/efile/myportal/efs-registered

  By Mail to: Mail Stop *Inter Partes* Reexam

      Attn: Central Reexamination Unit
      Commissioner of Patents
      United States Patent & Trademark Office
      P.O. Box 1450
      Alexandria, VA 22313-1450

  By FAX to: (571) 273-9900
      Central Reexamination Unit

  By hand to: Customer Service Window
      Randolph Building
      401 Dulany Street
      Alexandria, VA 22314

For EFS-Web transmissions, 37 CFR 1.8(a)(1)(i) (C) and (ii) states that correspondence
(except for a request for reexamination and a corrected or replacement request for
reexamination) will be considered timely filed if (a) it is transmitted via the Office's
electronic filing system in accordance with 37 CFR 1.6(a)(4), and (b) includes a
certificate of transmission for each piece of correspondence stating the date of
transmission, which is prior to the expiration of the set period of time in the Office action.

Any inquiry concerning this communication or earlier communications from the
examiner, or as to the status of this proceeding, should be directed to the Central
Reexamination Unit at telephone number (571) 272-7705.

Signed:

/B. James Peikari/

Primary Examiner
Art Unit 3992

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224   7590   02/26/2018
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
02/26/2018	PAPER

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The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

United States Patent and Trademark Office

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MORRISON & FOERSTER, LLP
707 WILSHIRE BOULEVARD
LOS ANGELES, CA 90017

Appeal No: 2018-003618
Inter Partes Reexamination Control Nos: 95/000,578; 95/000,579;
95/001,339
Appellants: SMART Modular Technologies (WWH), Inc., (1st Requester -
95/000,578); Google, Inc., (2nd Requester – 95/000,579); Inphi Corp., (3rd
Requester – 95/001,339); Netlist, Inc. (Patent Owner)

Patent Trial and Appeal Board Docketing Notice

Inter Partes Reexamination Control Nos. 95/000,578; 95/000,579; and 95/001,339 were received
from the Technology Center at the Board on February 20, 2018 and have been assigned Appeal
No: 2018-003618.

In all future communications regarding this appeal, please include all of the *Inter Partes*
Reexamination Control Numbers and the appeal number.

The mailing address for the Board is:

PATENT TRIAL and APPEAL BOARD
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VIRGINIA 22313-1450

Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number
listed above.

By order of the Patent Trial and Appeal Board.

MAT

Page 2

cc: Third Party Requesters – 95/000,578; 95/000,579; 95/001,339

TROUTMAN SANDERS LLP
ATTN: PATENTS
600 PEACHTREE STREET NE
SUITE 5200
ATLANTA, GA 30308

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

95/000,579; 95/001,389

25224 7590 02/26/2018	EXAMINER	
MORRISON & FOERSTER, LLP	PEIKARI, BEHZAD	
707 Wilshire Boulevard		
LOS ANGELES, CA 90017	ART UNIT	PAPER NUMBER
	3992	
	MAIL DATE	DELIVERY MODE
	02/26/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Ex. 1010, p. 7695
SAM-NET-293_00033966

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

TROUTMAN SANDERS LLP

ATTN: PATENTS

600 PEACHTREE STREET NE

SUITE 5200

ATLANTA, GA 30308

Transmittal of Communication to Third Party Requester
Inter Partes Reexamination

REEXAMINATION CONTROL NUMBER 95000,579; (95/000,578) 95/001,339

PATENT NUMBER 7619912.

TECHNOLOGY CENTER 3900.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it <u>cannot</u> be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

PTOL-2070 (Rev.07-04)

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

Page 1

United States Patent and Trademark Office

**Under Secretary of Commerce for Intellectual Property and
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MORRISON & FOERSTER, LLP
707 WILSHIRE BOULEVARD
LOS ANGELES, CA 90017

Appeal No: 2018-003618
Inter Partes Reexamination Control Nos: (95/000,578) 95/000,579;
95/001,339
Appellants: SMART Modular Technologies (WWH), Inc., (1st Requester -
95/000,578); Google, Inc., (2nd Requester – 95/000,579); Inphi Corp., (3rd
Requester – 95/001,339); Netlist, Inc. (Patent Owner)

Patent Trial and Appeal Board Docketing Notice

Inter Partes Reexamination Control Nos. (95/000,578) 95/000,579; and 95/001,339 were received
from the Technology Center at the Board on February 20, 2018 and have been assigned Appeal
No: 2018-003618.

In all future communications regarding this appeal, please include all of the *Inter Partes*
Reexamination Control Numbers and the appeal number.

The mailing address for the Board is:

**PATENT TRIAL and APPEAL BOARD
UNITED STATES PATENT AND TRADEMARK OFFICE
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ALEXANDRIA, VIRGINIA 22313-1450**

Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number
listed above.

By order of the Patent Trial and Appeal Board.

MAT

cc: Third Party Requesters – 95/000,578; 95/000,579; 95/001,339

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,578	10/20/2010	7619912	17730-3	8810

25224   7590   06/01/2018
MORRISON & FOERSTER, LLP
707 Wilshire Boulevard
LOS ANGELES, CA 90017

EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
06/01/2018	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

INPHI CORP.
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

_____

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

_____

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges.*

POTHIER, *Administrative Patent Judge.*

DECISION UNDER 37 C.F.R. § 41.77(f)

Appeal 2018-003618
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

<div align="center">STATEMENT OF THE CASE</div>

These proceedings involve U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon.

In our earlier Decision ("Dec.") mailed May 31, 2016, we affirmed the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi[1] under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC[2] under § 103, (4) claims 16 and 17 based on Amidi and Dell 2[3] under § 103, and (5) claims 57,[4] 58, 60, 68, 79, 84, 89–91, and 128–131 under § 112, first paragraph, as lacking written description support. Dec. 101–02. We additionally reversed the Examiner's decision not to adopt the rejections of:

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[1] U.S. Publ. 2006/0117152 A1 (published June 1, 2006 and filed Jan. 5, 2004) (Amidi).
[2] JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C); *JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C* (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C); *JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A)* 1-12 (May 2003) (JEDEC 82-4B). As indicated in the previous Decision, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.
[3] U.S. Patent No. 6,209,074 (issued Mar. 27, 2001) (Dell 2).
[4] The summary at the end of the Decision (Dec. 102) mistakenly omits independent claim 57. *See id.* at 84–89 (discussing claim 57 under the Lack of Written Description Support section).

<div align="center">2</div>

Appeal 2018-003618
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–43, 45–50, 120–122, and 132–136 based on Amidi and Dell 2 (Ground 5[5]) (*see id.* at 78–83, 102), (2) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 25, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 based on Micron[6] and Amidi (Ground 13) (*see id.* at 93–99, 102), (3) claims 52–54, 56, 67–71, 77–79, 82–84, and 87–89 based on Amidi and Dell 184[7] (Ground 20) (*see id.* at 91–93, 102), and (4) claims 52–54, 67–71, 77–79, 82–84, and 87–89 based on Micron, Amidi, and Olarig[8] (Ground 21) (*see id.* at 99–102). We designated the reversed, non-adopted rejections as new grounds. *Id.* at 102.

In Patent Owner's Response Requesting to Reopen Prosecution submitted August 1, 2016 (PO Response), Patent Owner canceled claims 25, 42, 53, 68, 79, 84, 89, 92, 93, 121, 124, and 128–130 of the '912 patent. PO Response 2. Previously, claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and 112–118 were canceled. *Id.* at 46. According to Patent Owner, claims 1, 15, 28, 39, 43, 52, 54, 58, 67, 77, 82, 87, 123, 125, 131, and 134–136 have been amended. *See id.* at 46. Patent Owner also submitted a declaration of Dr. Carl Sechen, dated July 31, 2016. Requesters 1 through 3 submitted comments (R1 Comments, R2 Comments, and R3 Comments) pursuant to 37 C.F.R. § 41.77(c) on August 31, 2016. Requester 1 presents a declaration of Dr. David Wang, dated August 30, 2016; Requester 2

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[5] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters refer to the various rejections by ground number. *See, e.g.,* RAN 11–15. We include the ground number here and throughout the Decision.
[6] Micron, *DDR SDRAM RDIMM, MT36VDDF12872-1GB, MT36VDDF25672-2GB* I-20 (2002) (Micron).
[7] U.S. Patent No. 6,446,184 B2 (issued Sept. 3, 2002) (Dell 184).
[8] U.S. Patent No. 6,260,127 B1 (issued July 10, 2001) (Olarig).

Appeal 2018-003618
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

presents a declaration of Dr. Nader Bagherzadeh, dated August 31, 2016. Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 were the subject of the remand order mailed February 9, 2017. Order 5.[9]

On remand, the Examiner maintained the following rejections in the Examiner's Determination (Ex. Deter.):

(1) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136[10] based on Amidi and Dell 2 (Ground 5),

(2) claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184 (Ground 20),

(3) claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi (Ground 13), and

(4) claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig (Ground 21). Ex. Deter. 21.

The Examiner further adopted Requester 1's proposed rejection of (5) claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C. *Id.*

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[9] A subsequent remand order was mailed May 2, 2017, and a Petition Decision related to the subsequent remand order was mailed June 5, 2017.
[10] The Examiner adds claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 to, and omits claims 120, 122 and 132–136 from, Ground 5. Ex. Deter. 21. We agree with Patent Owner that these additions and omissions were in error. PO Comments 2 n.1.

4

Appeal 2018-003618
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

After the Examiner's Determination, Patent Owner submitted comments (PO Comments) on November 3, 2017 and Requester 1 responded (R1 Reply) on December 1, 2017 pursuant to 37 C.F.R. § 41.77(e).

This proceeding has returned to the Board under 37 C.F.R. § 41.77(f). Our new Decision is deemed to incorporate our earlier Decision, except for any portion specifically withdrawn. 37 C.F.R. § 41.77(f).

Claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 are independent claims; claim 58 depends from independent claim 57. Claim 57 was not part of the remand. The remaining claims on remand depend directly or indirectly from these claims. Illustrative, independent claim 1 reads as follows:

> 1. (Twice Amended) A memory module connectable to a computer system, the memory module comprising:
> a printed circuit board;
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
> a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the

5

Appeal 2018-003618
Merged Control 95/001,339, 95/000,578, and 95/000,579
Patent 7,619,912 B2

plurality of memory devices, the first command signal and the set of
input control signals corresponding to the second number of ranks and
the second command signal and the set of output control signals
corresponding to the first number of ranks; and
    a phase-lock loop device mounted to the printed circuit board,
the phase-lock loop device operatively coupled to the plurality of
DDR memory devices, the logic element, and the register,
    wherein, in response to signals received from the computer
system, the phase-lock loop (PLL) device transmits a PLL clock signal
to the plurality of DDR memory devices, the logic element, and the
register,
    wherein, the register (i) receives, from the computer system,
and (ii) buffers, in response to the PLL clock signal, a plurality of
row/column address signals and the bank address signals, and (iii)
transmits the buffered plurality of row/column address signals and the
buffered bank address signals to the plurality of DDR memory
devices, wherein the at least one row/column address signal received
by the logic element comprises at least one row address signal
received by the logic element, and wherein the plurality of
row/column address signals received by the register are separate
from the at least one row address signal received by the logic element,
and
    wherein the logic element generates gated column access strobe
(CAS) signals or chip-select signals of the output control signals in
response at least in part to _(i) the at least one row address signal, (ii)_
the bank address signals, and (iii) the at least one chip-select signal of
the set of input control signals and (iv) the PLL clock signal.

PO Response 2–3 (underlining amendments relative to the originally issued
claims and italicizing newly added subject matter relative to the claims as
originally appealed).

The following summarizes various declarations in this proceeding:

Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),

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Declaration of Dr. Carl Sechen dated July 31, 2016 (2d Supp.[11] Sechen Decl.),

Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

Declaration of Dr. David Wang dated August 30, 2016 (4th Wang Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated August 31, 2016 (4th[12] Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.), and

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.).

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[11] We deviate from our nomenclature for other declarations to be consistent with Patent Owner's discussion. *See, e.g.,* PO Response 47.

[12] Requester 2 describes this declaration as "Bagherzadeh Decl. V" (R2 Comments 8). We however number the declaration sequentially as part of this list.

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Maintained/Adopted Rejections

In the Examiner's Determination, the Examiner maintains or adopts the following grounds of rejection:

References	Basis	Claims	Presented/Maintained
Amidi and Dell 2 (Ground 5)	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136	Dec. 78–83; Ex. Deter. 21; *see also* above footnote 10
Amidi, Dell 2, and JEDEC 21-C	§ 103(a)	1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Ex. Deter. 21

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Amidi and Dell 184 (Ground 20)	§ 103(a)	52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 91–93; Ex. Deter. 21
Micron and Amidi (Ground 13)	§ 103(a)	1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	Dec. 93–99; Ex. Deter. 21
Micron, Amidi, and Olarig (Ground 21)	§ 103(a)	52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88	Dec. 99–102; Ex. Deter. 21

II. ISSUES

The main issues are whether Patent Owner has presented sufficient arguments and evidence to overcome the new grounds of rejection for and the newly adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 presented in the May 31, 2016 Decision and the Examiner's Determination.

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III. ANALYSIS

A. *Amidi and Dell 2* (Ground 5)

In our May 31, 2016 Decision, claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 (canceled claims omitted) were rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 78–83. Patent Owner presents several argument related to this ground, asserting the amendments to independent claims 1, 15, 28, and 39 overcome the new grounds. PO Response 50–53. Patent Owner asserts the claimed "logic element [now] generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal of the set of input control signals, and (iv) the PLL [phase lock loop] clock signal." *Id.* at 52; *see also id.* at 3 (underlining omitted). Throughout this Decision, we will refer to this new limitation as the "logic element" limitation and the response signals collectively as signals (i)–(iv) or individually as signal (i), (ii), (iii), or (iv).

Regarding the "logic element" limitation, Patent Owner argues (1) "Amidi's CPLD 604 never receives bank address signals," instead generating control signals (e.g., chip select signals rcs0a–rcs3b) based on a row address signal and chip-select signals and (2) Dell 2 does not cure Amidi's deficiencies. *Id.* at 52 (citing 2d Supp. Sechen Dec. ¶¶ 21–22, 25). Additionally, Patent Owner argues combining Amidi and Dell 2 would not teach or suggest to one skilled in the art generating control signals based on a row address signal and bank address signals as now recited in the claims. *See id.* at 52–53 (citing 2d Supp. Sechen Dec. ¶¶ 23–24, 26).

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The Examiner maintained the Amidi/Dell 2 rejection on remand. Ex. Deter. 21. Citing to Requester 1–3's Comments, the Examiner determined the newly amended claim recitations, including the "logic element" limitation, have already been rejected in our previous Decision when addressing then existing claims 123, 128, and 129 (claims 128 and 129 are now canceled). *Id.* at 18 (citing R1 Comments 9, R2 Comments, and R3 Comments). Specifically, Requester 1 contends our previous Decision already determined Amidi and Dell 2 teach the recited "logic element" limitation. R1 Comments 7, 10–11 (citing 4th Wang Decl. ¶ 26 and Dec. 80–82, which refer to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach" (*id.* at 81)); *see also id.* at 40–43 (citing Amidi ¶ 71, Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, and 3d Bagherzadeh Decl. ¶ 37), 57–60 (citing Dell 2, 2:48–59, 8:36–41), 78–79 (citing Dell 2, 2:32–38). Requesters 2 and 3 present similar remarks. *See* R2 Comments 8–9 (discussing the similarities of the new claim amendments to claims 52, 123 (previously existed),[13] and 129 (now canceled)); *see also* R3 Comments 7–8 (discussing the previously existing claim 123).

We agree independent claim 52 and claim 123 (previously recited) included a recitation similar to the "logic element" limitation. For example, claim 52 previously recited "the logic element responds to at least a row address bit of the at least one row/column address signal, the bank address signals, and the at least one

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[13] Requester 2 cites to "RAN Claims 42." R2 Comments 8. Requester 2 states "RAN Claims" refers to "Patent Owner Response/Amendment" submitted on January 14, 2013. *Id.* at 1. Because the amendment to claim 123 is located on page 38 (RAN Claims 38), we presume Requester 2 is referring to page 38 in the comments.

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chip-select signal by generating a first number of chip-select signals of the set of output control signals." R1 App. Br., App'x A 17 (Claims App'x). Dependent claim 123 depends from claim 1 and previously recited "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals." *Id.*, App'x A 27 (Claims App'x). That is, other than the additional signal (iv) or the PLL clock signal now in claim 1 (PO Response 3), claim 1's "logic element" limitation generates chip-select signals in response to the same signals listed in previously recited claims 52 and 123.

However, when addressing Ground 5 (i.e., Amidi and Dell 2), we did not present a new ground of rejection for claim 52, 123, or 129. Dec. 78–83. Rather, we only presented a new ground of rejection for claims 52, 123, and 129 collectively based on Micron and Amidi (Ground 13). Dec. 93–99. As such, although these claims include similar subject matter to claim 1 as currently amended, we did not previously determine Amidi and Dell 2 teach or suggest the limitations found in claims 52, 123, and 129. Moreover, claim 1 previously recited the logic element "generates gated column access strobe (CAS) signals or chip-select signals . . . in response at least in part to a bank address signal" (R1 App. Br., App'x A 1) but did not recite that the CAS signals or chip-select signals were in response to bank address signals as well as signals (i), (iii), and (iv) as now recited in claim 1.

For reasons discussed below and based on the record, we agree with Patent Owner that Amidi and Dell 2 would not teach or suggest to an ordinarily skilled

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artisan the "logic element" limitation, which claims the logic element generates chip-select signals[14] in response to all four enumerated signals (i)–(iv) in claim 1.

In our previous decision, a register (e.g., 408) and a CPLD (e.g., 604) collectively were mapped to the recited "logic element." Dec. 18 (stating "we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited 'logic element.'") We analyzed whether Amidi taught or suggested a register (e.g., 408) receiving bank address signals. *See, e.g.,* Dec. 18–21, 27–34. As part of that analysis, we concluded Amidi at least suggests to an ordinarily skilled artisan some embodiments where signals other than those explicitly disclosed, including bank address signals, may be received by register 408. *See, e.g.,* Dec. 28, 30, 33.

However, as now claimed, claim 1 recites the logic element "generates chip-select signals" in response to signals (i)–(iv). In Amidi, its CPLD (e.g., 604 in Figures 6A-B)—not its registers—generates chip-select signals (e.g., rcs0a–3b). Amidi, Figs. 6A–B. Because Amidi's registers (e.g., 408, 418, and 608) do not teach or suggest "generat[ing] chip-select signals" (e.g., rcs0a–3b) and the signals Amidi's registers received do not attribute to the generated chip-select signals at Amidi's CPLD (*see* Amidi, Figs. 6A–B), Amidi's register (e.g., 408) can no longer be a component of claim 1's "logic element" limitation that generates the recited "chip-select signals" in response to signals (i)–(iv).

Amidi shows chip-select signals[15] (e.g., rcs0a–rcs3b) generated by CPLD 604 (e.g., a logic element). Amidi ¶¶ 52, 60, Figs. 6A–B. Also, Amidi teaches and

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[14] We discuss the alternatively generated, "gated column access strobe (CAS) signals" of claim 1 later in the Opinion.

[15] The '912 patent explains "rank-select signals" are "also called chip-select signals." The '912 patent 2:36–38.

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shows a row address signal (e.g., Add(n) or signal (i)) and a chip-select signal
(e.g., cs0 or cs1 or signal (iii)) are inputted into Amidi's CPLD 604. Amidi ¶¶ 49,
52, 58, 60, Fig. 6A. As such, Amidi generates chip-select signals in response to
both signals (i) and (iii) in claim 1. But, as we previously found, Amidi "fails to
describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD
410 or 604. *See* Amidi, Figs. 4A–B, 6A–B." Dec. 20; *see id.* at 36. Additionally,
we agreed with Patent Owner that "Requester 1's proposed obviousness rejections
based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a
CPLD receiving BA signals." Dec. 39.

When discussing the obviousness rejection based on Amidi and Dell 2
(Ground 5), we stated "Amidi teaches emulating a smaller memory module by
using an address signal, such as an extra row or column line, but does not
specifically discuss using a bank address line." Dec. 79; *see id.* at 79–80 (referring
to Grounds 4 and 6 for details). However, we additionally stated Dell 2's teaching
"provide[s] some evidence of generating [] chip select or rank select signals in
response at least in part to a bank address signal." Dec. 81 (referring to our
discussion of "bank address limitation in claim 7"). Notably, the "bank address
limitation in claim 7" addressed the previously recited "bank address signals of the
set of input control signals are received by both the logic element and the register"
(R1 App. Br., App'x A 4 (Claims App'x)), not the logic element generating
chip-select signals in response to signals (i)–(iv) as claim 1 now recites (PO
Response 3).

Even so, we stated "Amidi suggests other types of memory devices or
densities can be used to build the four rank memory module" (Dec. 42 (citing
Amidi ¶ 71)) and "Dell 2 teaches a technique for using various types of memory

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devices or densities other than those in Amidi, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory device. Dell 2, Abstract, claim 1." *Id.; see also id.* at 42–43 (citing Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1). We also stated "the discussion of Amidi's CPLD receiving bank address signals . . . based on Dell 2's teaching as previously discussed, does provide some evidence of generating [] chip select or rank select signals in response at least in part to *a* bank address signal." *Id.* at 81 (italics added), *quoted in* R1 Comments 10; *see id.* at 94 (stating "Amidi . . . 'at least suggests generating a chip-select signal in response in part to *a* bank address signal'") (emphasis added), *quoted in* R3 Comments 11. These discussions do not address Amidi's and Dell 2 generating chip select signals in response to signals (ii) or "the bank address signal*s*" as now recited.

The previous Decision also states "Dell 2 provides a teaching or suggestion to direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1)." *Id.* at 81–82 and *see also* 4th Wang Decl. ¶ 26, *cited in* R1 Comments 11. Requester 2 also states Dell 2 discloses the bank address signals of the "logic element" limitation and one skilled in the art would have recognized generating a CAS or chip-select signal in response to a bank address signal in order to ensure the correct bank is addressed. R2 Comments 9–10 (citing 4th Bagherzadeh Decl. ¶ 10[16], which cites Dell 2, 8:29–44).

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[16] Requester 2 provides no paragraph number. For purpose of this decision, we presume Requester 2 is referring to paragraph 10.

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Specifically, Dell 2 teaches a logic circuit (e.g., a switch circuit) that performs a remapping function (e.g., 50) of at least one address signal (e.g., A12) to an additional bank address signal (e.g., BA1) at CAS time to ensure the correct *bank* is addressed. Dell 2, 2:32–37, 49–51, 8:20–40, Fig. 1A. Thus, based on Dell 2's teachings or suggestions and what one skilled in the art would have recognized, we agree with Requester 1 (R1 Comments 10–11), Dr. Wang (4th Wang Decl. ¶ 26), Requester 2 (R2 Comments 9–10), and Dr. Bagherzadeh (4th Bagherzadeh Decl. ¶ 10) that one skilled in the art would have recognized using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank* during bank expansion (e.g., generate *bank-select* signals in response to bank address signals).

Although this discussion addresses why bank address signals may be received by a CPLD, this reasoning does not sufficiently address why one skilled in the art would have recognized a CPLD, like Amidi's, (e.g., a logic element) generates *chip-select* signals in response to received bank address signals and the other recited signals (i.e., signals (i), (iii), and (iv) recited in claim 1. That is, having a logic element specifically generate "rank-selecting signals . . . in response to" bank address signals in combination with signals (i), (iii), and (iv) as now claim 1 presently recites does not follow from the above teaching to generate signals for *bank* selection. Nor does the current record sufficiently establish that one skilled in the art would have recognized applying Dell 2's bank expansion technique to Amidi's rank expansion process, such that the combination suggests the "logic element" limitation recited in claim 1. Moreover, even assuming, without deciding, one skilled in the art would have recognized to apply such a regime to Amidi's rank expansion process, the teachings would at best suggest

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using one stored bank address signal—not bank address signals or signals (ii) required in claim 1—to generate chip-select signals.

The above-discussed teachings are inadequate to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal and bank address signals as recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 25 (stating "[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal"), 26 (stating "[t]here is no suggestion to repurpose a bank address signal for rank multiplication purposes."). Thus, in view of the record as it currently stands, we have reconsidered and withdraw our statement in the previous Decision that combining Dell 2's teaching with Amidi "would have predictably yielded" the logic element receiving bank address signals "so that the necessary rank chip select signals discussed in Amidi are produced" (*id.* at 43) as well as any other similar statements.

We additionally referred to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach." *Id.* at 81; *see also id.* at 82 and R1 Comments 23 (citing Dec. 81–82). For example, we discussed Dell 2 teaches "storing signals for later use, including during a column access procedure[], to ensure the correct bank is addressed." Dec. 59; *see also id.* at 80. As explained above, this teaching in Dell 2 does not teach or suggest sufficiently to one skilled in the art a "logic element" limitation generating *chip-select* signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

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Claim 1's "logic element" limitation alternatively recites generating "gated column access strobe (CAS) signals . . . in response at least in part to (i) row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal." PO Response 3. Amidi's CPLD 604 does not teach or suggest generating a CAS signal. *See* Amidi, Fig. 6A. Instead, CAS signals enter (e.g., CAS) and exit (e.g., rCAS) register 608. *See id.* Granted, Amidi's register 608 receives row address signals (e.g., Add[n-1:0]), bank address signals (e.g., BA[1:0]), and PLL signals (e.g., CLK0, CLK0_N). *See id.* ¶ 50, Fig. 6A. Yet, Amidi does not describe how the rCAS signal is generated. *See id.* Moreover, Amidi does not teach or suggest register 608 receiving chip-select signals (i.e., signal (iv) in claim 1) or operates as a logic element to generate gated CAS signals as recited. *See id.* As such, Amidi does not teach and suggest the "logic element" limitation in claim 1.

Additionally, Dell 2 does not teach or suggest the above missing feature. As explained above, Dell 2 teaches or suggests storing a bank address signal for use with a logic element (e.g., ASIC 24) during CAS time. Dell 2, 8:29–40, 9:32–34. Yet, there is no discussion of generating a CAS signal in response to signals (i) through (iv) as recited in claim 1. In particular, Dell 2 fails to teach or suggest generating a CAS signal in response to a chip-select signal (i.e., signal (iii)). Nor do we find Dr. Wang's testimony persuasive in teaching or suggesting generating a CAS signal in response to a chip-select signal. *See* Dec. 80–81 (citing 3d Wang Decl. ¶¶ 10–16). On the record, we therefore determine Amidi and Dell 2 collectively do not teach or suggest sufficiently to one skilled in the art the "logic element" limitation generating CAS signals in response to both a row address

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signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Lastly, Requester 1 points out Dr. Sechen's statement in paragraph 26 regarding "the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers." 2d Supp. Sechen Decl. ¶ 26, *cited in* R1 Comments 11. We agree with Requester 1 that claim 1's "logic element" limitation as currently recited requires the logic element to receive both a row address signal *and* bank address signals. *See* PO Response 3. From this perspective, Dr. Sechen's statement is confusing. *See* R1 Comments 11. Yet, when focusing on the recitation "the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element" in claim 1 (PO Response 3), Dr. Sechen's testimony is consistent with claim 1's recitation requiring the logic element to receive a separate or different row/column address signal from the row/column address signals entering the register. *See* 2d Supp. Sechen Decl. ¶ 26.

Independent claims 15, 28, and 39 each recite a similar "logic element" limitation to claim 1, which generates gated CAS signals or chip-select signals in response to signals (i) through (iv), including both a row address signal and bank address signals. PO Response 11, 18, 23–24. For the above reasons, we determine Amidi's and Dell 2's teachings are inadequate to teach or suggest the "logic element" limitation in these claims.

Upon reconsideration of the record, we withdraw the rejection of claims 1, 15, 28, and 39 and dependent claims 3, 4, 6, 8, 10–14, 18–20, 22, 24, 27, 29, 31,

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32, 34–38, 40, 41, 43, 45–50, 120, 122, and 132–136, which variously depend
from claims 1, 15, 28, and 39, based on Amidi and Dell 2.

B. Amidi, Dell 2, and JEDEC 21C

The rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32,
34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90,
91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and
JEDEC 21-C was newly proposed by Requester 1 in its comments. R1 Comments
12–77. The Examiner adopted this proposed rejection. Ex. Deter. 11.
Specifically, concerning the "logic element" limitation found in independent
claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58, Requester 1
proposes a similar mapping and reasoning for combining Amidi with Dell 2 to
teach or suggest this recitation. *See, e.g.,* R1 Comments 23. Requester 1 adds
JEDEC 21-C teaches or suggests transmitting PLL clock signals to a CPLD and,
and when combined with Amidi, generating its output control signals (e.g., rank-
selecting or chip-select signals) in response to a PLL signal for clocking additional
devices on a DIMM. *See* R1 Comments 22 (citing JEDEC 21-C, pp. 38–43), 23.
In essence, based on JEDEC 21-C's teaching, Requester 1 states one skilled in the
art would have known or recognized modifying Amidi so that the clock signals
comes Amidi's PLL 606 (e.g., PLL clock signals) rather than memory connector
602 for clocking DIMM devices. *See id.* at 22–23. This modification, in turn,
generates chip-select or rank-selecting signals in response to a PLL clock (i.e.,
signal (iv)) as recited. *See id.*

Yet, JEDEC 21-C's teaching is not relied upon and does not cure the
above-noted deficiencies in Amidi and Dell 2—namely the "logic element"
limitation generates gated CAS, chip-select or rank-selecting signals in response to

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both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv). We refer above for more details.

Accordingly, we withdraw the adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C.

C. *Amidi and Dell 184* (Ground 20)

In our May 31, 2016 Decision, claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 (canceled claims omitted) are rejected under 35 U.S.C. § 103 based on Amidi and Dell 184. Dec. 91–93. Independent claims 52, 67, 77, 82, and 87 include similar recitations to the "logic element" limitation in claim 1 that generates rank-selecting or chip-select signals in response to signals (i) through (iv). *Compare* PO Response 27, 33, 36, 38, and 41 *with id.* at 3. Notably, claims 52, 57, 77, 82, and 87 exclude the alternative recitation of generating a gated CAS signal. *Id.* at 27, 33, 36, 38, and 41.

Our rationale for rejecting these claims based on Amidi and Dell 184 was similar to that proposed for Amidi and Dell 2. Specifically, we noted in the opinion

> The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48-3:5, claim 1, a[n]d Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the

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> desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal . . . .

Id. at 92–93.

Similar to that noted above when addressing Dell 2, Dell 184 in combination with Amidi may provide a reason why bank address signals may be received by a CPLD, but does not sufficiently address why one skilled in the art would have specifically recognized Amidi's CPLD (e.g., a logic element as recited in claim 52) generates *chip-select* or *rank-selecting* signals in response to signals (i)–(iv) as recited in claims 52, 67, 77, 82, and 87. We refer above for more details.

Requester 2 asserts Patent Owner provided no argument related to the patentability of the claims rejected based on Ground 20 and relied upon the arguments presented for Micron and Amidi. *See* R2 Comments 10 (stating "Patent Owner did not provide any individual analysis concerning the patentability of those claims in view of this rejection, but rather relied on its analysis for the rejections under Micron and Amidi."). We disagree.

Patent Owner states "[t]hese amendments [to the claims presented after the previous Decision] distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV." PO Response 56. In "Section IV" of the declaration, Dr. Sechen discusses the similarities between the teachings of Dell 184 and Dell 2 and further articulates how Dell 184 does not use bank address inputs for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 38, 40–42. As such, when stating "as discussed above" (PO Response 56), Patent Owner was referring to the rejection of Amidi and Dell 2 and not Micron and Amidi as argued.

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Accordingly, we withdraw the rejection of claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184.

D. Micron and Amidi (Ground 13)

In our previous Decision, we determined claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 (canceled claims omitted) were obvious over Micron and Amidi. Dec. 93–99. For this rejection, Patent Owner reasserts Amidi does not use both bank address signals and row address signal for rank multiplication or for generating chip-select signals/CAS signals. PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30). As to whether one skilled in the art would be motivated to use bank address signals for proper operation of chip select signals, Patent Owner contends "this is a conclusion of fact and not an indication of what a POSITA[17] would recognize." Id. at 55 (citing 2d Supp. Sechen Decl. ¶¶ 32–33); see also id. at 55–56 (citing 2d Supp. Sechen Decl. ¶¶ 34–35). Patent Owner argues combining Micron and Amidi to arrive at the claimed invention as amended would not be obvious to one skilled in the art. Id. at 56. For reasons discussed below, we are persuaded Micron and Amidi do not teach or suggest the newly recited "logic element" limitation in claim 1 or similar independent claims.

At the outset, we address Patent Owner's argument that Dr. Kozyrakis's testimony represents how an expert—not an ordinarily skilled artisan—would have understood Amidi and that Amidi, which does not teach using bank signals to generate chip-select or CAS signals for rank expansion, is representative of what one skilled in the art would have understood. Id. at 54–55 (citing 2d Supp. Sechen Decl. ¶¶ 31–32). We agree with Requester 3 that Dr. Kozyrakis's testimony is

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[17] "POSITA" stands for a person of ordinary skill in the art.

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from the point of view of what an ordinarily skilled artisan would have known or recognized. *See* R3 Comments 12 (citing Kozyrakis Decl. ¶ 8, 2d Kozyrakis Decl. ¶¶ 12–14, 3d Kozyrakis Decl. ¶¶ 9–11, 4th Kozyrakis Decl. ¶¶ 12–14). For example, Dr. Kozyrakis testifies that one of ordinary skill in the art (e.g., two or more years of professional experience in memory design)[18] would have an understanding of "the latest memory devices," including DDR, DDR-2, and DDR-3 devices, and "the number of rows, columns, banks, and input/output bits of each device." 2d Kozyrakis Decl. ¶ 14, 3d Kozyrakis Decl. ¶ 11, and 4th Kozyrakis Decl. ¶ 14. On the other hand, we also agree with Patent Owner that "Amidi is representative evidence of what a POSITA would understand." PO Response 55; *see also* Dec. 27 (stating Amidi "reflects the appropriate skill level at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).").

Next, the amendments to independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58 have been made to include the "logic element" limitation that generates gated CAS, chip-select, or rank-selecting signals in response to four enumerated signals, signals (i) through (iv). *See* PO Response 2–3, 10–11, 17–18, 22–27, and 29–41. As stated above when addressing Ground 5, Amidi does not teach to an ordinarily skilled artisan using bank address signals to generate CAS signals or chip-select signals. *See also* Dec. 95 (stating "these

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[18] Our previous Decision established that one of ordinary skill in the art "is a person with (1) at least an undergraduate degree in either electrical engineering, computer engineering, or in a closely related discipline and (2) at least two years of experience in designing computer memory systems. This ordinarily skilled artisan would also have familiarity with and understanding of (1) JEDEC standards related to memory devices and modules, such as DDR SDRAM devices and DIMMs, and (2) the latest DRAM memory devices in the market." Dec. 26–27.

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passages in Amidi do not discuss using a *bank* address bit to generate the chip-select signals.") (referring to Amidi ¶¶ 43–44, 52). However, we previously noted "Amidi suggests other types of memory devices or densities can be used to build [its] four rank memory module." Dec. 42 (citing Amidi ¶ 71); *see also* Amidi ¶¶ 10–12, *cited in* Dec. 96. We therefore turned to what "an ordinarily skilled artisan would have recognized regarding bank address signals, as well as other signals, in the context of memory modules." Dec. 95.

> In referring to "our previous discussion," (*id.*), we stated
>
> Amidi, when accounting for inferences and creative steps that a person of ordinary skill in the art would have employed, at least suggests generating a chip-select signal in response in part to a bank address signal. For example, Requester 3's *second case* of using a spare bank address signal to generate the proper chip-select signals for rank multiplication as taught by Amidi is similar to our previous discussion of the collective teachings suggest a CPLD receiving a bank address signal.

Id. at 94–95. For example, Dr. Kozyrakis stated one skilled in the art would have recognized different generation of DDRs (e.g., DDR-1, DDR-2, and DDR-3) and that some DDR-2 devices have an extra bank address field (e.g., 3 bits rather than the conventional 2 bits). *Id.* at 61–62 (citing Kozyrakis Decl. ¶ 26); *see also* 3d Kozyrakis Decl. ¶¶ 22–25. We then concluded this provides evidence that one skilled in the art would have recognized or known a bank address signal is free in certain DDR devices to assist in creating the desired rank expansion for certain memory modules. *See id.* at 62; *see id.* at 65–66 and 98.

> In particular, we stated:
>
> [L]ike Amidi's teaching of using an extra row/column address bit for generating the proper chip-select signals (e.g., rank expansion) for

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> emulating a two rank memory module (Amidi ¶¶ 51, 59), Dr. Kozyrakis provides a reason with some rational underpinning that an ordinary skilled artisan would have used other known, extra address bits (e.g., the extra bank address in more recent DDR devices) to create the desired rank expansion in Amidi by directing such extra signals to Amidi's CPLD.

Id. at 62. We maintain our position that the record provides a reason with a rational underpinning to use *a* free signal—whether a row address or a bank address signal—to achieve desired rank expansion. Despite Patent Owner asserting this "second case" no longer applies "to the amended claims" (PO Response 54), neither Patent Owner nor Dr. Sechen's testimony (2d Supp. Sechen Decl. ¶ 29) sufficiently explains why this scenario no longer pertains to the amended claims or why bank signals cannot be used by both the registers and a logic element. *See* R3 Comments 10.

Additionally, in the previous Decision, we noted Amidi uses an extra row or column address signal as an input to the CPLD to generate chip-select signals and uses a column address signal (e.g., A11) for multiple purposes. Dec. 63–64 (citing Amidi ¶¶ 50–52, 57–60, Figs. 6A–B). Based on Amidi's teaching, we concluded an ordinary skilled artisan having two years of experience in logic circuit design would have recognized to use address signals in an unconventional manner and for multiple purposes. We additionally found Requester 3 provides adequate evidence that one skilled in the art would have recognized using bank address signals in a manner similar to the row and column address signals, some of which are received by Amidi's CPLD. *Id.* at 64, 66. Yet, the evidence of record does not teach or suggest generating the specifically recited chip-select signals using more than one bank address signal and, more particularly, both bank address

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signals (i.e., signals (ii)) and a row address signal (i.e., signal (i)) as well as signals (iii) and (iv) claimed in claim 1.

Requester 3 offers yet another reason for a logic element to generate chip-select signals in response to both multiple bank address signals and a row address signal. *See* Dec. 96–97 (citing R3 App. Br. 7–10, R3 Reb. Br. 2, 4, 3d Kozyrakis Decl. ¶¶ 17–19, 4th Kozyrakis Decl. ¶¶ 15–25, and Amidi ¶ 61). In particular, Requester 3 stated previously (*see* R3 App. Br. 10) and now (*see* R3 Comments 13) "[b]ecause the extra row address bit [used during row address time] is unavailable at column address time, the rank-multiplying module must store information from row address time for use during column access time." R3 Comments 13 (citing 3d Kozyrakis Decl. ¶ 19). According to Requester 3, "[i]nput bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals at column address time. Kozyrakis Decl. III ¶ 19." R3 Comments 13; *see also* R3 App. Br. 7. Requester 3 thus asserts chip-select signals are generated in response to both a row address signal and bank address signals

> because the input bank address signals are used to select the previously stored "highest [row] address number Add(n)" needed to generate the chip-select signals matching those generated at RAS time. In other words, the CPLD 604 would generate chip-select signals based on the stored row address bit, which is selected based on the input bank address signals from the memory controller.

R3 App. Br. 10, *quoted in* Dec. 97.

Turning to Amidi, this reference teaches CPLD 410's circuitry for row address decoding and column address decoding (e.g., row address time and column address time) differs. Amidi ¶ 61. Amidi states the "Row

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address" cycle and "the Column address" cycle need to be provided with "the proper control and command signals" but fails to provide any specifics related to which control and command signals are provided during these cycles. *Id.* Nor does Amidi show or suggests bank address signals entering CPLD 604 during row address or column address decoding. *See id.*, Figs. 6A–B; *see also* PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30).

Concerning row and column address time, Dr. Kozyrakis states an ordinary artisan would have known of alternative scenarios from Amidi where the logic element can decode or pre-process the one row address bit, store the resulting signals from decoding or pre-processing, and then use the stored, resulting signals during column access operations "to generate chip-select signals or the bank address field." 2d Kozyrakis Decl. ¶ 18(d)(ii); *see also id.* ¶ 33. In this scenario, decoded or pre-processed signals—not bank address signals—are used during column access time to generate chip-select signals. Dr. Kozyrakis further states "bank address are not always necessary in order to determine the output control signals for the lower density memory devices," such as in Amidi. 2d Kozyrakis Decl. ¶ 23. As such, Dr. Kozyrakis's testimony conflicts with Requester 3's position that bank address signals *are necessary* (R3 Comments 13) to generate the chip-select signals during column access time.

Nevertheless, Dr. Kozyrakis also asserts an "obvious way to know which of the two banks has the proper row open" during subsequent CAS commands is to store the address bit (e.g., A_{13}) and to reuse the stored address bit to identify the correct pair of banks (e.g., reuse as a bank address signal). *See* 3d Kozyrakis Decl. ¶¶ 18–19. Notably, Dr. Kozyrakis does not

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discuss how the stored address bits are located during subsequent CAS commands (*see id.*), such as by using bank address signals as Requester 3 asserts (R3 Comments 13).

To elaborate, Dr. Kozyrakis testifies that a memory module's controller must identify which bank should receive the CAS command using bank address and chip-select signals. 3d Kozyrakis Decl. ¶¶ 17–18. Dr. Kozyrakis also states the incoming bank address and chip-select signals from a memory controller are not sufficient for certain rank-multiplying modules. *Id.* ¶ 18 (discussing "the case where the originally specified module uses two ranks of 512Mbit DDR2 devices [having four banks] and the rank-multiplying module uses four ranks of 256Mbit DDR2 devices [having four banks]."). Specifically, during a RAS command to a bank in a 512Mb device, Dr. Kozyrakis states a rank-multiplying module designer would use bank address and chip-select signals to identify a bank pair from eight banks and would use a free address bit (e.g., A_{13}) to identify which of the two banks in the bank pair will receive a command. *Id.* ¶ 19.

During a subsequent CAS command, Dr. Kozyrakis further states the memory controller does not provide the free address (e.g., A_{13}) bit to identify the correct bank in the bank pair. *Id.* Thus, Dr. Kozyrakis states an obvious way to identify the correct bank in a pair with the proper row open is to store the address bit of the last RAS command (e.g., A_{13}) and to reuse the stored address bit. *Id.* However, unlike Requester 3's assertion that bank address signals are used to identify this stored address bit (R3 Comments 13), Dr. Kozyrakis does not additionally testify the incoming bank address signals are used to identify the stored address bit. 3d Kozyrakis Decl. ¶ 19.

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Instead, Dr. Kozyrakis states "the module must have a total of 8 bits of storage for A_{13} address bits" without discussing how the proper address bit is identified. *Id.*

Dr. Kozyrakis's testimony in his fourth declaration also cited by Requester 3 (R3 Comments 13) does not further explain or address how stored address bits are identified—namely, whether or not using bank address signals are used. *See, e.g.*, 4th Kozyrakis Decl. ¶¶ 15–25, *cited in* R3 Comments 13. Similarly, Dr. Bagherzadeh also states storing the extra address bit is "a standard feature in transparent memory modules like the embodiments disclosed in Amidi" and the circuit "will be unable to identify the correct chip to access during the column access procedure" if the extra bit is not stored. 2d Bagherzadeh Decl. ¶ 22. But, once again, Dr. Bagherzadeh does not explain how the stored address bit is later identified.

Granted, Dr. Kozyrakis and Dr. Wang point to references in asserting one skilled in the art would have known to store some address bits for each bank in a logic device and use them later during column commands. 4th Kozyrakis Decl. ¶ 24 (citing Olarig); *see* 3d Wang Decl. ¶ 10 (citing Dell 2). Nevertheless, Olarig and Dell 2 form no part of this rejection based on Micron and Amidi and thus are not persuasive. Moreover, these references do not teach or suggest using bank address signals later to identify the stored bits.

Moreover, to the extent Dr. Kozyrakis's testimony does suggest bank address signals are used to identify the stored bits, this position clashes with his earlier testimony stating

> bank address signals must be used as one of the inputs for the
> calculation of the output chip-select signals *only if* the number of

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> banks in the memory devices used in the lower cost memory module
> is *smaller* than the number of banks in the memory devices in the
> originally specified module. In all other cases, the bank address
> signals can be simply clocked through the logic element . . . without
> further processing.

2d Kozyrakis Decl. ¶ 23 (italics added). In the example provided in the third
declaration (3d Kozyrakis Decl. ¶¶ 18–19), the bank number of the lower
cost memory module's memory devices (e.g., 256Mb devices having four
banks) is not smaller than the originally specified module's memory devices
(e.g., 512Mb devices also with four banks), implying that bank address
signals will only be clocked through the logic element. *See id.*
Additionally, Dr. Kozyrakis states the bank address signals "must be used as
one of the inputs for the calculation of the output chip-select signals" (2d
Kozyrakis Decl. ¶ 23 (italics added)) when the bank number in the lower
cost memory module is smaller than the bank number of the originally
specified module, suggesting at most one bank address signal—instead of
bank address signals (i.e., signals (ii))—is used.

Thus, Requester 3's assertions that Amidi's "CPLD 604 would
generate chip-select signals based on the stored row address bit, *which is
selected based on the input bank address signals from the memory
controller*" (R3 App. Br. 10) (emphasis added) is not corroborated
adequately with Dr. Kozyrakis's testimony. Likewise, Requester 3's
conclusion that it would have been obvious to an ordinarily skilled artisan to
generate chip-select signals in response to both a row address signal and
"input bank address signals during column address time, because the input
bank address signals must be used to identify the stored row address bit

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required to generate the chip select signals" (*see* R3 Comments 13; *see also* R3 App. Br. 7) is not corroborated sufficiently by Dr. Kozyrakis.

Additionally, Dr. Sechen provides countering evidence and arrives at the opposite conclusion of Requester 3. 2d Supp. Sechen Decl. ¶¶ 22 (citing Sechen Decl. ¶ 23, 2d Sechen Decl. ¶¶ 14–15), 29 (citing "Section II"). Specifically, Patent Owner and Dr. Sechen focus on Amidi and assert this reference demonstrates what one skilled in the art would have recognized. PO Response 55. Patent Owner and Dr. Sechen state Amidi provides no recognition to one of ordinary skill that bank address signals are necessary for generating chip-select signals. 2d Supp. Sechen Decl. ¶¶ 33, 35; PO Response 54–55. Dr. Sechen further states Amidi does not recognize generating chip-select signals using both the bank address signals and a row address signal as recited in claim 1 for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 29, 31, 32; *see also* PO Response 55. Dr. Sechen testifies additionally Amidi and Micron do not teach using bank address signals to generate rank or chip-select signals and that using the bank address signals in this manner would not have been known by one of ordinary skill based on Micron and Amidi. Sechen Decl. ¶¶ 35, 37. Patent Owner and Dr. Sechen argue one skilled in the art "would conclude that Amidi is operative without bank address signals for generating control signals." 2d Supp. Sechen Decl. ¶ 33; *see also* PO Response 55.

As previously noted, we agree that Amidi provides evidence of what one skilled in the art would have known or recognized at the time of the invention. *See Okajima*, 261 F.3d at 1355. As such, we agree with Dr. Sechen that one skilled in the art "would conclude that Amidi is operative without bank address signals for

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generating control signals," and thus a memory module's logic element (e.g., Amidi's CPLD) can generate chip-select signals without using bank address signals. *See* 2d Supp. Sechen Decl. ¶ 33. Although an obviousness "analysis need not seek out precise teachings" and we further consider an ordinarily skilled artisan's background knowledge (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)), Dr. Kozyrakis's testimony and Requester 3's articulated reason that bank address signals are known to be used to identify the row address signal, which in turn is used generate chip-select signals, lacks sufficient corroborating evidence to provide a rational underpinning to support an obviousness conclusion. *See id.*

Lastly, Requester 3 notes that claims 52, 123, and 129 recite similar limitations to claim 1 (excluded a PLL clock signal (i.e., signal (iv)) and were addressed in our previous Decision. R3 Comments 8–9. We acknowledge claims 52, 128, and 129 were previously rejected based on Micron and Amidi. Dec. 93–99. However, the specific limitations found in claims 52, 128, and 129 similar to the "logic element" limitation in claim 1 as now amended were not disputed in Requester 3's brief. For example, regarding claim 52, Requester 3's arguments referred back to claim 1 as previously recited (*see* Dec. 98 (citing R3 App. Br. 12 (stating "[a]s discussed above, it would have been obvious for the chip-select signals generated as CAS time to be generated based on *an* input bank address") (italics added))), which did not include the "logic element" limitation found in claim 1 as now amended.

Upon reconsideration of claim 1 as now amended, we withdraw our conclusion of obviousness for these claims based on Micron and Amidi. We also withdraw the remarks made in our previous Decision concerning one skilled in the art would have recognized using bank address signals for generating chip-select

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signals (*see* Dec. 96–97), in view of the above discussion. Weighing all the evidence in the record, we determine one skilled in the art would not have recognized using a known logic element, such as Amidi's, to generate chip-select signals in response to a row address signal (i.e., signal (i)), multiple bank address signals (i.e., signals (ii)), a chip-select signal (i.e., signal (iii), and a PLL clock signal (i.e., signal (iv)) as recited in claim 1.

Regarding the logic element alternatively generating gated CAS signals in response to signals (i) through (iv) as recited in claim 1 (PO Response 3), there is insufficient evidence to support such CAS signals are generated in response at least in part to these signals. *See* R3 Comments 11–13 (focusing on generating chip-select signals); *see also* 3d Kozyrakis Decl. ¶¶ 16–19, 22–25 (discussing receiving a CAS command and generating chip-select signals) and 4th Kozyrakis Decl. ¶¶ 22–24 (same). As discussed above, Amidi's CPLD 604 does not teach or suggest generating a CAS signal but rather a CAS signal entering (e.g., CAS) and exiting (e.g., rCAS) register 608. *See* Amidi, Fig. 6A. Amidi also does not (a) describe how the rCAS signal is generated or (b) teach or suggest chip-select signals entering register 608. *See id.* ¶ 50, Fig. 6A. Micron similarly does not disclose or teach how gated CAS signals are generated. *See* Micron 5–8.

For the above reasons, we withdraw our rejection of claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Micron and Amidi.

E. *Micron, Amidi, and Olarig* (Ground 21)

Above, we stated Requester 3 provided insufficient evidence to support the assertion that bank address signals are necessary for generating

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gated CAS/chip-select signals or that one skilled in the art would have recognized using both a row address signal and bank address signals as well as signals (iii) and (iv) for this purpose. Unlike Ground 20, Olarig is also being relied upon in Ground 21. Thus, Dr. Kozyrakis's testimony concerning storing some address bits for each bank in a logic device and using them later during column commands illustrates storing and reusing an address bit for a later operation is known to an ordinary skilled artisan. 4th Kozyrakis Decl. ¶ 24 (citing Olarig). But, this teaching does not further illustrate using bank address signals to identify the stored row address bit as Requester 3 asserts. *See* R3 Comments 13.

> Nevertheless, as indicated in our previous Decision,
>
> Olarig teaches combining a bank address signal with a column address bit. Olarig 22:49-51. As such, there is a teaching to use a bank address signal (e.g., an input bank address signal) with an address signal to generate another output signal during a read/write command. *Id.* Granted, there is no discussion in Olarig that this generated signal is a chip-select or rank-selecting signal as recited. *Id.* But, we agree with Requester 3 that this teaching in Olarig illustrates using bank address signals to generate other control signals was known. *See* R3 App. Br. 18-19.

Id. at 100. We then concluded "Olarig teaches combining address signals, including a bank address signal, to generate another control signal, and artisans armed with Olarig's and Amidi's teachings and employing their background knowledge, would have recognized using a bank address signal to generate other control signals, such as chip-select signals." *Id.* at 101.

This analysis indicates an ordinary artisan would have recognized to combine address signals with *a* bank address signal to generate control signals. But, even this teaching falls short of suggesting generating a control

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signal, such as a chip-select signal, in response to both at least one row address signal (e.g., recited signal (i)) and bank address *signals* (i.e., signals (ii)) recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 46–48. Granted, we also concluded "when combined with Amidi's teachings, the collective teachings suggest that an ordinarily skilled artisan would have recognized generating a chip-select signal in response at least in part to bank address signal*s.*" *Id.* at 100–101 (italics added). In light of the record before us now, we no longer conclude Amidi, Dell 2, and Olarig collectively teach or suggest combining multiple bank address signals with a row address signal as well as signals (iii) and (iv) to generate chip-select (or gated CAS signals for that matter).

Requester 3 asserts Patent Owner relies on "Section IV," which is directed to the rejection based on Micron and Amidi, and does not address Olarig. R3 Comments 13. For this reason, Requester 3 argues Patent Owner fails to show the claims rejected based on Micron, Amidi, and Olarig are unobvious. *Id.*

Patent Owner refers to its previous discussion when address the rejection based on Micron, Amidi, and Olarig. PO Response 56–57. As noted above, based on the record, we are persuaded that Micron and Amidi do not sufficiently demonstrate the "logic element" limitation found in the independent claims as now amended. We refer above for more analysis. Patent Owner also refers to "Second Supp. Sechen Decl. Section V" (*id.* at 57), which discusses Olarig. *See* 2d Supp. Sechen Decl. ¶¶ 45, 48–52. We thus disagree with Requester 3 that Patent Owner does not address Olarig in its remarks.

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In "Section V" of the declaration, Dr. Sechen notes our previous Decision stating Olarig teaches combining a bank address signal with a column address bit to generate an output signal. 2d Supp. Sechen Decl. ¶ 45. Dr. Sechen further asserts that one skilled in the art would not reach the conclusion that Amidi and Olarig teach the claims as now amended. *Id.* ¶¶ 46–48. Although we disagree with Dr. Sechen that one skilled in the art would not recognized using a bank address signal to generate chip-select signals (*see id.*) for reasons previously stated, we agree that Amidi and Olarig alone or in combination with Micron do not suggest generating gated CAS, chip-select, or rank-selecting signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv) as now recited in claim 1. Requester 3 provides no rebuttal to Dr. Sechen's testimony. *See* R3 Comments 13.

For the above reasons, we withdraw our rejection of claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Micron, Amidi, and Olarig.

F. Proposed Rejections based on Micron, Amidi, and Additional References

In the earlier Decision, we did not reach the proposed rejections set forth in Ground 19 (Micron, Amidi, Dell 2, and JEDEC 79C) and Ground 22 (Micron, Amidi, Olarig, and Memory Explained[19]). Dec. 101.[20] Based on the amendments

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[19] *HP Printer Memory Explained* 1-7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained).

[20] We mistakenly included Grounds 7 and 20 in Section (III)(4)'s heading. Dec. 101. Ground 7 was addressed in the previous Decision, indicating that the Examiner determined there was no substantial new question (SNQ) of patentability for this proposed rejection. *Id.* at 83–84. Further, as discussed above in Section (III)(C), Ground 20 was also addressed. *Id.* at 90–93.

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to claims 1, 15, 58, 67, 77, 82, and 87 and our withdrawal of the other grounds, we now consider the Examiner's decision not to adopt these proposed rejections.

Specifically, the Examiner did not adopt the following proposed rejections:

Reference(s)	Basis	Claims (canceled claims omitted)	
Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)	§ 103	1, 15, 28, 39, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136	RAN 14–15; R3 App. Br. 13
Micron, Amidi, Olarig, and Memory Explained (Ground 22)	§ 103(a)	56	RAN 15

1. Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19)

Above, we addressed the rejection of Micron and Amidi in Section (III)(D), concluding that one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as now recited in claims 1, 15, 58, 67, 77, 82, and 87. We additionally addressed rejections based on Amidi and Dell 2 (Section (III)(A) and Amidi, Dell 2, and JEDEC 21-C (Section (III)(B)), also concluding one skilled in the art would have not recognized based on the references' teachings a logic element generates gated CAS signals, chip-select or rank-selecting signals in response to signals (i)–(iv) as now recited. We refer above for more details.

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As discussed in the context of the rejection of Amidi and Dell 2 (Ground 5), Dell 2 does not teach or suggest the missing feature of using both signal (i) and signals (ii) to generate gated CAS, chip-select, or rank-selecting signals as now recited in claims 1, 15, 52, 58, 67, 77, 82, and 87. We refer above for more details.

Regarding JEDEC 79C, Requester 3 does not explain how this reference is being relied upon in its Appeal Brief. *See* R3 App. Br. 13–17. Moreover, the cited comments, submitted August 29, 2011, in the Appeal Brief do not address JEDEC 79C. *Id.* at 14 (citing pages 18 and 19). As for Appendix L also cited in the Appeal Brief, (*id.*), the proposed rejection discusses how JEDEC 79C teaches a read operation reads from the row selected by the preceding activate command on the same bank. Requester 3's August 29, 2011 Comments, App'x L, p. 1 (addressing claim 52). Yet, this teachings do not suggest the missing feature of generating gated CAS signals or chip-select signals in response to both a row address signal (i.e., recited signal (i)) and bank address signals (i.e., recited signals (ii)). *See id.*, App'x L, pp. 1–2. We thus determine Requester 3 has not sufficiently demonstrated how JEDEC 79C teaches or suggests the claimed features missing from Micron, Amidi, and Dell 2.

Accordingly, we determine the Examiner has not erred in not adopting the proposed rejection of claims 1, 15, 28, 39, 52, 54, 56, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 (canceled claims omitted) based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19).

2. *Micron, Amidi, Olarig, and Memory Explained* (Ground 22)

Above, we addressed the rejection of Micron, Amidi, and Olarig in Section (III)(E), concluding that one skilled in the art would have not recognized based on

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the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as recited in claims 1, 15, 28, 39, 52, and 58.

As for Memory Explained, the Examiner stated and we agree that this reference, even when combined with Micron, Amidi, and Olarig, does not teach or suggest generating CAS or chip-select signals in response to bank address signals (i.e., signals (ii)) as well as recited signals (i), (iii), and (iv). RAN 58–69. Requester 3 does not rebut this determination. R3 App. Br. 19 (asserting Micron, Amidi, and Olarig teach these features). In particular, Requester 3 turns to Memory Explained to teach the features recited in dependent claim 56, not the features in independent claim 52. *See* Requester 3's February 13, 2013 Comments 24–25, App'x S.

For the above reasons, we determine the Examiner has not erred in not adopting the proposed rejection of claim 56 (as well as claims 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131)[21] based on Micron, Amidi, Olarig, and Memory Explained (Ground 22).

V. CONCLUSIONS

We withdraw the following rejections maintained or adopted by the Examiner.

(1) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5).

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[21] Despite including only claim 56 in our previous Decision (Dec. 69), Requester 3 appealed the Examiner not adopting the rejection of claim 56 as well as the remaining claims listed above. R3 App. Br. 19–22.

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(2) Claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Amidi and 184 (Ground 20).

(3) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Amidi, Dell 2, and JEDEC 21-C.

(4) Claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Micron and Amidi (Ground 13).

(5) Claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Micron, Amidi, and Olarig (Ground 21).

We further affirm the Examiner's decision not to adopt the rejection of certain claims based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19) or Micron, Amidi, Olarig, and Memory Explained (Ground 22), previously not reached.

Based on our previous Decision, we note the following rejections are affirmed.

(1) Claim 9 and 33 is rejected under 35 U.S.C. § 102 based on Amidi. Dec. 11, 13, 23.

(2) Claims 2, 5, 7, 9, 21, 23, 30, 33, 57, and 119 are rejected under 35 U.S.C. § 103 based on (a) Amidi or (b) Amidi and JEDEC. Dec. 12–13, 39, 57.

(3) Claims 2, 5, 7, 9, 21, 23, 26, 30, and 33 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 12–13, 43, 60.

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(4) Claims 7, 9, 21, 26, 33, and 57 are rejected under 35 U.S.C. § 103 based on Micron and Amidi. Dec. 12–13, 66–67.

(5) Claim 9 is rejected based on (a) Dell 1[22] and JEDEC under 35 U.S.C. § 103 (RAN 13, 36–39) (Ground 9), (b) Wong[23] and JEDEC under 35 U.S.C. § 103 (RAN 13, 41–43) (Ground 11), and (c) Micron and Connolly[24] under 35 U.S.C. § 103 (RAN 13, 44–47) (Ground 12). Dec. 12–13.

We also note the Examiner's decision not to adopt the proposed rejection of claims 16 and 17 based on Amidi and Dell 2 remains affirmed and we do not reach the propriety of the non-adopted rejection of claim 119 under Ground 5. Dec. 82–83.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

<u>37 C.F.R. § 41.77(f)</u>

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[22] U.S. Patent No. 5,926,827 (issued July 20, 1999) (Dell 1).
[23] U.S. Patent No. 6,414,868 (issued July 2, 2002) (Wong).
[24] U.S. Patent No. 5,745,914 (issued April 28, 1998) (Connolly).

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95/000,578	10/20/2010	7619912	17730-3	8810

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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
01/31/2019	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

_____

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

_____

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and
JEREMY J. CURCURI, *Administrative Patent Judges.*

POTHIER, *Administrative Patent Judge.*

DECISION ON REHEARING

Appeal 2018-003618
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Patent 7,619,912 B2

This merged proceeding involves U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon. This is a request by Requester 3, Google Inc., for a rehearing under 37 C.F.R. § 41.79 ("Req. for Reh'g") of our Decision Under 37 C.F.R. § 41.77(f) ("Decision 2") dated July 27, 2018, on the Examiner's Determination Under 37 C.F.R. § 41.77(d) ("Ex. Deter.") mailed October 3, 2017. Decision 2 is subsequent to and incorporates a Decision dated June 6, 2016 ("Decision 1")[1] in which new grounds of rejection were entered under 37 C.F.R. § 41.77(b).

In response to the new grounds of rejection, Patent Owner reopened prosecution, amending claims and submitting new evidence for consideration. Patent Owner's Response Requesting to Reopen Prosecution Pursuant to 37 C.F.R. § 41.77(b)(1) ("PO Request"), pp. 2–57 (August 1, 2016). Requester 3 responded, urging the new grounds of rejection be maintained. *See generally* Requester 3's Comments Pursuant to 37 C.F.R. §41.77(c) ("R3 Comments") (August 31, 2016). In Decision 2, we withdrew many rejections maintained or adopted by the Examiner (Decision 2, pp. 40–41) while other rejections of certain claims remain affirmed (Decision 2, pp. 41–42).

Requester 3 sets forth three occasions in Decision 2 where we allegedly misapprehended or overlooked points in withdrawing the new grounds of rejection presented in Decision 1. First, Requester 3 contends we overlooked findings in concluding that cited prior art does not render the "logic element" limitation in claim 1 and other independent claims obvious. Req. for Reh'g 2–6. Second, Requester 3 argues we misapprehended the meaning of the "logic element"

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[1] In Decision 2, we state "Our new Decision is deemed to incorporate the earlier Decision, except for those portions specifically withdrawn. 37 C.F.R. §41.77(f)." Decision 2, 5.

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limitation in determining this limitation has written description support. Req. for
Reh'g 6–7. Third, because we determined there is written description support for
the recitation "logic element," Requester 3 asserts we overlooked that the prior art
supports the obviousness rejection grounds. Req. for Reh'g 8–9. We are not
persuaded.

Requester 3 presents arguments for the claims as group. *See generally* Req.
for Reh'g. We select claim 1 as representative. *See* 37 C.F.R. §41.67(c)(1)(vii).

*"Logic Element" in Claim 1 is Purportedly Taught by
Requester 3 Newly Proposed Ground*

Requester 3 asserts we found Amidi discloses receiving all four claimed
signals "by its logic elements and some use of all four claimed signals in logic
operations performed by those logic elements." Req. for Reh'g 3 (citing Decision
2, p. 18). Requester 3 further states we found Amidi teaches its CPLD (complex
programmable logic device) receives a row address signal and a chip select-select
signal and generates a chip-select signal in response. Req. for Reh'g 3 (citing
Decision 2, pp. 13–14). We are not persuaded we misapprehended Amidi such
that it teaches the claimed "logic element" limitation in claim 1.

The "logic element" limitation recites "the logic element generates gated
column access strobe (CAS) signals or chip-select signals of the output control
signals in response at least in part to (i) the at least one row address signal, (ii) the
bank address signals, and (iii) the at least one chip-select signal of the set of input
control signals and (iv) the PLL clock signal."[2] PO Request 3. In Decision 2, we
stated Amidi teaches register 608 (e.g., a logic element) receiving row address

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[2] In Decision 2, we referred to this limitation as "the 'logic element' limitation"
and "the response signals collectively as signals (i)–(iv) or individually as signal
(i), (ii), (iii), and (iv)." Decision 2, p. 10. We similarly do so here.

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NOTICE OF INTENT TO ISSUE INTER PARTES REEXAMINATION CERTIFICATE	**Control No.** 95/000,578 & 95/000,579 & 95/001,339	**Patent Under Reexamination** 7619912
	Examiner BEHZAD PEIKARI	**Art Unit** 3992

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address.* --

1. ☑ Prosecution on the merits is (or remains) closed in this inter partes reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of:

    a. ☐ The communication filed on _____ by _____ .

    b. ☐ Patent owner's failure to file an appropriate timely response to the Office action dated _____ .

    c. ☐ The failure to timely file an Appeal with fee by all parties to the reexamination proceeding entitled to do so. 37 CFR 1.959 and 41.61

    d. ☐ The failure to timely file an Appellant's Brief with fee by all parties to the reexamination proceeding entitled to do so. 37 CFR 41.66(a).

    e. ☑ The decision on appeal by the ☐ Board of Patent Appeals and Interferences ☑ Court dated <u>15 June 2020</u>

    f. ☐ Other: _____

2. ☑ The Reexamination Certificate will indicate the following:

    a. Change in the Specification: ☐ Yes   ☑ No

    b. Change in the Drawings: ☐ Yes   ☑ No

    c. Status of the Claims:

        (1) Patent claim(s) confirmed _____ .

        (2) Patent claim(s) amended (including dependent on amended claim(s)): <u>See Continuation Sheet</u>

        (3) Patent claim(s) cancelled: <u>2,5,7,9,21,23,25-26,30,33,42,44 and 51</u> .

        (4) Newly presented claim(s) patentable: <u>See Continuation Sheet</u> .

        (5) Newly presented cancelled claims: <u>See Continuation Sheet</u> .

        (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____

        (7) Patent claim(s) not subject to reexamination: _____ .

3. ☑ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."

4. ☐ Note attached NOTICE OF REFERENCE CITED, (PTO-892).

5. ☑ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).

6. ☐ The drawings filed on _____ is: ☐ approved. ☐ disapproved.

7. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. § 119(a) - (d) or (f).
    a) ☐ All   b) ☐ Some*   c) ☐ None   of the certified copies have

        ☐ been received.

        ☐ not been received.

        ☐ been filed in Application No. _____ .

        ☐ been filed in reexamination Control No. _____ .

        ☐ been received by the International Bureau in PCT Application No. _____ .

    * Certified copies not received: _____ .

8. ☑ Note Examiner's Amendment.

9. ☐ Other: _____ .

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

/B. JAMES PEIKARI/ Primary Examiner, Art Unit 3992	/Alex Kosowski/ SPRS, CRU	/CMT/ Primary Examiner, AU3992

U.S. Patent and Trademark Office   Part of Paper No. 20201202

PTOL-2068 (07-10)   **NOTICE OF INTENT TO ISSUE *INTER PARTES* REEXAMINATION CERTIFICATE**

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Art Unit: 3992

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent

provisions.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below:

- Cancel claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119

- Amend claim 58 as follows:

58.   (New)   A memory module connectable to a computer system, the memory

module comprising:

a printed circuit board:

a plurality of double-data-rate (DDR) memory devices mounted to the printed

circuit board, the plurality of DDR memory devices having a first number of DDR

memory devices arranged in a first number of ranks:

a circuit mounted to the printed circuit board, the circuit comprising a logic

element and a register, the logic element receiving a set of input control signals from the

computer system, the set of input control signals comprising at least one row/column

address signal, bank address signals, and at least one chip-select signal, the set of

input control signals corresponding to a second number of DDR memory devices

arranged in a second number of ranks, the second number of DDR memory devices

smaller than the first number of DDR memory devices and the second number of ranks

less than the first number of ranks, the circuit generating a set of output control signals

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Art Unit: 3992

in response to the set of input control signals, the set of output control signals

corresponding to the first number of DDR memory devices arranged in the first number

of ranks, wherein the circuit further responds to a first command signal and the set of

input control signals from the computer system by generating and transmitting a second

command signal and the set of output control signals to the plurality of memory devices,

the first command signal and the set of input control signals corresponding to the

second number of ranks and the second command signal and the set of output control

signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock

loop device operatively coupled to the plurality of DDR memory devices, the logic

element, and the register,

wherein operation of the register is responsive at least in part to clock signals

received from the phase-lock loop device and the logic element generates a first

number of chip-select signals of the set of output control signals in response at least in

part to clock signals received from the phase-lock loop device, the first number of chip-

select signals generated by the logic element equal to the first number of ranks, and the

at least one chip-select signal of the set of input control signals comprises a second

number of chip-select signals equal to the second number of ranks,

wherein the bank address signals of the set of input control signals are received

by the logic element,

wherein a plurality of row/column address signals and the bank address signals

are received from the computer system and buffered by the register, the register

transmitting the buffered plurality of row/column address signals and the buffered bank

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address signals to the plurality of DDR memory devices, wherein the at least one

row/column address signal received by the logic element comprises at least one row

address signal received by the logic element, and wherein the plurality of row/column

address signals received by the register are separate from the at least one row address

signal received by the logic element, and

    wherein the generation of the first number of chip-select signals of the output

control signals by the logic element is based on the logic element responsive at least in

part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the

at least one chip-select signal of the set of input control signals received by the logic

element and (iv) the clock signals received from the phase-lock loop device.

Note: New claims 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90,

91, 109-111, 120, 122, 123, 125-127 and 131-136 are renumbered as 52-91, not

respectively, but in an order that immediately follows the highest numbered patent claim

(for example, claim 58 above is now renumbered as claim 80).

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STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

Summary of claim status:

- Claims 1-51 were original patent claims.

- Claims 52-136 were newly added during the course of this reexamination proceeding.

- Claims 25, 42, 44, 51, 53, 55, 59, 64-66, 68, 72-74, 76, 79, 84, 89, 92-108, 112-118, 121, 124, and 128-130 were canceled by patent owner during the course of this reexamination proceeding.

- Claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57 and 119 have rejections that have been upheld by the CAFC and are canceled by the examiner's amendment above.

- Claims 1, 3, 4, 6, 8, 10-20, 22, 24, 27-29, 31, 32, 34-41, 43 and 45-50 are patent claims that have been amended or are dependent on claims that have been amended by patent owner during the course of this reexamination proceeding.

- No original, unamended patent claims remain pending.

- Claim 58 is amended to independent form by the examiner's amendment above, to avoid a claim formatting error.

- **Claims 1, 3, 4, 6, 8, 10-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52, 54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123, 125-127 and 131-136 are found patentable in this reexamination proceeding.**

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The following is an examiner's statement of reasons for patentability and/or confirmation

of the claims found patentable in this reexamination proceeding:

On June 15, 2020, the U.S. Court of Appeals for the Federal Circuit (CAFC) affirmed the

following decisions by the Patent Trial and Appeal Board (PTAB):

> May 31, 2016 (for 95/000,578 and 95/001,339)
>
> June 6, 2016 (for 95/000,579)
>
> June 1, 2018 / July 27, 2018 (under 37 C.F.R. § 41.77(f))
>
> January 31, 2019 (Decision on Rehearing)

Consequently, claims 1, 3, 4, 6, 8, 10-20, 22, 24, 27-29, 31, 32, 34-41, 43, 45-50, 52,

54, 56, 58, 60-63, 67, 69-71, 75, 77, 78, 80-83, 85-88, 90, 91, 109-111, 120, 122, 123,

125-127 and 131-136 are patentable.

Any comments considered necessary by the PATENT OWNER regarding the above

statement must be submitted promptly to avoid processing delays. Such submission by

the patent owner should be labeled: "Comments on Statement of Reasons for

Patentability and/or Confirmation" and will be placed in the reexamination file.